

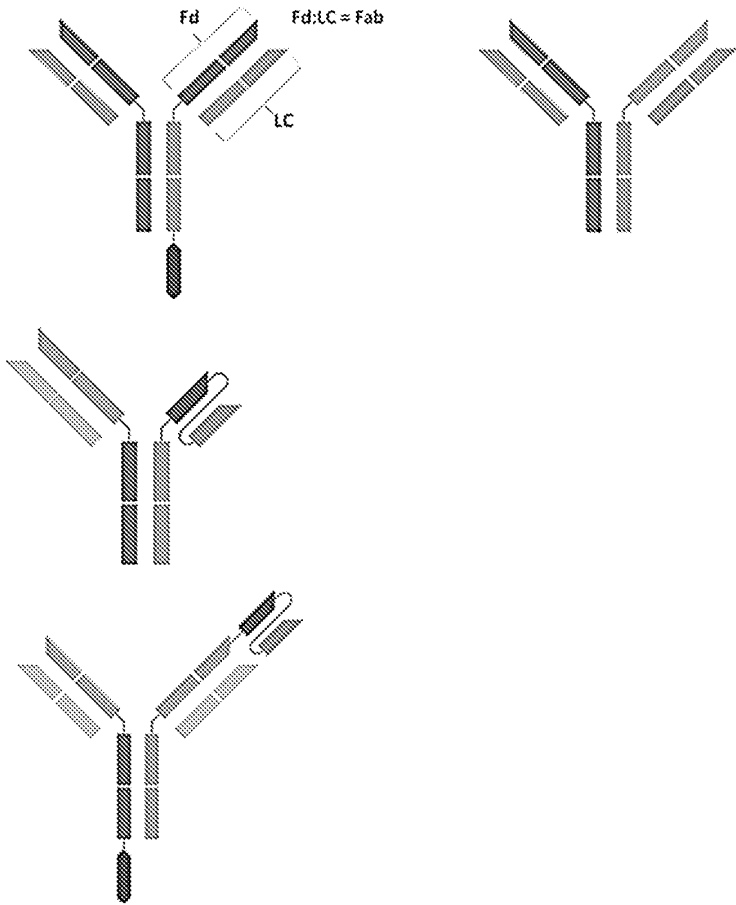


FIG. 1A

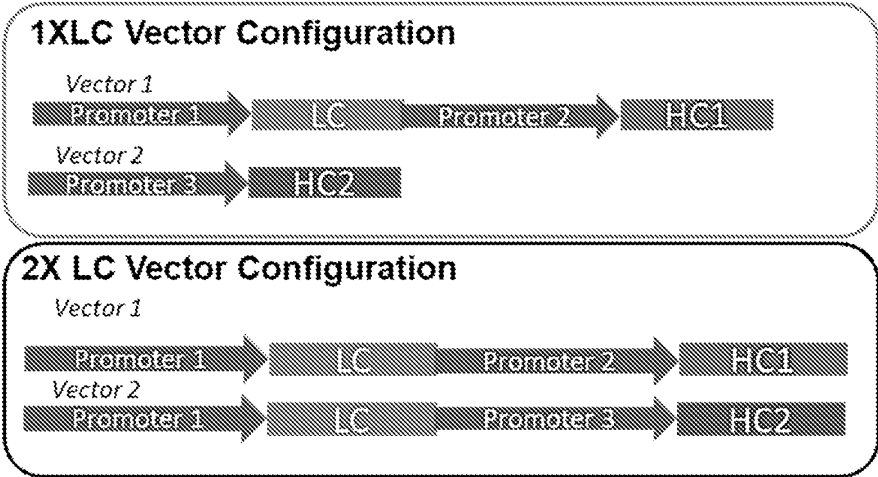


FIG. 1B

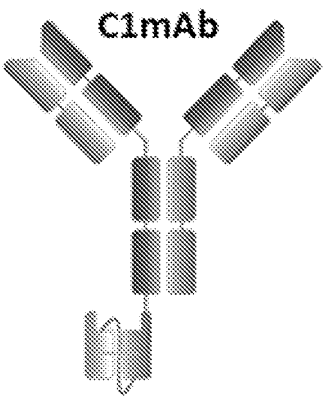
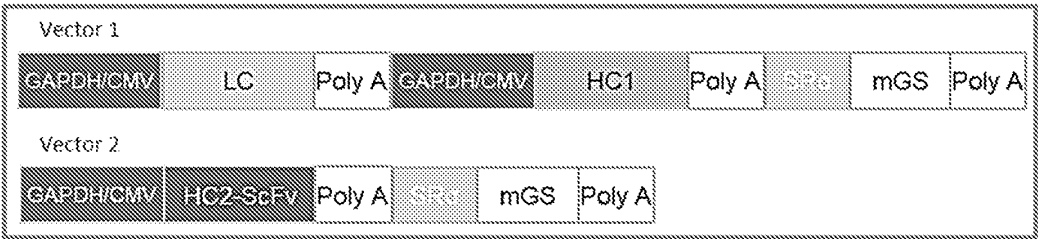


FIG. 2A

1x LC vector configuration:



2x LC vector configuration:

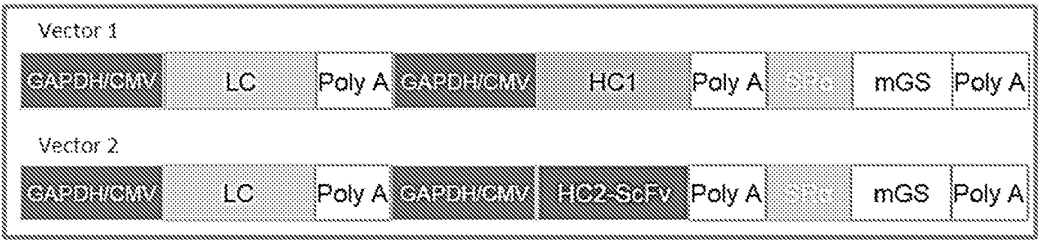


FIG. 2B

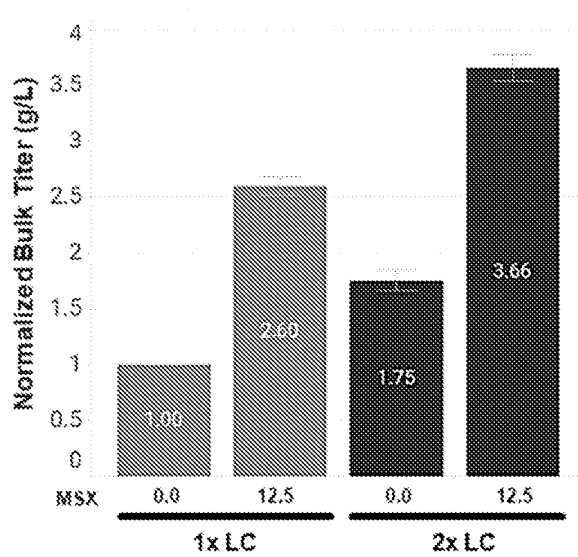


FIG. 3A

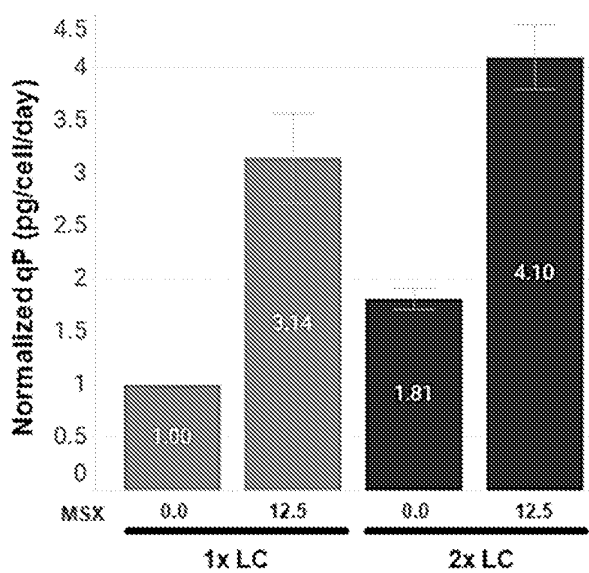


FIG. 3B

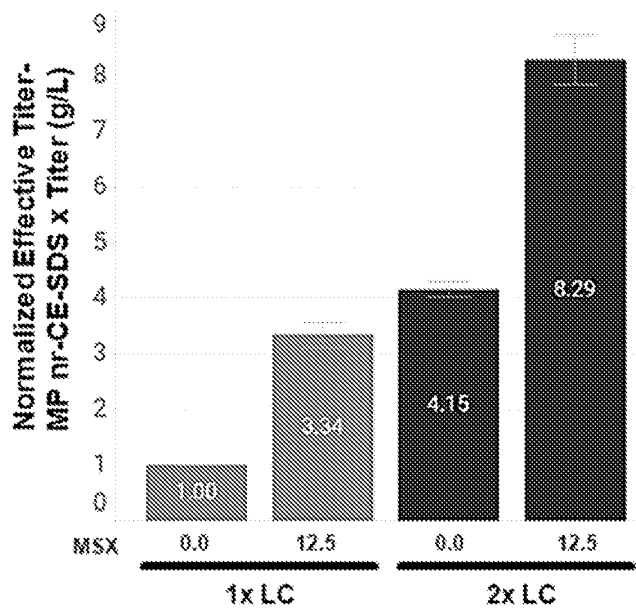


FIG. 4A

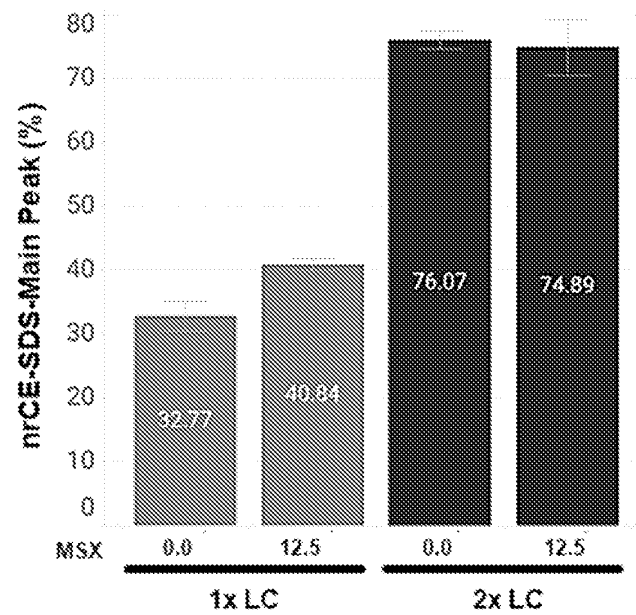


FIG. 4B

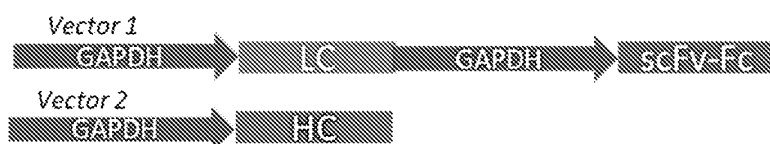
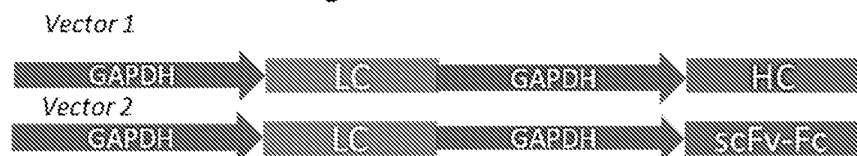
1XLC1 Vector Configuration**1XLC2 Vector Configuration****2X LC Vector Configuration**

FIG. 5

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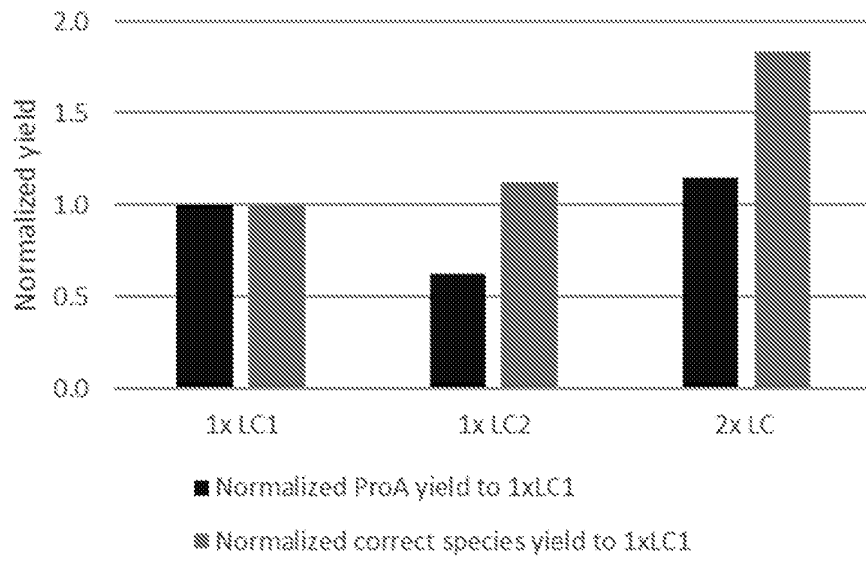


FIG. 6A

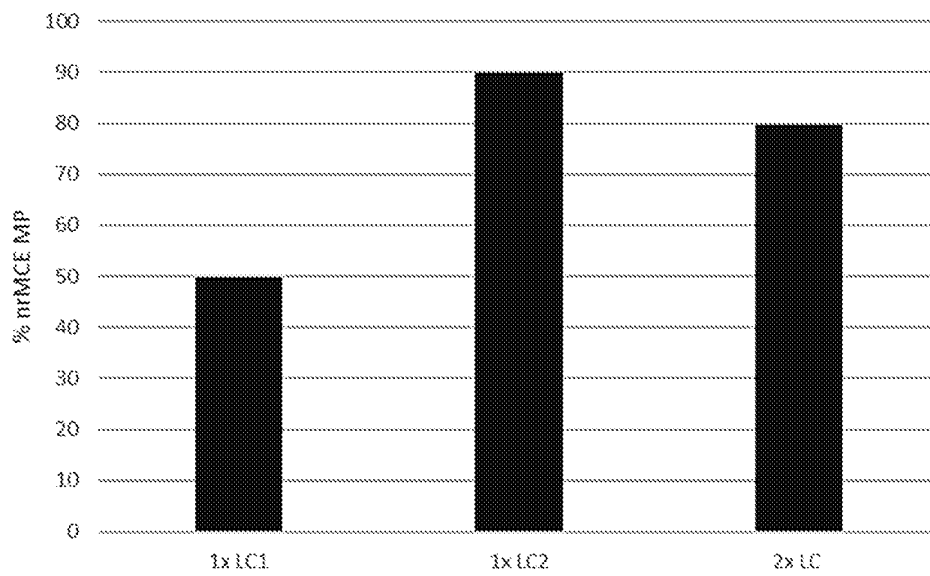


FIG. 6B

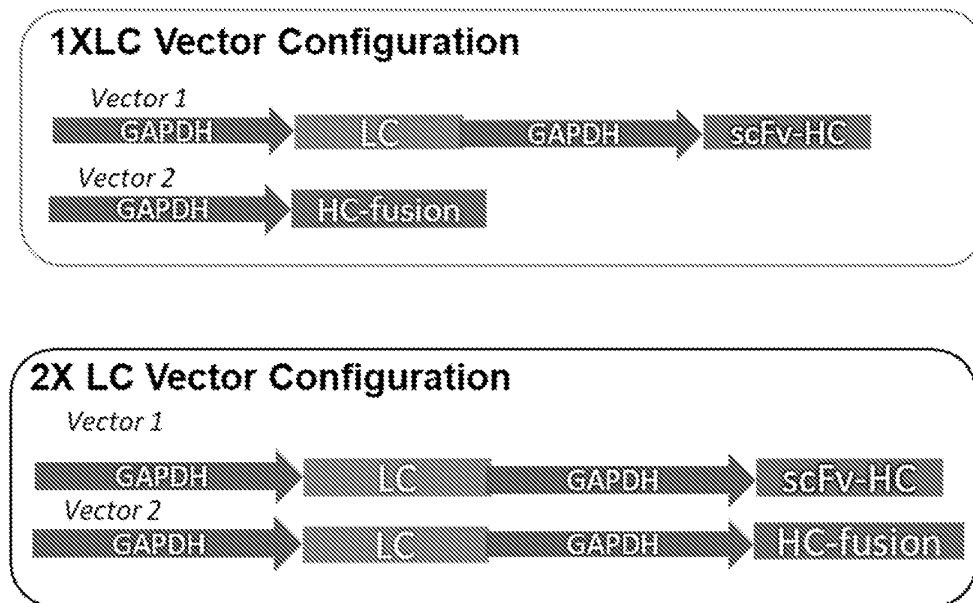


FIG. 7

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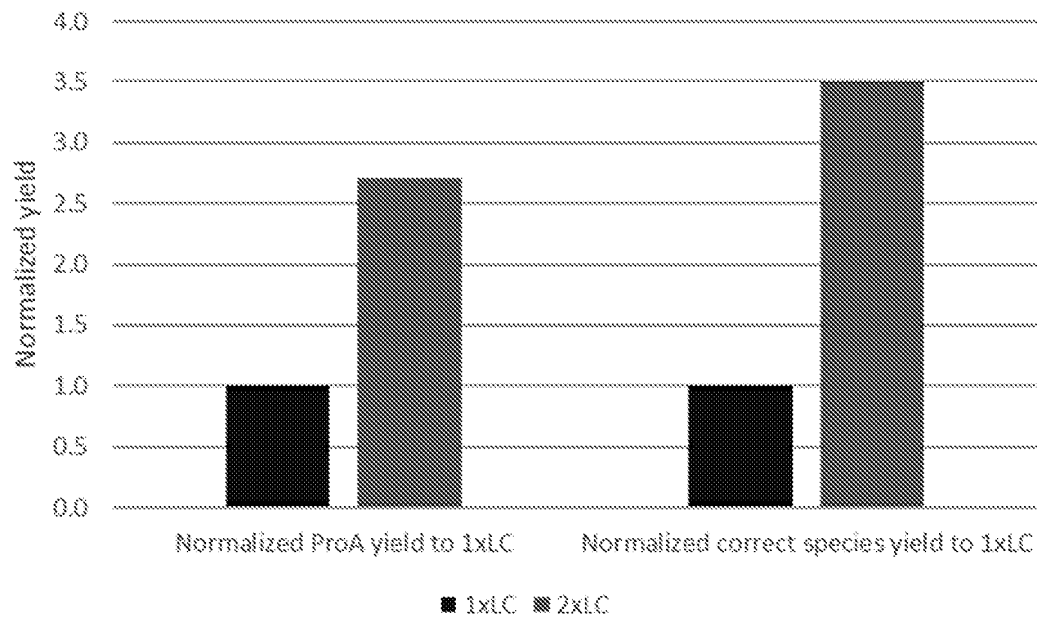


FIG. 8A

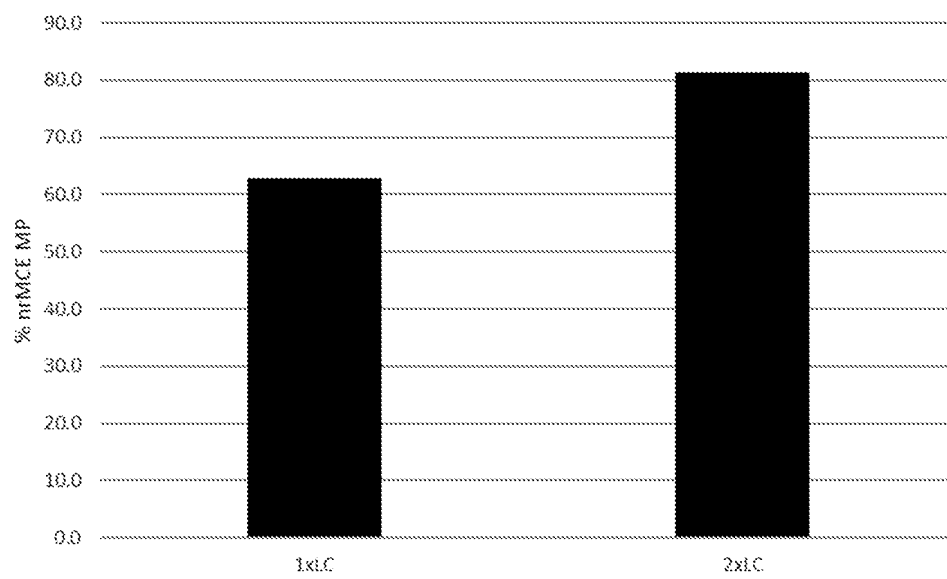


FIG. 8B

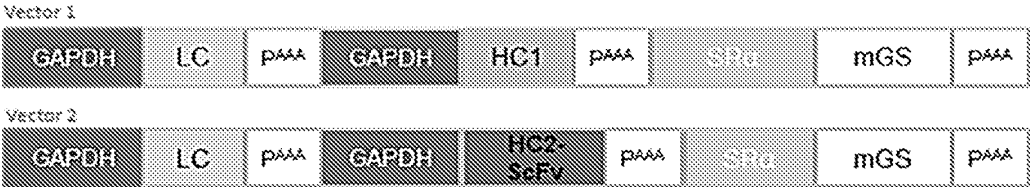


FIG. 9