CLAIMS

1. A semiconductor structure, comprising:

a first capacitive structure and first support columns located on a substrate, wherein a plurality of first support columns are disposed on the substrate in parallel and spaced apart from each other, the first capacitive structure comprises a first lower electrode layer, a first dielectric layer and a first upper electrode layer, the first lower electrode layer covers the substrate and sidewall surfaces of the first support columns, the first dielectric layer covers the first lower electrode layer, and the first upper electrode layer covers the first dielectric layer; and

a plurality of first segmentation trenches that are disposed on the substrate in parallel and spaced apart from each other, wherein an extending direction of the first segmentation trenches is perpendicular to the first support columns, the first segmentation trenches divide the first capacitive structure into a plurality of capacitors, a first insulation layer is formed in each of the plurality of first segmentation trenches, the first insulation layer is disposed between corresponding first lower electrode layers of adjacent capacitors, the first lower electrode layers of adjacent capacitors electrically connected to each other by the first support columns, the first insulation layer covers the substrate and the sidewall surface of the first support column corresponding to the first segmentation trench, and the corresponding first upper electrode layers of the adjacent capacitors are electrically connected to each other by filling a conductive material into the first segmentation trench.

2. The semiconductor structure of claim 1, wherein a material of the first insulation layer comprises a material having a high dielectric constant, silicon oxide, silicon nitride or silicon oxynitride.

3. The semiconductor structure of claim 2, wherein a thickness of the first insulation layer is greater than a thickness of the first lower electrode layer, and is less than a sum of the thickness of the first

lower electrode layer and a thickness of the first dielectric layer.

4. The semiconductor structure of claim 1, wherein a material of the first support column comprises single-crystal silicon, single-crystal germanium, single-crystal silicon germanium, or indium gallium zinc oxide.

5. The semiconductor structure of claim 3, wherein the first capacitive structure and the first support columns form first capacitive assemblies; in a direction perpendicular to the substrate, a plurality of first capacitive assemblies arranged in stack are disposed on the substrate; and corresponding first upper electrode layers of adjacent first capacitive assemblies are electrically connected to each other.

6. The semiconductor structure of claim 5, further comprising a first support layer and a second support layer covering the substrate, wherein the first support layer and the second support layer surround the sidewall surface of the first support column; each first capacitive assembly is located between the first support layer and the second support layer; and the first dielectric layer covers sidewalls of the first support layer and the second support layer.

7. The semiconductor structure of claim 5, further comprising an isolation portion located on the substrate and a plurality of second capacitive assemblies, wherein in the direction perpendicular to the substrate, the plurality of second capacitive assemblies arranged in stack are disposed on the substrate; the isolation portion is located between the first capacitive assemblies and the second capacitive assemblies; and the first capacitive assemblies and the second capacitive assemblies are symmetrically disposed with respect to the isolation portion.

8. A method for manufacturing a semiconductor structure, comprising:

providing a substrate;

forming a plurality of first support columns that are disposed on the substrate in parallel and spaced apart from each other;

forming a first capacitive structure comprising a first lower electrode layer, a first dielectric layer and a first upper electrode layer, wherein the first lower electrode layer covers the substrate and sidewall surfaces of the first support columns, the first dielectric layer covers the first lower electrode layer, and the first upper electrode layer covers the first dielectric layer;

forming a plurality of first segmentation trenches that are disposed on the substrate in parallel and spaced apart from each other, wherein an extending direction of the first segmentation trenches is perpendicular to the first support columns, and the first segmentation trenches divide the first capacitive structure into a plurality of capacitors;

forming a first insulation layer in the first segmentation trench, wherein the first insulation layer is disposed between the first lower electrode layers of adjacent capacitors, the first lower electrode layers of adjacent capacitors electrically connected to each other by the first support columns, and the first insulation layer covers the sidewall surface of the first support column corresponding to the first segmentation trench and the substrate; and

filling a conductive material into the first segmentation trench, to electrically connect the corresponding first upper electrode layers of the adjacent capacitors to one another.

9. The method for manufacturing a semiconductor structure of claim 8, wherein a material of the first insulation layer comprises a material having a high dielectric constant, silicon oxide, silicon nitride or silicon oxynitride.

10. The method for manufacturing a semiconductor structure of claim 8, wherein a thickness of the first insulation layer is greater than a thickness of the first lower electrode layer, and is less than a sum of thickness of the first lower electrode layer and a thickness of the first dielectric layer.

11. The method for manufacturing a semiconductor structure of claim 9, wherein a material of the first support column comprises single-crystal silicon, single-crystal germanium, single-crystal silicon germanium, or indium gallium zinc oxide.

12. The method for manufacturing a semiconductor structure of claim 11, wherein the forming a first support column comprises:

forming a sacrificial layer covering the substrate;

removing a part of the sacrificial layer to form a plurality of first grooves disposed on the substrate in parallel and spaced apart from each other;

forming filling layers in the first grooves;

removing a part of the sacrificial layer and a part of the filling layers to form a plurality of second grooves, wherein the plurality of second grooves are disposed on the substrate in parallel and spaced apart from each other, and an extending direction of the second grooves is perpendicular to the first grooves;

removing a part of the sacrificial layer to form a plurality of filling channels spaced from one another and disposed parallel to the first grooves; and

forming the first support column in each filling channel.

13. The method for manufacturing a semiconductor structure of claim 12, wherein the sacrificial

layer comprises a first sacrificial layer and a second sacrificial layer that are alternately disposed and stacked onto one another; the removing a part of the sacrificial layer to form filling channels comprises:

removing the second sacrificial layer of the sacrificial layer with the first sacrificial layer being retained, to form filling structures stacked on the substrate, wherein, in a direction perpendicular to the substrate, each filling structure comprises the filling channels that are spaced apart from each other and are disposed in parallel; and

the forming a first capacitive structure further comprises: forming a plurality of first capacitive assemblies which are formed by the first capacitive structure and the first support columns and are stacked in the direction perpendicular to the substrate, wherein corresponding first upper electrode layers of adjacent first capacitive assemblies are electrically connected to each other.

14. The method for manufacturing a semiconductor structure of claim 13, wherein, while the first support columns are formed in the filling channels, the method further comprises:

forming intermediate support layers in the second grooves; and

the forming a first capacitive structure further comprises:

removing a part of the intermediate support layers; and

forming second support layers in a part of the second grooves.

15. The method for manufacturing a semiconductor structure of claim 14, wherein, after the first support columns are formed in the filling channels, the method further comprises:

removing a part of the filling layers to form a plurality of third grooves, wherein the plurality of third grooves are disposed on the substrate in parallel and spaced apart from each other, and an extending direction of the third grooves is perpendicular to the first grooves;

removing the sacrificial layer corresponding to sidewalls of the third grooves with the first support columns being retained, to form filling sidewalls; and

forming first support layers in a part of the filling sidewalls, wherein the first support layers surround the sidewall surfaces of the first support columns.

16. The method for manufacturing a semiconductor structure of claim 15, wherein the forming a first capacitive structure further comprises:

removing a part of the sacrificial layer and the filling layers to retain the first support columns and the first support layers;

forming the first lower electrode layers on the first support columns and the substrate by means of a selective growth process; and

successively forming the first dielectric layers and the first upper electrode layers.

17. The method for manufacturing a semiconductor structure of claim 15, wherein the forming first segmentation trenches comprises:

removing a part of the first support layers.

18. The method for manufacturing a semiconductor structure of claim 14, further comprising:

forming an isolation portion while the first support columns are formed; and

the forming a plurality of first capacitive assemblies further comprises: forming a plurality of second capacitive assemblies stacked in the direction perpendicular to the substrate, wherein the isolation portion is located between the first capacitive assemblies and the second capacitive assemblies, and the first capacitive assemblies and the second capacitive assemblies are symmetrical

with respect to the isolation portion.