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PATENT SPECIFICATION

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(54) COUNTING APPARATUS

(71) We, HEWLETT-PACKARD COMPANY, a corporation organised and existing under the laws of the State of California, United States of America, of 1501 Page Mill Road, Palo Alto, State of California, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to a counting apparatus, especially digital signal apparatus.

Certain known commercial instruments commonly count input pulses recurring at an unknown rate for a period of time determined by the known recurrence rate of reference pulses to provide an output indication of frequency of the input pulses. These commercial instruments are also usually capable of counting the recurring reference events for a period of time determined by the recurrence rate of input pulses to provide an output indication of the period of input events. This period-measuring mode of operation usually provides greater measurement resolution in a given measuring interval because the recurrence rate of the reference pulses that are counted may be chosen to be at about the upper limit of counting speed of the instrument for all operating values of recurrence rates of input events. However, the resulting indication of period measurement is less acceptable than the direct indication of frequency provided by the former operating mode, and a calculation is required whenever it is desired to convert the period indication to an indication of frequency.

The present invention seeks to provide the resolution of conventional period counters as well as the direct display provided by conventional frequency counters.

Accordingly, the present invention provides a digital signal apparatus comprising first and second signal-counting means, each for accumulating a count of the number of signals applied thereto; a source of reference signals and an input terminal for receiving applied signals other than the reference signals; first and second gating means, each being enabled to pass signals therethrough in response to a control signal applied thereto; said first gating means being connected to apply reference signals from said source to the first signal-counting means and said second gating means being connected to apply signals appearing at said input terminal to the second signal-counting means; gate control means coupled to each of said gates for applying control signals thereto for selected time intervals of substantially equal duration; divider means responsive to the accumulated counts in each of the first and second signal-counting means for producing an output proportional to the quotient of the accumulated count in one of the first and second signal-counting means divided by the accumulated count in the other of the first and second signal-counting means; and display means responsive to said output for producing an output indication of said quotient of the one accumulated count divided by the other accumulated count.

The invention will now be more particularly described with reference to the accompanying drawings, in which:

Figure 1 is a schematic diagram of a conventional counter apparatus capable of measuring period or frequency of input pulses,

Figure 2 is a schematic diagram of the circuit of the present invention, and

Figure 3 is a graph showing operating waveforms of the circuit of Figure 2.

Referring now to the conventional counter apparatus of Figure 1, there is shown a simplified arrangement of a pair of scalers 9, 11, a gate 13 and mode-selecting switching means 15. Counter apparatus of this type is widely reported in the literature and accordingly is discussed only briefly herein. The scaler 9 may also be referred to as one

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or more decade counting units, each of which counts groups of ten applied pulses and produces a carry signal for application to the next unit in line. Each decade counting unit thus scales down the repetition rate of applied pulses by ten so that, with display means associated with each unit, the units may count and display the total number of applied pulses according to units, tens, hundreds, thousands, etc. designations of the displayed digits.

Pulses to be counted may be applied to the scaler 9 for a predetermined counting interval. The gate 13 controls application of pulses to scaler 9 in accordance with the operating mode selected by switching means 15. In the FREQuency-measuring mode, the switching means 15 (in the position as shown) applies the unknown signal from a source 17 to the scaler 9 through gate 13 for an interval of time which is determined by the reference signal from source 19 and scaler 11. The scaler 11 usually includes one or more decade dividers, each of which produces an output for application to a succeeding divider in response to ten pulses applied thereto. In this way, the gate 13 passes the unknown signal from source 17 to the scaler 9 for an interval that is decimally related to the frequency of the reference signal from source 19. If this measurement interval is related to one second in time, then the display means associated with scaler 9 may thus provide a direct display of frequency in Hertz of the unknown signal from source 17.

When the switching means is set in the PERIOD mode (alternate position as shown), then the scaler 9 counts reference signals from source 19 for an interval determined by the unknown signal from source 17. The time interval during which gate 13 is conductive is determined by the decade division by the scaler 11 of the frequency of the unknown signal from source 17. The display means associated with scaler 9 thus provides a direct display of the number of reference signals from source 19 which were counted during the unknown time interval and this display thus represents the average period between the unknown signals from source 17. However, in order to obtain the desired information about the frequency of the unknown signal from source 17, a calculation must be performed on the direct display to obtain the reciprocal of the period indication.

Referring now to Figure 2 which shows a circuit diagram of one embodiment of the present invention, there is shown a counter 21 arranged to count the unknown input signal N_x and a counter 23 arranged to count the reference signal N_o from a reference source or clock 25. In accordance with the present invention, both counters 21 and 23 are operated simultaneously for substantially identical counting intervals to accumulate total counts of unknown input signals (in counter 21) and of reference signals (in counter 23) from clock 25. The counting interval for the two counters is controlled by the gates 27, 29 connected in the respective input lines to the counters 21, 23, which gates 27, 29 receive a synchronized gate signal, as shown in Figure 3c, from the asynchronous to synchronous converter circuit 31. This converter circuit 31 receives from the controller 33 an asynchronous arming signal (Figure 3b) that has a length or duration which is representative of the approximate desired counting interval. This approximate counting interval is determined by the controller 33 as the interval of, say, M number of recurrences of the reference signal N_o, as scaled by counter 23. In general, the gate signals (Figure 3b) are not synchronized with occurrences of the unknown input signals (Figure 3a) and therefore may be unsuitable in practice for operating the counting gates 27, 29 where a high degree of measurement accuracy is required. The converter circuit 31 may include conventional clocked flip-flop circuits, or other suitable armable and triggerable circuits, for producing the actual gating signal, as shown in Figure 3c, with leading and trailing edges synchronized with the occurrences of unknown input signals N_x. The gates 27, 29 are thus enabled for the period of the actual counting interval (Figure 3c) which has a duration that is equal to an integer number of occurrences of the unknown signals N_x. Counter 21 thus counts an integer number of recurrences of the unknown signals N_x during the actual counting interval (Figure 3c) and counter 23 counts the number of recurrences of the reference signal from clock 25 during the same counting interval.

At the end of the actual counting period, Figure 3c, controller 33 disables the gates 27 and 29, thereby preventing the counters 21, 23 from accumulating additional counts. The counts of signals in the counters 21, 23 are transferred through transfer gates 32, 34 to the shift registers 35, 37, respectively, in response to a transfer command (Figure 3e) applied to the transfer gates 32, 34 by the controller 33. Each of the shift registers 35, 37 attains an operating state that corresponds to the count transferred thereto from the associated counters 21, 23. The operating states of the shift registers 35, 37 typically include several data bits or logic stages, each of which or groups of which may represent selected digits of the counts transferred thereto. It should be understood that the individual digit stages of the counters 21, 23 may also serve as the shift register stages directly. In this way, the logic ele-

ments per digit which operate to accumulate counts during the actual gating period of Figure 3c may then be interrogated in digit sequence upon command (say, Figure 3e) during the division operation to yield the desired dividend and divisor numbers.

During the division operation, the data bits or logic states of each register 35, 37 (or counter-register 21, 23) may be supplied to an arithmetic divider 39 which divides the number (dividend) represented by the logic states in register 35 by the number (divisor) represented by the logic states in register 37. The divider 39 may perform conventional computer division operations on the data bits or logic states of the registers 35, 37 which are sequentially applied to the divider in a conventional manner (see, for example, British Patent Specifications Nos. 1,197,291 and 1,197,292). The quotient of the two numbers represented by the logic states in registers 35, 37 is thus a direct indication of the frequency of the input signal N_x. The quotient may be supplied to a suitable display means 41 to provide a visual indication of the frequency of the input signal. This display means 41 may include conventional display storage circuitry, decoding circuitry, and the like, for maintaining a continuous display as the associated circuitry is disconnected therefrom to perform another measurement operation, as described above. Alternatively, since the time required for division is typically less than one millisecond, one of the existing registers such as 35 or 37 or a register for accumulating the quotient may also be used for display storage during the time it is not being used for computation. If computations are frequent, display blanking may be employed to mask the computational use of the storage register.

After the counts in counters 21, 23 are transferred to the registers 35, 37, respectively, the counters may then be reset by a signal on line 43 from the controller 33 and the gates 27, 29 may be enabled again to permit the counters 21, 23 to accumulate new counts of the input and reference signals, respectively.

Operation of the illustrated embodiment of the present invention in the manner described above thus assures that the usual ± 1 count ambiguity is referred to the reference signal which has a frequency that is high and near the limit of counting speed of counter 23. This provides the high measurement resolution usually obtained with period counters as well as the direct frequency readout usually obtained with frequency counters. Also, the arithmetic processing of two independent counts provides versatility in the selection of measurement time and the convenience of direct display of frequency over a wide range of unknown input signal frequencies. The present invention also accurately measures pulse modulated signals or signal bursts since the asynchronous to synchronous converter 31 can be armed by the controller 33 in the absence of an input signal. The measurement will then start on receipt of an input signal and, as long as the measurement time is less than the burst duration, an accurate measurement will be made.

WHAT WE CLAIM IS:—

1. Digital signal apparatus comprising first and second signal-counting means, each for accumulating a count of the number of signals applied thereto; a source of reference signals and an input terminal for receiving applied signals other than the reference signals; first and second gating means, each being enabled to pass signals therethrough in response to a control signal applied thereto; said first gating means being connected to apply reference signals from said source to the first signal-counting means and said second gating means being connected to apply signals appearing at said input terminal to the second signal-counting means; gate control means coupled to each of said gates for applying control signals thereto for selected time intervals of substantially equal duration; divider means responsive to the accumulated counts in each of the first and second signal-counting means for producing an output proportional to the quotient of the accumulated count in one of the first and second signal-counting means divided by the accumulated count in the other of the first and second signal-counting means; and display means responsive to said output for producing an output indication of said quotient of the one accumulated count divided by the other accumulated count.

2. Digital signal apparatus as claimed in Claim 1, wherein said gate control means includes means coupled to said input terminal for applying control signals simultaneously to said first and second gating means substantially in synchronism with signals appearing at said input terminal.

3. Digital signal apparatus as claimed in Claim 2, wherein said gate control means includes a trigger circuit which produces said control signal in response to a triggering signal applied thereto following arming of the trigger circuit in response to an arming signal applied thereto; means are coupled to said gate control means for applying thereto an arming signal derived from said reference signal; and means are coupled to said gate control means for applying a triggering signal thereto derived from signals appearing at said input terminal for initiating and terminating said control signal in synchronism with signals at said input ter-

ments per digit which operate to accumulate counts during the actual gating period of Figure 3c may then be interrogated in digit sequence upon command (say, Figure 3e) during the division operation to yield the desired dividend and divisor numbers.

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minal that appear, respectively, after said arming signal is applied to said gate control means and after said arming signal is removed.

4. Digital signal apparatus constructed and operable as hereinabove described with reference to, and as illustrated in, Figure 2 of the accompanying drawings.

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