CLAIMS

1. A method of processing a wafer used in fabricating semiconductor devices, said method comprising:

forming multiple high aspect ratio features in a layer on the wafer;

performing wet processing of the wafer;

subsequently completely drying the wafer which causes pattern collapse; and thereafter

repairing by etching at least 60% of the pattern collapse among the multiple high aspect ratio features, wherein a high aspect ratio comprises an aspect ratio of at least ten to one.

2. The method of claim 1 wherein the forming of the multiple high aspect ratio features comprises:

forming a photoresist patterned mask over a silicon based layer;

plasma etching the high aspect ratio features into the silicon based layer.

3. The method of claim 2 wherein the forming of the multiple high aspect ratio features further comprises stripping the photoresist patterned mask.

4. The method of claim 3, wherein an aspect ratio of at least a portion of the multiple high aspect ratio features is 10 to 1 or greater.

5. The method of claim 4, wherein a characteristic dimension of the portion of the multiple high aspect ratio features is less than 40 nm.

6. The method of claim 4, wherein the repairing of the pattern collapse comprises a dry trimming process.

7. The method of claim 6, wherein the repairing the pattern collapse further comprises an etch of a silicon based layer.

8. The method of claim 7, wherein the etch is an STI etch.

9. The method of claim 4, wherein the repairing of the pattern collapse is performed using a wet etch trimming process.

10. The method of claim 9, wherein the wet etch trimming process includes an HF etch.

11. The method of claim 1, wherein the repairing breaks bonds formed between adjacent features during drying.

12. The method of claim 11, wherein the multiple high aspect ratio features comprise a top SiN layer and the bonds are formed in the SiN layer.

13. The method of claim 1, wherein the wet processing of the wafer comprises a wet cleaning process.

14. The method of claim 1, further comprising applying queue time control between an end of the wet processing and the repairing of the pattern collapse to ensure the repairing is performed within a specific time period after the end of the wet processing.

15. The method of claim 1, wherein the multiple high aspect ratio features comprise a top layer of SiN, a middle layer of TEOS and a bottom layer of SiN.

16. The method of claim 1, wherein the layer is a photoresist layer and the wet processing is used to develop a photoresist layer pattern including the multiple high aspect ratio features.

17. A method of processing a wafer used in fabricating semiconductor devices, said method comprising:

forming a photoresist patterned mask over a silicon based layer;

plasma etching multiple high aspect ratio features into the silicon based layer wherein an aspect ratio of at least a portion of the multiple high aspect ratio features is

10 to 1 or greater and wherein a characteristic dimension of the portion of the multiple high aspect ratio features is less than 30 nm;

performing wet processing of the wafer;

subsequently completely drying the wafer which causes pattern collapse; and thereafter

repairing by etching at least 60% of the pattern collapse among the multiple high aspect ratio features using a trimming process.

18. The method of claim 17, the repairing breaks bonds formed between adjacent features during drying.

19. The method of claim 17, wherein the wet processing of the wafer comprises a wet cleaning process.

20. The method of claim 17, further comprising applying queue time control between an end of the wet processing and the repairing of the pattern collapse to ensure the repairing is performed within a specific time period after the end of the wet processing.

CLAIMS

What is claimed is:

1. A method of processing a wafer used in fabricating semiconductor devices, said method comprising:

forming multiple high aspect ratio features in a layer on the wafer;

performing wet processing of the wafer;

subsequently drying the wafer which causes pattern collapse; and

repairing the pattern collapse among the multiple high aspect ratio features.

2. The method of claim 1 wherein the forming of the multiple high aspect ratio features comprises:

forming a photoresist patterned mask over a silicon based layer;

plasma etching the high aspect ratio features into the silicon based layer.

3. The method of claim 2 wherein the forming of the multiple high aspect ratio features further comprises stripping the photoresist patterned mask.

4. The method of claim 3, wherein an aspect ratio of at least a portion of the multiple high aspect ratio features is 10 to 1 or greater.

5. The method of claim 4, wherein a characteristic dimension of the portion of the multiple high aspect ratio features is less than 40 nm.

6. The method of claim 4, wherein the repairing of the pattern collapse comprises a dry trimming process.

7. The method of claim 6, wherein the repairing the pattern collapse further comprises an etch of a silicon based layer.

8. The method of claim 7, wherein the etch is an STI etch.

9. The method of claim 4, wherein the repairing of the pattern collapse is performed using a wet etch trimming process.

10. The method of claim 9, wherein the wet etch trimming process includes an HF etch.

11. The method of any of claims 1 or 2, wherein the repairing breaks bonds formed between adjacent features during drying.

12. The method of claim 11, wherein the multiple high aspect ratio features comprise a top SiN layer and the bonds are formed in the SiN layer.

13. The method of any of claims 1, 2 or 11, wherein the wet processing of the wafer comprises a wet cleaning process.

14. The method of any of claims 1, 2, 11 or 13, further comprising applying queue time control between an end of the wet processing and the repairing of the pattern collapse to ensure the repairing is performed within a specific time period after the end of the wet processing.

15. The method of any of claims 1, 2, 11, 13 or 14, wherein the multiple high aspect ratio features comprise a top layer of SiN, a middle layer of TEOS and a bottom layer of SiN.

16. The method of any of claims 1, 2, 11, 13, 14 or 15, wherein the layer is a photoresist layer and the wet processing is used to develop a photoresist layer pattern including the multiple high aspect ratio features.

17. A method of processing a wafer used in fabricating semiconductor devices, said method comprising:

forming a photoresist patterned mask over a silicon based layer;

plasma etching multiple high aspect ratio features into the silicon based layer wherein an aspect ratio of at least a portion of the multiple high aspect ratio features is 10 to 1 or greater and wherein a characteristic dimension of the portion of the multiple high aspect ratio features is less than 30 nm;

performing wet processing of the wafer;

subsequently drying the wafer which causes pattern collapse; and

repairing the pattern collapse among the multiple high aspect ratio features using a trimming process.

18. The method of claim 17, the repairing breaks bonds formed between adjacent features during drying.

19. The method of any of claims 17 or 18, wherein the wet processing of the wafer comprises a wet cleaning process.

20. The method of any of claims 17, 18, or 19, further comprising applying queue time control between an end of the wet processing and the repairing of the pattern collapse to ensure the repairing is performed within a specific time period after the end of the wet processing.