ENCAPSULATED TAPELESS BOARD-ON-CHIP (BOC) WITH EXPOSED BACKSIDE SILICON CHIP

FIELD OF THE INVENTION

The present invention relates to packaging semiconductor devices and more particularly to packaging board-on-chip (BOC) devices.

BACKGROUND OF THE INVENTION

The semiconductor industry has shown a general trend towards a dramatic increase in integrated circuit speed and density. Both of these trends are fueled by a general reduction in device (active element) geometries. As semiconductor devices become smaller, the distances between them on a semiconductor die becomes smaller, and parasitics (such as parasitic capacitance) and switching currents becomes smaller. In technology's, such as CMOS, where overall current draw and switching speed characteristics are dominated by the effects of parasitics, the result is reduction in total power consumption at the same time as switching speed is improved.

Overall speed is further improved by the reduction in signal propagation time between active devices (for example transistors), resulting from the shorter distances involved. In today's high speed integrated circuitry based on sub-micro geometry, delays are in the tens on hundreds of pico seconds can be appreciable.

Typically, integrated circuit dies (chips or semiconductor dies) are diced (cut apart or singulated) from a semiconductor wafer and are separated into integrated circuit packages which have pins, leads, solder (ball) bumps, or conductor pads by which electrical conductors may be made from external systems to the integrated circuit chip. The packages are then typically applied to the circuit board assemblies including systems of integrated circuit chips.

The above mentioned dramatic improvements in integrated circuit speed and density have placed new demands on integrated circuit assembles, both at the chip and circuit board levels. Without attendant improvements in these areas, much of the benefit of high speed devise speed is lost. Wiring propagation delays and transmission line effects in integrated circuit packages and on circuit board assemblies which were once negligible are now significant factors in the overall performance of systems based on high-speed integrated circuitry. In order to achieve the potential higher system performance opportunities afforded by the new

high density technology, it is necessary to reduce the amount of signal propagation time between integrated circuits.

Another significant factor in achieving high system level performance is signal drive capability. Longer signal paths are susceptible to noise, cross-talk etc. and require low impedance, high current drive circuits on the integrated circuit chip (dies). Such circuits tend to occupy large portions of the die area, either reducing the area available for other circuitry or increasing the overall die size, and such circuits can introduce significant delays of there own. Merely, shorter signal paths and their attendant low signal drive current requirements are desirable to achieve higher performance.

In the prior art, the number of high density chip assemblies and packages have been proposed and then implemented. One such technique is commonly known as the "chip-on-board" technology, whereby integrated circuit dies are bonded directly to die mounting areas on the circuit board substrate, for example, ceramic, fiberglass etc. and are wire bonded (within "bond wires") to traces on the circuit board in

areas adjacent to the edges of the dies. The elimination of the traditional integrated circuit permits chips to be placed much closer together then would otherwise be possible, thereby shorting signal paths and reducing delays. Thus, it is desirable to further decrease the distance between the chip assembles.

SUMMARY OF THE INVENTION

The present invention provides an encapsulated tapeless board-on-chip (BOC) with a silicon chip having an exposed back side. This unique design is applicable to any integrated circuit (IC) such as DRAM, EPROM, FLASH, SRAM, etc. The silicon chip is directly attached to the printed circuit board PCB substrate through a layer of adhesive coating on the surface of a silicon chip or PCB. The wires are connected between the bond pads located approximately at the center of the silicon chip and the stitch pad on the PCB substrate through the PCB slot. The stitch pads are electrically connected to the solder column or solder ball by copper trace routing. A sealing resin for example a liquid epoxy or molding cpd is used to encapsulate the PCB substrate, bonding wires on silicon chip with only its back side being exposed to the atmosphere . The solder columns or solder balls are then placed on the PCB to form a complete BOC component. The silicon chip is directly attached to the PCB substrate by a layer of adhesive coating on the surface on the printed circuit board (PCB) or silicon chip.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig 1 illustrates a PCB with a slot;

Fig 2 illustrates the PCB with adhesive;

Fig 3 illustrates the PCB with chip attached;

Fig 4 illustrates the PCB and chip with formed wire routings and solder column;

Fig 5 illustrates PCB with chip and with enclosed package;

Fig 6 illustrates a top view of the package;

Fig 7 illustrates a cross sectional view of an encapsulated tapeless board-on-chip (BOC) with the exposed backside silicon chip.

DETAILED DESCRIPTION OF THE INV

The silicon chip 400 is directly attached to the PCB substrate 200 by a layer of adhesive coating 300 on the surface of the printed circuit board (PCB substrate 200 and the semiconductor chip 400). Throughout the description of the present invention, top and bottom have no meaning. For purpose of this application, the side of the printed circuit board 200 with the solder columns 500 away from the semiconductor chip 400 is referred to as the top portion of the semiconductor chip 400, and the bottom portion of the printed circuit board 200 is the side opposite to the solder column 500 and as the same side as the semiconductor chip 400.

Turning now to Fig 1, a slot 100 is formed in the PCB substrate 200.

As illustrated in Fig 2, a layer of the adhesive coating 300 is applied to the bottom surface of the printed circuit board substrate 200. One example of the PCB substrate 200 is FR-5 material manufactured by Hitachi, and examples of the adhesive coating 300 could be either

PIX-G-7631-POLYIMIDE or G-8320.

In Fig 3, a semiconductor chip 400 is attached to the adhesive layer 300.

In Fig 4, a hole 502 is formed by etching or another suitable process and extends from the top surface of the printed circuit board substrate 200 down to an appropriate layer within the PCB substrate 200 in order to provide connection with the semiconductor chip 400. Conductive material for example gold or copper is plated within the walls of the hole 502. A solder column 500 or solder ball is placed on the hole 502 in the PCB substrate 200. This solder column 500 or solder ball can be either 9OSn/10Pb or commonly used 63-Sn/37Pb. The size of the solder column 500 or solder column can range between 10 mils to 30 mils, and the pitch of the solder column 500 is between 40 and 50 mils. For solder column 500, the height of the solder column 500 is between 25 to 40 mils while the diameter of the solder column 500 is between 15 to 20 mils.

Turning now to Fig 5, wires 600 are bonded between the bond pads located at the center of the semiconductor chip 400 and the stitch pads located on the PCB substrate 200. The stitch pads are copper/nickel with gold plating. During an encapsulation process, liquid epoxy (Nb:Shinetsu-X-43-5000) are molding compound (Shinetsu-KMC188VA-4 or Dexter-MG65F) is used to house the PCB substrate 200, wire bondings and semiconductor chip 400 to form a sealing resin. However, this liquid epoxy is not placed on the back side of the silicon chip 400, leaving this back side exposed to the atmosphere to enhance the thermal conductivity and dissipation of heat of the semiconductor chip 400. Side sealing resin 800 forms the sides of the package while top sealing resin 700 covers the top of semiconductor chip 400 and PCB substrate 200.

Fig 6 illustrates a top view of the invention with a sealing resin 800 surrounding the PCB substrate 200.

Fig 7 illustrates a side view of the present invention, As illustrated in Fig 7, the width a of the semiconductor chip 400 is approximately 11 mils. The width c of the adhesive is approximately 1 mil. The width of the PBC is approximately 8 mils, which is comprised of two sections b and c which are 3 mils and 5 mils respectively. Section d extends from the bottom of the PCB substrate 400 to a position where the holes 502 extend to and section b which extends from the top of section d to the top of the PBC substrate 200.

CLAIMS

1. A package for an integrated circuit, comprising of a semiconductor chip; a printed circuit board for mounting the top side of said semiconductor chip; a encapsulation device for encapsulating the printed circuit board and the semiconductor chip, wherein semiconductor chip is exposed from encapsulation on at least one side.

2. A package for an integrated circuit, as in claim 1, wherein a backside of said semiconductor chip is exposed and free from encapsulation.

3. A package for an integrated circuit as in claim 1, wherein said package further comprises a layer of adhesive between said semiconductor chip and said printed circuit board.

4. A package for an integrated circuit as in claim 1, wherein said package further comprises solder column to electrical connect said

semiconductor chip.

5. A package for an integrated circuit as in claim 1, wherein said package further comprises solder balls to electrically connect said semiconductor chip.

6. A method for encapsulating a package for an integrated circuit, comprising the steps of: forming a semiconductor chip; forming a printed circuit board for mounting the top side of said semiconductor chip; encapsulating the printed circuit board and the semiconductor chip, wherein semiconductor chip is exposed from encapsulation on at least one side.

7. A method for encapsulating a package for an integrated circuit, as in claim 6, wherein a backside of said semiconductor chip is exposed and free from encapsulation.

8. A method for encapsulating a package for an integrated circuit as in claim 6, wherein said method further comprises the step of

forming a layer of adhesive between said semiconductor chip and said printed circuit board.

9. A method for encapsulating a package for an integrated circuit as in claim 6, wherein said method further comprises the step of forming a solder column to electrical connect said semiconductor chip.

10. A method for encapsulating a package for an integrated circuit as in claim 6, wherein said method further comprises the step of forming a solder ball to electrically connect said semiconductor chip.