WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a substrate;

an active pattern spaced apart from the substrate and extending in a first direction, wherein the active pattern includes:

a first side surface having a first height in a third direction perpendicular to the upper surface of the substrate; and

a second side surface opposite to the first side surface and having a second height in the third direction, the second height being different from the first height; and

a gate structure on the active pattern and extending in a second direction crossing the first direction,

wherein a lower portion of the active pattern extends in the first direction and includes a first lower surface that is sloped with respect to an upper surface of the substrate.

2. The semiconductor device according as claimed in claim 1, wherein the first lower surface is perpendicular to a [111] orientation of the active pattern.

3. The semiconductor device according as claimed in claim 1, wherein the first lower surface is a (111) surface.

4. The semiconductor device according as claimed in claim 1, wherein the upper surface of the substrate is a (100) surface.

5. The semiconductor device according as claimed in claim 1, wherein the lower portion of the active pattern further includes a second lower surface extending in the first direction, the second lower surface being substantially parallel to the upper surface of the substrate.

6. The semiconductor device according as claimed in claim 1, wherein the second height is less than the first height.

7. The semiconductor device according as claimed in claim 1, wherein the active pattern has a fin shape or a plate shape.

8. The semiconductor device according as claimed in claim 1, further comprising an interlayer insulating layer on the substrate, wherein the lower portion of the active pattern is buried in the interlayer insulating layer.

9. The semiconductor device according as claimed in claim 8, further comprising an isolation pattern between the substrate and the interlayer insulating layer, wherein the active pattern is spaced apart from the isolation pattern.

10. The semiconductor device according as claimed in claim 1, wherein the active pattern includes a different material from a material of the substrate.

11. A semiconductor device, comprising:

a substrate;

a pair of active patterns spaced apart from the substrate; and

a gate structure extending across the pair of active patterns,

wherein a lower portion of each active pattern of the pair of active patterns includes a lower surface sloped with respect to an upper surface of the substrate, the lower portion of each active pattern of the pair of active patterns extending in a direction crossing an extension direction of the gate structure.

12. The semiconductor device according as claimed in claim 11, wherein the pair of active patterns are in mirror symmetry relative to a plane orthogonal to the upper surface of the substrate and equidistant from each of the active patterns.

13. The semiconductor device according as claimed in claim 11, wherein each active pattern of the pair of active patterns includes:

a first side surface having a first length in a perpendicular direction relative to the upper surface of the substrate; and

a second side surface opposite to the first side surface and having a second length in the perpendicular direction, the second length being less than the first length.

14. The semiconductor device according as claimed in claim 13, wherein the first side surface of one active pattern of the pair of active patterns faces the first side surface of the other active pattern of the pair of active patterns.

15. The semiconductor device according as claimed in claim 11, further comprising an interlayer insulating layer on the substrate, wherein the lower portion of each active pattern of the pair of active patterns is buried in the interlayer insulating layer.

16. The semiconductor device according as claimed in claim 15, further comprising spaced isolation patterns between the substrate and the interlayer insulating layer, wherein each of the isolation patterns is located below a corresponding one of the pair of active patterns.

17. The semiconductor device according as claimed in claim 16, wherein:

the substrate includes a protrusion portion protruding between the isolation patterns, and

in plan view, the protrusion portion extends between and parallel to the pair of active patterns.

18. The semiconductor device according as claimed in claim 11, wherein:

the gate structure includes a gate insulating pattern and a gate electrode, and

the gate insulating pattern and the gate electrode extend between the substrate and the pair of active patterns.

19. The semiconductor device according as claimed in claim 11, wherein:

the upper surface of the substrate is a (100) surface, and

the lower surface of each active pattern of the pair of active patterns is a (111) surface.