Description

This invention relates to an apparatus for decoding digital signals, such as PCM signals, arranged in blocks, each having a predetermined number of data words.

To compress the volume of information to be transmitted, it has become customary to use different bit reduction processes, as e. g. differential processing or as companding. This is e. g. described in Japanese laid-open patent publications 223032/1984 or 103746/1985.

In the techniques described there, each block may be coded in one of a plurality of modes, e. g. different prediction filter processing modes or different bit compression ratio modes. At the reproducing side, the decoding processing is carried out blockwise in accordance with the mode at the transmitting side.

An example of an audio bit reduction system employing these techniques is now explained by referring to Fig. 1.

The system of Fig. 1 is made up of a transmitting or recording side encoder 10 and a receiving or reproducing side decoder 30. To an input terminal 11 of the encoder 10 are supplied PCM signals x(n) obtained by sampling analog audio signals by a frequency fs, followed by quantizing and encoding. These input signals x(n) are supplied to a prediction unit 12 and an adder 13 to produce a predicted error signal d(n). This signal is supplied through an adder 14 to a bit compression means consisting of a shifter 15 with a gain G and a quantizer 16 for outputting a coded signal to an output terminal 22. The encoder 10 further comprises a noise shaping circuit 17 having an adder 18, a shifter 19 and a prediction unit 20, and a prediction range adapted circuit 22, the latter one outputting range information at an output terminal 23. Mode selection information is output at an output terminal 24.

The decoder 30 receives the encoded data signals via an input terminal 33 and supplies them to an adder 33 through a shifter 32. A prediction unit 34 is connected in between the output and one input of the adder 33. The output signal of this adder is supplied to an output terminal 35 of the decoder 30. Gain information to be supplied to the shifter 32 is received via an input terminal 36, whereas mode information to be supplied to the prediction unit 34 is received via an input terminal 37.

Details of the encoder 10 and the decoder 30 are explained in the publication (EP-A-0234354) of the patent application associated to this patent. It is not necessary to know these details for understanding the present invention.

When decoding reproduced data words, the word length increases. It is therefore desirable to execute error correction or error interpolation before decoding the reproduced data words.

As such error interpolation, it is known to use a mean value interpolation using the mean value of data before and after an erroneous data word, a preceding value interpolation using data before the erroneous data word, or a succeeding value interpolation using data after the erroneous data word. It is customary to use the mean value interpolation.

However, there may arise problems in interpolation at the boundary between two adjacent blocks. This is illustrated by Fig. 2, in which Fig. 2A shows two succeeding blocks BL1 and BL2 before encoding, whereas Fig. 2B shows the same two blocks after encoding whereby the first block BL1 contains first order differential PCM data, whereas the second block BL2 contains straight PCM data. Due to the different PCM modes, a discontinuity is caused at the boundary between the two blocks. The decoded signal is the same as that of Fig. 2A. When interpolating an erroneous data word adjacent to the boundary between the two blocks, e. g. the first data word Da of the second block or the last data word Wb of the first block, an error may arise when using the encoded instead of the decoded data.

GB-A-2 082 025 describes an apparatus for decoding jitter signals which apparatus detects erroneous data words and interpolates the same based on data preceding and succeeding the erroneous word. The output of the interpolation circuit is fed to a juncture interpolation circuit which performs interpolation of data at the juncture between the blocks. This smoothes the interpolation error as it arises when substituting an erroneous data word at a boundary between two blocks by the mean value of the preceding and the succeeding word. However, it is a disadvantage of this apparatus that it always provides an interpolation at the boundary between two blocks due to the function of the juncture interpolation circuit.

US-A-3,071,727 describes an apparatus for decoding a digital signal which is encoded either in the differential or the straight PCM mode. This apparatus provides no error detection, but generally interpolates all data. When interpolating a data value at the boundary between data which were encoded in different PCM modes, the apparatus calculates the mean value of the last data encoded in one of the PCM modes, and the first data encoded in the other PCM mode. Thereby, an interpolation error arises as is discussed in relation with Fig. 2B.

It is the object of the present invention to provide an apparatus for decoding digital signals, which apparatus does not produce interpolation

errors when correcting an erroneous data word at the boundary between adjacent blocks being coded by different types of signal coding.

The apparatus of the present invention comprises:

- an error detecting means for detecting an erroneous data word within reproduced data words;
- an interpolation means for substituting an erroneous data word by an interpolated data word; and
- a decoding means for decoding the data as output by said interpolation means; and
- said interpolation means is arranged to detect the location of an erroneous word within a block and to substitute an erroneous data word by a value determined in dependence of the location of the erroneous data word within the block and determined solely on base of data words within said block.

Most preferably, an erroneous first data word in a block is substituted by the succeeding word, an erroneous last data word within a block is substituted by the preceding word, and an erroneous data word between the first and last data words within a block is substituted by a mean value calculated from at least one data word preceding the erroneous data word and at least one data word succeeding the erroneous data word.

The invention will now be explained by describing preferred embodiments illustrated through drawings.

Fig. 1 is a block circuit diagram showing a prior-art example of an audio bit rate reduction system.

Fig. 2A and 2B are waveform diagrams showing waveforms of encoder input signals of the same signals before and after encoding, respectively.

Fig. 3 is a block circuit diagram showing an embodiment of the present invention.

Fig. 4 is a timing chart for illustrating the interpolating operation of the embodiment of Fig. 3.

Fig. 5 is a block circuit diagram showing an essential part of a modified embodiment of the present invention.

Fig. 6 shows an example of the interleaving processing for the recording format.

Reference is now had to Fig. 3 illustrating an embodiment of the present invention as applied to the aforementioned audio bit rate reduction system.

In the decoder shown in Fig. 3, the parts or portions similar to those shown in Fig. 1 are indicated by the same reference numerals. Referring to this figure, to an input terminal 31, there are supplied signals from the output terminal 22 shown in Fig. 1, these signals being transmitted and supplied through a transmission medium or a recording medium after having been processed in such a manner that the mode and the range are switchingly selected blockwise as described above.

When transmitting these signals on the transmission medium or the recording medium, it is customary that these signals are converted by a multiplexer into serial data strings, word or block sync data are affixed to these serial data strings and the resulting signals are modulated by a modulating system proper to transmission. At a receiving or reproducing side, there are provided a demodulating circuit 70, a sync separating circuit 71 and an error correcting and detecting circuit 72 so that signals corresponding to the audio signal component are supplied to a terminal 31 and the range information signals are supplied to a terminal 36 while the mode selection information signals are supplied to a terminal 37.

In addition, an error flag from the error detecting circuit 72 is supplied to a terminal 38, while a word clock from a word clock generator 73 is applied to the terminal 39.

The input signal from the terminal 31 corresponding to the transmitted audio signal components in the block form are supplied through an input terminal 51 of an interpolating circuit 50 to a one-word delay circuit 52 and to a terminal b of a changeover switch 53. The output of a one-word delay circuit 52 is supplied to a terminal a of the changeover switch 53. The one-word delay circuit 52 and the changeover switch 53 take charge of the succeeding-value interpolation or holding, as later described in detail. The output from the changeover switch 53 is supplied to a terminal a of a changeover switch 54, the output of which is supplied through the one-word delay circuit 55 to the terminal b of the changeover switch 54. The changeover switch 54 and the one-word delay circuit 55 take charge of the previous value interpolation or holding or zero'th order interpolation, as also described later in detail. The output from the one-word delay circuit 55 is supplied to a terminal a of a changeover switch 56 and to a mean value circuit 57. The circuit 57 computes a value equal to 1/2 of the sum of the output data from the delay circuit 55 and the output data of the changeover switch 53, or the mean value, which is then supplied to a terminal b of the changeover switch 56. These changeover switches 54, 56, the delay circuit 55 and the mean value circuit 57 take charge of the mean value interpolation or first order interpolation of the error. The output from the changeover switch 56 is taken out at an output terminal 59 of the interpolating circuit 50 so as to be supplied to the shifter 32 of the decoder shown in Fig. 1. The structure and operation of the circuit downstream of the shifter 32 are similar to those of the decoder 30 shown in Fig. 1 so that the cor-

responding description is omitted for simplicity.

The changeover switches 53, 54 and 56 are switched by switching control signals S_1, S_2 and from an interpolating control circuit 60. As an example of the switching control operation, when there is no code error, the switches 53, 54 and 56 are all connected to the terminals a. When a code error is caused at the leading or first word of a block, the switch 53 is switched to the terminal b by the signal S_1 so that the error is interpolated by the next following value or by the second word in the block. When a code error is caused in the last word of a block, the switch 54 is switched to the terminal b by the signal S_2 so that the error is interpolated by the preceding value (previous value holding). When the code error is caused in some other positions, the switches 54, 56 are switched to the terminal b to make a mean value interpolation. For producing these switching control signals S_1, S_2 and S_3, timing pulses T_1, T_2 and T_3 are first produced in a timing pulse generator 61 for designating interpolation modes to be selected in dependence upon the word position in a block, and are used to gate control the error flag EF_0 supplied to the terminal 38 by using AND gates 66, 67 and 68. In view of the word delay caused in the delay circuits 52 and 55 in the interpolation circuit 50, it is necessary to set the timing of the pulses T_1, T_2 and T_3 or to delay the error flag EF. To this end, the error flag from the terminal 38 is sequentially delayed one word by two one-word delay circuits 62 and 63.

Reference is made to Fig. 4 for illustrating a more specific example of interpolating operation. In the present example, it is assumed that, for simplicity of illustration, the word number in one block is 8, the words are indicated as W_1, W_2, ..., W_8 from the first word in the block, and code errors are caused in the first, last and some other interiacent word, such as the fifth word.

That is, the input data A shown in Fig. 4 is supplied to the input terminal 51 shown in Fig. 3 and the words W_1', W_5' and W_8' of the eight words in one block are invalid data containing code errors. Hence, the error flag EF_0 supplied to the terminal 38 is "1" at the position of these words W_1', W_5' and W_8'. It is noted that the circled numerals 1 to 8 in Fig. 4 stand for the corresponding word numbers in the block at the signal input and output points and thus in disregard of the word number deviation caused by word delaying.

Since the input data A is delayed one word in the delay circuit 52, the error flag EF_0 is also delayed one word by a delay circuit 62 to produce an error flag EF_1 shown in Fig. 4 The timing pulse T_1 from the timing pulse generator 61 represents a signal that goes to "1" at the first word position of the signal thus delayed one word and that designates the word position for which the succeeding-value interpolation mode should be selected if the code error exists. An AND is taken of this error flag EF_1 and the timing pulse T_1 at the AND circuit 66 to produce the switching control Signal S_1 of the switch 53. This control signal S_1 goes to "1" at, for example, the second word position of the original undelayed input data A, that is, at the first word position after the one-word delay of the input data. When the control signal S_1 is "1", the switch 53 is switched to the terminal b. Hence, in the output B from the switch 53, the first word in the block or the error word W_1' is substituted by the second word W_2 so that the output is the suceeding-value interpolated output.

The timing pulse T_2 specifies the range of selection of the preceding-value hold and the mean value interpolation mode, and has a waveform which is an inversion of the timing pulse T_1, and thus goes to "1" at other than the first word in the block of the signal delayed by one word. The switching control signal S_2 of the switch 54 is obtained by taking an AND of this timing pulse T_2 and the error flag EF_1 at the AND circuit 67 and goes to "1" at the fifth and last or eighth words. When the switching control signal S_2 is "1", the switch 54 is switched to the terminal b so that the output from the delay circuit 55 is fed back to the delay circuit 55. Thus, the output C from the delay circuit 55 has its word numbers further delayed by one word and thus delayed by two words from the original input data A, while the output C produced when the control signal S_2 goes to "1" (words W_4 and W_7) is produced with one word delay for substituting the fifth and the eighth (or last) words in the two-word-delay signal.

In association with the delay caused by this delay circuit 55, the error flag EF_1 is delayed one word in a delay circuit 63 to produce an error flag EF_2 delayed by two words from the original input error flag EF_0. The timing pulse T_3 specifies the range of selection of the mean value interpolate mode for the two-word-delay signal. Thus, it goes to "1" at the second to seventh word positions excluding the first and last or eighth word positions. The switching control signal S_3 for the switch 56 is obtained by taking an AND of the error flag EF_2 and the timing pulse T_3 at the AND circuit 68. The control signal S_3 goes to "1" only at the fifth word position of the two-word-delay signal. At this time, the switch 56 is switched to the terminal b such that a mean value of the word W_6 of the output B from the switch 53 and the word W_4 of the output C from the delay circuit 55 or

$$\frac{W_4 + W_6}{2}$$

is taken from the mean value circuit 57 and supplied to an output terminal 59. Hence, the interpolated output from the switch 56 is delayed by two words with respect to the original input data A such that the word order in the block is W_2, W_2, W_3, W_4,

$$\frac{W_4 + W_6}{2},$$

W_6, W_7, W_7. In other words, the first word W_1' in the block where the code error has occurred is interpolated by the second word W_2 (succeeding value interpolate or hold), the last word W_8' is interpolated by the word W_7 one word before (previous value holding) and the interjacent fifth word W_5' is interpolated by the mean value of the preceding and the next following or succeeding words

$$\frac{W_4 + W_6}{2}$$

(mean value interpolation) such that the interpolation is realized only using the data in the block containing the word where the code error has occurred and thus without using data of any other blocks. This results in satisfactory interpolation since it becomes possible to prevent interpolation of error data by data of different or heterogeneous nature, such as predictive coding processing modes comprising differential or straight PCM modes or range data, that is, the bit compression rate data. In addition, it is only possible to make the interpolation for the data of a shorter word length before the decoding operation such as bit expansion by for example the shifter 32 so that the operation word length is reduced, thus resulting in correspondingly simplified circuit design and increased processing speed.

Reference is now made to Figs. 5 and 6 for explaining a modified embodiment of the present invention.

In will be noted that, in case of application of the present invention to, for example, a CD-ROM using an optical disk as the recording medium, it becomes necessary to perform an interleaving in conformity to the recording format. For example, in case of a decoding device in which the data of a four channel audio signal data are repeatedly applied word by word at the four-word periods, the interpolating circuit for the four channels may be provided in a parallel circuit configuration. However, it is also possible to make the interpolation within the block by a simpler arrangement using two four-word delay circuits 72 and 75, as shown in Fig. 5.

In the interpolating circuit 70 shown in Fig. 5, the parts similar to those shown in Fig. 3 are designated by the same reference numerals. The circuit structure is similar to that of Fig. 3 except that the delay circuit 72 and 75 perform the four-word delaying. Thus, the delay circuit 72 and the changeover switch 53 take charge of the succeeding value interpolation or holding in case the code error has occurred at the first word in the block of each channel. Similarly, the changeover switch 54 and the delay circuit 75 take charge of the preceding-value interpolation or holding in case the code error has occurred at the last word in the block in each channel, while the changeover switches 54, 56, the delay circuit 75 and the mean value circuit 57 take charge of the mean value interpolation in case the code error has occurred at the words other than the leading word and the last word in the block.

An example of the four-channel audio signals recorded on the aforementioned CD-ROM is shown in Fig. 6. The left and right channel sterophonic audio signals are separately sampled to produce two-channel data having a word length of for example 16 bits. These data are separately subjected to the aforementioned bit compression processing to produce the left-channel data strings L_1, L_2, L_3 .... and the right-channel data strings R_1, R_2, R_3, ..., each having the word length of, for example, eight bits. When the two-channel data string with each word consisting of eight bits is recorded on the recording medium such as an optical disk, the data are subjected to interleaving using, for example, a random access memory (RAM). Fig. 6 shows an example of such interleaving for a 28-row 4-column memory area. Thus, the left channel data strings L_1, L_2, ... and the right channel data strings R_1, R_2, ... are written in the first and the second rows in the regular order in the vertical direction as indicated by an arrow mark P, starting from the first row. After the words L_{28} and R_{28} are written in the 28th lines, the data strings L_{29}, L_{30}, ... and the data strings R_{29}, R_{30}, ... are sequentially written in the third and fourth rows, respectively. When the data are read from the memory, the data are read transversely in the sequence of the first column of the first row, the second column of the first row et seq., as indicated by an arrow mark Q, that is, in the order of the words L_1, R_1, L_{29}, R_{29}, L_2, R_2, L_{30}, R_{30}, ... so as to be recorded on the recording medium such as the optical disk. Thus, the reproduced data signals are temporarily continuous data with the four-word periods, such that it becomes necessary to perform the interleaving on the data strings having four-word periods.

The interpolating circuit of Fig. 5 may be advantageously employed for the interleaving of the signals having such recording format.

In the above described embodiments, the succeeding value interpolation, the previous value holding and the mean value interpolation are selected for the leading word, the last word and the interjacent word in the block. However, the present invention is not limited to these specific embodiments. For example, the succeeding value or previous value interpolation may be used in place of the mean value interpolation for the interjacent word positions, while it is also possible to effect the second or higher order interpolation.

Claims

1. An apparatus for decoding digital signals arranged into blocks, each having a predetermined number of data words, whereby the type of signal coding may vary from block to block, said apparatus comprising:
   - an error detecting means (72) for detecting an erroneous data word within reproduced data words;
   - an interpolation means (50) for substituting an erroneous data word by an interpolated data word; and
   - a decoding means (32, 33, 35) for decoding the data as output by said interpolation means;

   characterized in that said interpolation means (50) is arranged to detect the location of an erroneous word within a block and to substitute an erroneous data word by a value determined in dependence of the location of the erroneous data word within the block and determined solely on base of data words within said block.

2. An apparatus according to claim 1, **characterized in that** said interpolation means (50, 60) is arranged to substitute an erroneous first data word in a block by the succeeding word.

3. An apparatus according to one of the claims 1 and 2, **characterized in that** said interpolation means (50, 60) is arranged to substitute an erroneous last data word in a block by the preceding word.

4. An apparatus according to one of the claims 1 to 3, **characterized in that** the interpolation means (50, 60) is arranged to substitute an erroneous data word between the first and last words within a block by a mean value calculated from at least one data word preceding the erroneous data word and at least one data word succeeding the erroneous data word.

Patentansprüche

1. Gerät zum Dekodieren digitaler Signale, die in Blöcken angeordnet sind, von denen jeder eine vorgegebene Anzahl von Datenwörtern aufweist, wobei sich der Typ der Signalkodierung von Block zu Block ändern kann, welches Gerät folgendes aufweist:
   - eine Fehlerermittlungseinrichtung (72) zum Ermitteln eines fehlerhaften Datenworts innerhalb reproduzierter Datenwörter;
   - eine Interpoliereinrichtung (50) zum Ersetzen eines fehlerhaften Datenwortes durch ein interpoliertes Datenwort; und
   - eine Dekodiereinrichtung (32, 33, 35) zum Dekodieren der Daten, wie sie von der Interpoliereinrichtung ausgegeben werden;

   dadurch gekennzeichnet, daß die Interpoliereinrichtung (50) so ausgebildet ist, daß sie den Ort eines fehlerhaften Worts innerhalb eines Blocks ermittelt und ein fehlerhaftes Datenwort durch einen Wert ersetzt, der abhängig vom Ort des fehlerhaften Datenworts innerhalb des Blocks bestimmt wird, und dabei ausschließlich auf Grundlage der Datenwörter innerhalb dieses Blocks bestimmt wird.

2. Gerät nach Anspruch 1, **dadurch gekennzeichnet**, daß die Interpoliereinrichtung (50, 60) so ausgebildet ist, daß sie ein fehlerhaftes erstes Datenwort in einem Block durch das folgende Wort ersetzt.

3. Gerät nach einem der Ansprüche 1 oder 2, **dadurch gekennzeichnet**, daß die Interpoliereinrichtung (50, 60) so ausgebildet ist, daß sie ein fehlerhaftes letztes Datenwort in einem Block durch das vorangehende Wort ersetzt.

4. Gerät nach einem der Ansprüche 1 bis 3, **dadurch gekennzeichnet**, daß die Interpoliereinrichtung (50, 60) so ausgebildet ist, daß sie ein fehlerhaftes Datenwort zwischen dem ersten und dem letzten Wort innerhalb eines Blocks durch einen Mittelwert ersetzt, der mindestens aus einem Datenwort vor dem dem fehlerhaften Datenwort und mindestens einem Datenwort nach dem fehlerhaften Datenwort berechnet wird.

Revendications

1. Dispositif de décodage de signaux numériques agencés en blocs, chacun comportant un

The interpolating circuit of Fig. 5 may be advantageously employed for the interleaving of the signals having such recording format.

In the above described embodiments, the succeeding value interpolation, the previous value holding and the mean value interpolation are selected for the leading word, the last word and the interjacent word in the block. However, the present invention is not limited to these specific embodiments. For example, the succeeding value or previous value interpolation may be used in place of the mean value interpolation for the interjacent word positions, while it is also possible to effect the second or higher order interpolation.

Claims

1. An apparatus for decoding digital signals arranged into blocks, each having a predetermined number of data words, whereby the type of signal coding may vary from block to block, said apparatus comprising:
   - an error detecting means (72) for detecting an erroneous data word within reproduced data words;
   - an interpolation means (50) for substituting an erroneous data word by an interpolated data word; and
   - a decoding means (32, 33, 35) for decoding the data as output by said interpolation means;

   characterized in that said interpolation means (50) is arranged to detect the location of an erroneous word within a block and to substitute an erroneous data word by a value determined in dependence of the location of the erroneous data word within the block and determined solely on base of data words within said block.

2. An apparatus according to claim 1, **characterized in that** said interpolation means (50, 60) is arranged to substitute an erroneous first data word in a block by the succeeding word.

3. An apparatus according to one of the claims 1 and 2, **characterized in that** said interpolation means (50, 60) is arranged to substitute an erroneous last data word in a block by the preceding word.

4. An apparatus according to one of the claims 1 to 3, **characterized in that** the interpolation means (50, 60) is arranged to substitute an erroneous data word between the first and last words within a block by a mean value calculated from at least one data word preceding the erroneous data word and at least one data word succeeding the erroneous data word.

Patentansprüche

1. Gerät zum Dekodieren digitaler Signale, die in Blöcken angeordnet sind, von denen jeder eine vorgegebene Anzahl von Datenwörtern aufweist, wobei sich der Typ der Signalkodierung von Block zu Block ändern kann, welches Gerät folgendes aufweist:
   - eine Fehlerermittlungseinrichtung (72) zum Ermitteln eines fehlerhaften Datenworts innerhalb reproduzierter Datenwörter;
   - eine Interpoliereinrichtung (50) zum Ersetzen eines fehlerhaften Datenwortes durch ein interpoliertes Datenwort; und
   - eine Dekodiereinrichtung (32, 33, 35) zum Dekodieren der Daten, wie sie von der Interpoliereinrichtung ausgegeben werden;

   dadurch gekennzeichnet, daß die Interpoliereinrichtung (50) so ausgebildet ist, daß sie den Ort eines fehlerhaften Worts innerhalb eines Blocks ermittelt und ein fehlerhaftes Datenwort durch einen Wert ersetzt, der abhängig vom Ort des fehlerhaften Datenworts innerhalb des Blocks bestimmt wird, und dabei ausschließlich auf Grundlage der Datenwörter innerhalb dieses Blocks bestimmt wird.

2. Gerät nach Anspruch 1, **dadurch gekennzeichnet**, daß die Interpoliereinrichtung (50, 60) so ausgebildet ist, daß sie ein fehlerhaftes erstes Datenwort in einem Block durch das folgende Wort ersetzt.

3. Gerät nach einem der Ansprüche 1 oder 2, **dadurch gekennzeichnet**, daß die Interpoliereinrichtung (50, 60) so ausgebildet ist, daß sie ein fehlerhaftes letztes Datenwort in einem Block durch das vorangehende Wort ersetzt.

4. Gerät nach einem der Ansprüche 1 bis 3, **dadurch gekennzeichnet**, daß die Interpoliereinrichtung (50, 60) so ausgebildet ist, daß sie ein fehlerhaftes Datenwort zwischen dem ersten und dem letzten Wort innerhalb eines Blocks durch einen Mittelwert ersetzt, der mindestens aus einem Datenwort vor dem dem fehlerhaften Datenwort und mindestens einem Datenwort nach dem fehlerhaften Datenwort berechnet wird.

Revendications

1. Dispositif de décodage de signaux numériques agencés en blocs, chacun comportant un

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nombre prédéterminé de mots de données, dans lequel le type de codage de signal peut varier d'un bloc à un autre, ledit dispositif comprenant :

un moyen de détection d'erreur (72) pour détecter un mot de données erroné dans des mots de données reproduits ;

un moyen d'interpolation (50) pour substituer à un mot de données erroné un mot de données interpolé ; et

un moyen de décodage (32, 33, 35) pour décoder les données telles qu'émises en sortie par ledit moyen d'interpolation,

caractérisé en ce que ledit moyen d'interpolation (50) est agencé pour détecter l'emplacement d'un mot erroné dans un bloc et pour substituer à un mot de données erroné une valeur déterminée en fonction de l'emplacement du mot de données erroné dans le bloc et déterminée seulement sur la base de mots de données contenus dans ledit bloc.

2. Dispositif selon la revendication 1, caractérisé en ce que ledit moyen d'interpolation (50, 60) est agencé pour substituer à un premier mot de données erroné contenu dans un bloc le mot suivant.

3. Dispositif selon l'une des revendications 1 et 2, caractérisé en ce que ledit moyen d'interpolation (50, 60) est agencé pour substituer à un dernier mot de données erroné contenu dans un bloc le mot précédent.

4. Dispositif selon l'une des revendications 1 à 3, caractérisé en ce que le moyen d'interpolation (50, 60) est agencé pour substituer à un mot de données erroné situé entre les premier et dernier mots contenus dans un bloc une valeur moyenne calculée à partir d'au moins un mot de données précédant le mot de données erroné et d'au moins un mot de données suivant le mot de données erroné.

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