

ABSTRACT

According to an exemplary embodiment, a memory device may include a memory cell array that includes memory cells connected to word lines arranged in sequential order depending on a sequential change of a row address, a row decoder that, for each row address
5 input to the row decoder, scrambles a first bit of the row address and a second bit of the row address depending on a selection signal, thereby forming a scrambled row address, decodes the scrambled row address, and selects the a word line from the word lines based on the scrambled row address, and an anti-fuse array that includes an anti-fuse in which a logical value of the selection signal is programmed. A first word line and a second word line of the
10 word lines may be adjacent to each other, and a difference between a first value of the row address corresponding to the first word line and a second value of the row address corresponding to the second word line may be a value corresponding to the first bit.

FIG. 1