

## CLAIMS

1. A method for manufacturing a structure comprising a first substrate (1) comprising at least one electronic component (10) likely to be damaged by a temperature higher than 400 °C and a semi-conductor layer extending on said first substrate, characterised in that it comprises the following steps of:

(a) providing a first bonding metal layer (11) on the first substrate (1),

(b) providing a second substrate (2) comprising successively:

- a semi-conductor base substrate (20),

- a stack (21) of a plurality of semi-conductor epitaxial layers, a layer (210) of  $\text{Si}_x\text{Ge}_{1-x}$ , with  $0 \leq x \leq 1$  being located at the surface of said stack (21) opposite to the base substrate (20),

- a second bonding metal layer (22),

(c) bonding the first substrate and the second substrate through the first and second bonding metal layers (11, 22), said bonding step being carried out at a temperature lower than or equal to 400 °C,

(d) removing a part of the second substrate so as to transfer the layer (210) of  $\text{Si}_x\text{Ge}_{1-x}$  on the first substrate (1), said removing comprising at least selectively chemically etching a layer of the second substrate (2) relative to the  $\text{Si}_x\text{Ge}_{1-x}$  layer (210).

2. The method according to claim 1, wherein the second substrate (2) comprises a dielectric layer (23) between the layer (210) of  $\text{Si}_x\text{Ge}_{1-x}$  and the second bonding metal layer (22).

3. The method according to claim 2, wherein the thickness of the dielectric layer (23) is between 10 and 20 nm.

4. The method according to claim 1, wherein the base substrate (20) is a silicon substrate.

5. The method according to one of claims 1 and 2, wherein the stack (21) successively comprises, from the base substrate (20):

- a layer (213) of silicon-germanium having a composition gradually varying over its thickness,

- a layer (212) of silicon-germanium having a constant composition over its thickness,

- a layer (211) of  $\text{Si}_y\text{Ge}_{1-y}$ , with  $0 \leq y \leq 1$  and  $y$  different from  $x$ , said layer of  $\text{Si}_y\text{Ge}_{1-y}$  having a different composition from that of the layer (212) of silicon-germanium having a constant composition over its thickness so as to make up an etching barrier layer towards the layer (210) of  $\text{Si}_x\text{Ge}_{1-x}$ ,

5        - the layer (210) of  $\text{Si}_x\text{Ge}_{1-x}$ .

6.        The method according to claim 5, wherein:

10        - the composition of the layer (213) of silicon-germanium having a composition gradually varying over its thickness is  $\text{Si}_{0.8}\text{Ge}_{0.2}$  at the surface of said layer (213) opposite to the base substrate (20),

      - the composition of the layer (212) of silicon-germanium having a constant composition over its thickness is  $\text{Si}_{0.8}\text{Ge}_{0.2}$ , the thickness of said layer (212) being between  $0.5 \mu\text{m}$  and  $2 \mu\text{m}$ ,

15        - the composition of the etching barrier layer (211) is chosen from Si and  $\text{Si}_{0.6}\text{Ge}_{0.4}$ , the thickness of said layer (211) being between 10 nm and 50 nm,

      - the composition of the layer (210) of  $\text{Si}_x\text{Ge}_{1-x}$  is chosen from  $\text{Si}_{0.8}\text{Ge}_{0.2}$ , Si and Ge, the thickness of said layer (210) being between 5 and 50 nm.

20        7.        The method according to one of claims 1 to 6, wherein the first and second bonding metal layers comprise titanium, nickel, copper and/or tungsten.

8.        The method according to one of claims 1 to 7, wherein step (b) comprises the following successive steps of:

25        - epitaxially growing a layer (213) of silicon-germanium with a gradual composition,

      - epitaxially growing a layer (212) of silicon-germanium with a constant composition,

      - polishing the layer (212) of silicon-germanium with a constant composition,

30        - epitaxially growing a layer (211) of  $\text{Si}_y\text{Ge}_{1-y}$ , with  $0 \leq y \leq 1$  and  $y$  different from  $x$  on the polished layer (212) of silicon-germanium, said layer (211) of  $\text{Si}_y\text{Ge}_{1-y}$  having a different composition from that of the layer (212) of silicon-germanium having a constant composition over its thickness,

      - epitaxially growing the layer (210) of  $\text{Si}_x\text{Ge}_{1-x}$  on the layer (211) of  $\text{Si}_y\text{Ge}_{1-y}$ ,

      - depositing the second bonding metal layer (22).

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9. The method according to claim 8, wherein step (b) comprises, between the step of epitaxially growing the layer (210) of  $\text{Si}_x\text{Ge}_{1-x}$  and the step of depositing the second bonding metal layer (22), a step of depositing a dielectric layer (23).

5 10. The method according to claim 9, wherein step (b) comprises, after the step of depositing the dielectric layer (23), a densification annealing of said layer.

10 11. The method according to one of claims 9 and 10, wherein step (b) further comprises forming, between the dielectric layer (23) and the second bonding metal layer (22), a layer (24) of a binary or ternary metal alloy.

15 12. The method according to one of claims 1 to 11, wherein step (d) comprises withdrawing a part of the thickness of the base substrate (20) by polishing, followed by selectively etching the rest of said base substrate (20).

13. The method according to claim 12, wherein etching the base substrate (20) is made with a TMAH, KOH, and/or  $\text{HF:HNO}_3$  solution.

20 14. The method according to one of claims 12 and 13, wherein removing the base substrate (20) is followed by selectively etching the layers (213, 212) of silicon-germanium with a constant composition and a gradual composition by means of a SC1 solution and/or a  $\text{HF:H}_2\text{O}_2:\text{CH}_3\text{COOH}$  solution.

25 15. A method for manufacturing a tridimensional monolithic integrated circuit, characterised in that it comprises:

- manufacturing a structure comprising a first substrate (1) comprising at least one electronic component (10) likely to be damaged by a temperature higher than 400 °C and a layer (210) of  $\text{Si}_x\text{Ge}_{1-x}$  extending on said first substrate by means of a method according to one of claims 1 to 14,

30 - manufacturing at least one other electronic component in or on the layer (210) of  $\text{Si}_x\text{Ge}_{1-x}$ ,

said method being further characterised in that all the steps implemented on said structure are made at a temperature lower than or equal to 400 °C.

35 16. A structure comprising a first substrate (1) comprising at least one electronic component (10) likely to be damaged by a temperature higher than 400 °C and a semi-conductor layer (210) extending on said first substrate, characterised in that said

semi-conductor layer (210) is a layer of  $\text{Si}_x\text{Ge}_{1-x}$ , with  $0 \leq x \leq 1$  and in that said structure comprises successively, from said first substrate (1) to said semi-conductor layer (210):

- a metal layer (11, 22);
- a layer (24) of a binary or ternary metal alloy;
- a dielectric layer (23).

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17. The structure according to claim 16, wherein said at least one electronic component (10) comprises a transistor, a memory, a photodetector, a diode, a laser, a switch, an amplifier and/or a filter.

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