

Description

Technical field

The present invention relates to an improvement of a multiplex system used in a hierarchical data transmission system in which a plurality of signals output by multiplexers are further multiplexed and transmitted to a transmission line, especially an optical transmission line.

Background art

A hierarchical transmission system is known in which, for example, 9-channel data trains, each having a transmission rate of 45 Mb/s, are multiplexed by low group multiplexers to obtain a multiplexed data train of 405 Mb/s and, for example, two of these multiplexed data trains are further multiplexed by a high group multiplexer to obtain a multiplexed data train of 810 Mb/s, and this high group multiplexed data train is electro-optic converted by an optical interface circuit and transmitted to an optical transmission line, whereby a large amount of data transmission is performed. In this system, the output signals of the low group multiplexers are scrambled at the highest speed now possible, whereby the ratio of "1" and "0" of the output signal becomes almost equal.

In such a system, when one of the low group multiplexers becomes unavailable through a fault occurrence, the unavailable multiplexer outputs "0" or "1" continuously. Accordingly, the ratio of "0" and "1" of the output signal does not become equal.

However, when the unavailable low group multiplexer outputs, for example, "0" continuously, if the transmission rate of the system is very high and the number of low group multiplexers is small, for example, two, it is difficult to extract a timing clock from a received signal in the receiver side, therefore normal reception becomes impossible. On the other hand, when the unavailable low group multiplexer outputs "1" continuously, if this system is used in the optical transmission system, the lighting time of a light emission element, for example, a semiconductor laser, becomes long in comparison with the case in which a fault does not occur, and accordingly, the life time of the light emission element is shortened.

From EP-A-0117544 a multiplexing system is known in which, on the sender side, parallel signals are input to a plurality of first multiplexers and converted into a plurality of multiplexed signals, these signals being then input to a second multiplexer for further multiplexing. This known system uses a supervisory or frame synchronization signal which is input to the second multiplexer. On the receiver side first and second demultiplexers are used to demultiplex the signals. The frame synchronization signal is extracted by the first demultiplexer.

FR-A-2295650 describes a PCM system in which a supervisory signal is inserted into a PCM signal prior to transmission. On the receiving side

the supervisory signal is extracted and a scramble signal is output to show the effect of an obstacle.

Accordingly, an object of the present invention is to provide an improved multiplex system which can facilitate the extraction of the timing clock at the receiver side and prolong the life time of the light emission element at the transmitter side.

The object of the present invention is solved by a multiplex system comprising a plurality of first multiplexers having outputs supplying data signals; a second multiplexer for multiplexing a parallel input signal by simply converting the parallel input signal to a serial output signal; a pattern generator for generating an alternating pattern signal in synchronization with the signals output by the said first multiplexers; and a plurality of selectors, each operatively connected to said pattern generator, said second multiplexer and the output of a corresponding one of said first multiplexers, for selecting the data signal output by the corresponding first multiplexer when the corresponding first multiplexer assumes a normal state and selecting the alternating pattern signal when the corresponding first multiplexer assumes a fault state and for outputting the selected signals selected thereby to said second multiplexer as the parallel input signal.

Brief description of the drawings

Embodiments of a multiplex system according to the present invention will be described with reference to the accompanying drawings, in which:

Fig. 1 is a block diagram of a prior art multiplex system;

Fig. 2 is a block diagram of an embodiment of a multiplex system according to the present invention;

Fig. 3 and Fig. 4 show time charts of signal-waveforms for explaining the operation of the system shown in Fig. 2;

Fig. 5 is a block diagram of another embodiment according to the present invention;

Fig. 6 is a time chart of the signal-waveform of the Fig. 5 system; and

Fig. 7 and Fig. 8 are block diagrams of further embodiments according to the present invention.

Best mode for carrying out the invention

Before describing the embodiments of the present invention, a prior art and the disadvantages therein will be described. Figure 1 is a block diagram of a multiplex system of the prior art. In Fig. 1, 11 to 1n are n number of low group digital multiplexers, 2 a high group multiplexer. The multiplexer 2 comprises AND gates 211 to 21n, an OR gate 22, and a flip-flop 23. Each of AND gates 211 to 21n has two input terminals, to one of which a data signal output by the related multiplexer is led and to the other a clock having an n multiplied clock rate of the timing clock of multiplexers 11 to 1n, i.e. n phase clock of multiplexers 11 to 1n. Output signals of the AND gates 211 to 21n are led to the flip-flop 23 for shaping the waveform.

In the Fig. 1 system, a further multiplex of the output signal of multiplexers 211 to 21n is performed by opening AND gates 211 to 21n in sequence to send these data signals of the multiplexers 211 to 21n in sequence to the flip-flop 23 to shape the waveform.

However, in the Fig. 1 system, if one of multiplexers 11 to 1n becomes unavailable due to a fault, that unavailable multiplexer outputs "0" or "1" sequentially, as a result, the ratio of "0" and "1" of the signal output by the multiplexer 2 does not become equal. Therefore, extraction of the timing clock at the receiver side becomes difficult and the life time of the light emission element at the transmitter side is shortened.

Figure 2 illustrates an embodiment of a multiplex system according to the present invention. In Fig. 2, 11 to 1n are n units of digital low group multiplexers, 2 a high group multiplexer, 31 to 3n n units of selector, 4 a divide-by-2 frequency divider as a pattern generator, and 51 to 5n D type flip-flops for shaping the waveform. In later figures, the same references represent the same components.

The multiplexers 11 to 1n output a multiplexed data train of a low group as an output signal respectively. These multiplexed data trains are scrambled by each of the multiplexers respectively, therefore, the ratio of "0" and "1" of the output signal in a normal state becomes almost 1:1. When these multiplexers 11 to 1n become unavailable due to a fault, these multiplexers 11 to 1n output "0" continuously. These multiplexers 11 to 1n are provided with a fault detector which detects the fault and outputs an output cut-off detecting signal at a continuous "1" level. Of course, this fault detector may be equipped outside of the multiplexers 11 to 1n.

Selectors 31 to 3n are provided for each of the multiplexers 11 to 1n respectively, and comprises AND gates 311 to 31n and OR gates 321 to 32n respectively. In selectors 31 to 3n, the AND gates 311 to 31n have two input terminals. The detecting signals SD1 to SDn from multiplexers 11 to 1n are respectively led to one of the input terminals of the AND gates 311 to 31n, and the alternating pattern signal from the frequency divider 4 is input to the other input terminal thereof. Also, OR gates 321 to 32n have two input terminals, and the data signals output by the multiplexers 11 to 1n are respectively led to one of the input terminals and output signals of the AND gates 311 to 31n are respectively led to the other terminal thereof.

These selectors 31 to 31n select the data signals output by multiplexers 11 to 1n when the detecting signals SD1 to SDn are "0" respectively, select the alternating pattern signal from the frequency halver 4 when the detecting signals are "1" respectively, and supply the selected signals to the multiplexer 2 via flip-flops 51 to 5n respectively.

The divide-by-2 frequency divider 4 divides the timing clock of the multiplexer by 2 in frequency, thereby outputting the alternating patterns signal

which alternates "0" and "1" in a 1/2 frequency of the timing clock. The flip-flops 51 to 5n are operated by the timing clock of the multiplexers 11 to 1n to shape the waveform of the input signal.

The multiplexer 2 is the same as that shown in Fig. 1. The output signal of the multiplexer 2 is supplied to the optical interface circuit (not shown) which includes a light emission element such as the semiconductor laser, and then transmit it to the optical transmission line.

The mode of operation of the system shown in Fig. 2 will now be described by referring to Fig. 3 and Fig. 4. In the normal state, multiplexers 11 to 1n output a data signal, and the output cut-off detecting signals SD1 to SDn are "0". Accordingly, selectors 31 to 3n select the data signals from the multiplexers 11 to 1n, and supply them to the multiplexer 2 via the flip-flop 51 to 5n. In this case, as shown in Fig. 3(a) and Fig. 4(a), the output signal of the multiplexer 2 repeats the data signals from the multiplexers 11 to 1n in sequence. Figure 3 shows the time chart of the signal output by the multiplexer 2 when the number n of the multiplexers 11 to 1n is 2, and Fig. 4 shows the same when the number n is 4. The ratios of "0" and "1" of the signals output by the multiplexers 11 to 1n are 1:1, since these signals are scrambled.

Now if, for example, the multiplexer 11 becomes unavailable due to a fault, the signal data output by the multiplexer 11 becomes "0" and at the same time the detecting signal SD1 becomes "1". Therefore, the selector 31 selects the alternating pattern signal of the frequency halver 4 instead of the output signal of the multiplexer 11 and supplies it to the multiplexer 2 via the flip-flop 51.

As a result, as shown in Fig. 3(b) and Fig. 4(b), the data portion of the multiplexer 11 in the output signal of the multiplexer 2 alternates "0" and "1" in sequence, and therefore the ratio of "0" and "1" of the signal output by the multiplexer 2 becomes almost 1:1 in spite of the fault at the multiplexer 11. Accordingly, the extraction of the timing clock at the receiver side becomes easy, and if this system is used in the optical data transmission system, the life time of the light emission element becomes longer in comparison with the case where a continuous "1" is output from the unavailable multiplexer 1.

Figure 5 illustrates another embodiment of the multiplex system according to the present invention. In the system shown in Fig. 5, the selection functions of the selectors, the alternating pattern generating function of the frequency halver, and the waveform shaping function of the flip-flop in the Fig. 2 system are realized by one circuit, i.e., a signal supplying circuit, thereby reducing the number of components and adapting for a high transmission rate. In Fig. 5, the system comprises multiplexers 11 to 1n, signal supplying circuits 61 to 6n provided for each of the multiplexers 11 to 1n, and the multiplexers 2. The multiplexers 11 to 1n and multiplexer 2 have the same function as

those of Fig. 2 except that the output cut-off detecting signals SD1 to SDn from the multiplexers 11 to 1n are "1" level in the normal state and "0" level in the fault state.

Signal supplying circuits 61 to 6n comprise OR gates 61 to 6n, NOR gates 621 to 62n, and flip-flops 631 to 63n respectively. Data signals output by the multiplexers 11 to 1n are led to one of the input terminals of the OR gates 611 to 61n respectively. Output signals of the OR gates 611 to 61n are led to data input terminals of the flip-flops 631 to 63n respectively. Output signals Q of the flip-flop 631 to 63n are led to the multiplexer 2 at the same time to one of the input terminals of the NOR gates 621 to 62n respectively. The detecting signals SD1 to SDn are led to the other input terminals of the NOR gates 621 to 62n respectively. Output signals of the NOR gates 621 to 62n are led to the other input terminals of the OR gates 611 to 61n respectively. The timing clock of the multiplexers 11 to 1n is led to the clock input terminals of the flip-flops 631 to 63n.

The operation of the system shown in Fig. 5 will be described hereinafter. As an example, the operation of the signal supplying circuit 61 will be described. Figure 6 is a time chart of the signal waveforms of the circuit 61. In Fig. 6, (a) represents the data output signal from the multiplexer 11, (b) a low group timing clock, (c) an output cut-off detecting signal SD1 from the multiplexer 11, (d) an output signal of the flip-flop 631, (e) an output signal of the OR gate 611, and (f) an output signal of the NOR gate 621.

In the normal state, the NOR gate 621 is closed, since the output cut-off detecting signal SD1 is "1". Therefore, the data signal output by the multiplexer 11 is input to the flip-flop 631 via the OR gate 611. The flip-flop 631 shapes the waveform of the data output signal and then sends it to the multiplexer 2.

On the other hand, when the multiplexer 11 becomes unavailable due to a fault at time t1, the data output signal thereof is cut-off, i.e., becomes "0" continuously, and at the same time, the detecting signal SD1 changes from "1" to "0", whereby the NOR gate 621 is opened. Therefore, the output signal Q of the flip-flop 631 is reversed by the NOR gate 621 and fed back to the data input terminal D of the flip-flop 631 via the OR gate 611. As a result, the flip-flop 631 operates as a divide-by-2 frequency divider, i.e., a binary counter, and outputs an alternating signal, obtained by dividing in frequency the timing clock by 2, to the multiplexer 2 instead of the data signal output by the multiplexer 11.

Accordingly, the output signal of the signal supplying circuit 61 has the ratio of "0" and "1" of almost 1:1. Using this signal supplying circuit, a single flip-flop is commonly used as the flip-flop for frequency dividing and the flip-flop for waveform shaping, whereby the number of the components is reduced in comparison with the Fig. 2 system, and the system may be adapted for the high rate transmission system.

Figure 7 illustrates another embodiment of the

signal supplying circuit according to the present invention. In Fig. 7, an inverted output signal $\bar{Q}$ of a flip-flop 73 is fed back to a data input terminal thereof via an AND gate 72 and OR gate 71. The output cut-off detecting signal SD is led to an inverting input terminal of the AND gate 72. This signal supplying circuit also outputs the alternating pattern signal instead of the data signal from the low group multiplexer when the detecting signal SD becomes "0".

Figure 8 illustrates another embodiment of the multiplex system according to the present invention in which the signal supplying circuit of Fig. 6 is utilized as the alternating pattern generator. In Fig. 8 8 is an AND gate, 6 the signal supplying circuit, and 91 and 92 selectors. As shown in Fig. 8, the output cut-off detecting signals SD1 and SD2 are led to the AND gate 8 to obtain the logical product thereof, and the output signal of the AND gate 8 is led to the input terminals of OR gate 61 and NOR gate 62. This signal supplying circuit outputs the alternating signal to the selectors 91 and 92 when at least one of the detecting signals SD1 and SD2 become "0".

Although preferred embodiments have been described, various modifications and alterations are possible within the scope of the present invention.

Capability of exploitation in industry

As can be seen from the above description, a multiplex system according to the present invention can be used in a hierarchical data transmission system in which a plurality of signals output by multiplexers are further multiplexed and transmitted to a transmission line, especially an optical transmission line.

Claims

1. A multiplex system including:

a plurality of first multiplexers (11, 12, 1n) in having outputs supplying data signals; and a second multiplexer (2) for multiplexing a parallel input signal by simply converting the parallel input signal to a serial output signal; characterized by:

a pattern generator (4, 6) for generating an alternating pattern signal in synchronization with the signals output by said first multiplexers (11, 12 ... 1n); and

a plurality of selectors (31, 32 ... 3n; 61, 62 ... 6n; (91, 92 ... 9n)) each operatively connected to said pattern generator (4, 6) said second multiplexer (2) and the output of a corresponding one of said first multiplexers (11, 12 ... 1n), for selecting the data signal output by the corresponding first multiplexer (11, 12 ... 1n) when the corresponding first multiplexer (11, 12 ... 1n) assumes a normal state and selecting the alternating pattern signal when the corresponding first multiplexer (11, 12 ... 1n) assumes a fault state and for outputting signals selected thereby to said second multiplexer (2) as the parallel input signal.

those of Fig. 2 except that the output cut-off detecting signals SD1 to SDn from the multiplexers 11 to 1n are "1" level in the normal state and "0" level in the fault state.

Signal supplying circuits 61 to 6n comprise OR gates 61 to 6n, NOR gates 621 to 62n, and flip-flops 631 to 63n respectively. Data signals output by the multiplexers 11 to 1n are led to one of the input terminals of the OR gates 611 to 61n respectively. Output signals of the OR gates 611 to 61n are led to data input terminals of the flip-flops 631 to 63n respectively. Output signals Q of the flip-flop 631 to 63n are led to the multiplexer 2 at the same time to one of the input terminals of the NOR gates 621 to 62n respectively. The detecting signals SD1 to SDn are led to the other input terminals of the NOR gates 621 to 62n respectively. Output signals of the NOR gates 621 to 62n are led to the other input terminals of the OR gates 611 to 61n respectively. The timing clock of the multiplexers 11 to 1n is led to the clock input terminals of the flip-flops 631 to 63n.

The operation of the system shown in Fig. 5 will be described hereinafter. As an example, the operation of the signal supplying circuit 61 will be described. Figure 6 is a time chart of the signal waveforms of the circuit 61. In Fig. 6, (a) represents the data output signal from the multiplexer 11, (b) a low group timing clock, (c) an output cut-off detecting signal SD1 from the multiplexer 11, (d) an output signal of the flip-flop 631, (e) an output signal of the OR gate 611, and (f) an output signal of the NOR gate 621.

In the normal state, the NOR gate 621 is closed, since the output cut-off detecting signal SD1 is "1". Therefore, the data signal output by the multiplexer 11 is input to the flip-flop 631 via the OR gate 611. The flip-flop 631 shapes the waveform of the data output signal and then sends it to the multiplexer 2.

On the other hand, when the multiplexer 11 becomes unavailable due to a fault at time t1, the data output signal thereof is cut-off, i.e., becomes "0" continuously, and at the same time, the detecting signal SD1 changes from "1" to "0", whereby the NOR gate 621 is opened. Therefore, the output signal Q of the flip-flop 631 is reversed by the NOR gate 621 and fed back to the data input terminal D of the flip-flop 631 via the OR gate 611. As a result, the flip-flop 631 operates as a divide-by-2 frequency divider, i.e., a binary counter, and outputs an alternating signal, obtained by dividing in frequency the timing clock by 2, to the multiplexer 2 instead of the data signal output by the multiplexer 11.

Accordingly, the output signal of the signal supplying circuit 61 has the ratio of "0" and "1" of almost 1:1. Using this signal supplying circuit, a single flip-flop is commonly used as the flip-flop for frequency dividing and the flip-flop for waveform shaping, whereby the number of the components is reduced in comparison with the Fig. 2 system, and the system may be adapted for the high rate transmission system.

Figure 7 illustrates another embodiment of the

signal supplying circuit according to the present invention. In Fig. 7, an inverted output signal $\bar{Q}$ of a flip-flop 73 is fed back to a data input terminal thereof via an AND gate 72 and OR gate 71. The output cut-off detecting signal SD is led to an inverting input terminal of the AND gate 72. This signal supplying circuit also outputs the alternating pattern signal instead of the data signal from the low group multiplexer when the detecting signal SD becomes "0".

Figure 8 illustrates another embodiment of the multiplex system according to the present invention in which the signal supplying circuit of Fig. 6 is utilized as the alternating pattern generator. In Fig. 8, 8 is an AND gate, 6 the signal supplying circuit, and 91 and 92 selectors. As shown in Fig. 8, the output cut-off detecting signals SD1 and SD2 are led to the AND gate 8 to obtain the logical product thereof, and the output signal of the AND gate 8 is led to the input terminals of OR gate 61 and NOR gate 62. This signal supplying circuit outputs the alternating signal to the selectors 91 and 92 when at least one of the detecting signals SD1 and SD2 become "0".

Although preferred embodiments have been described, various modifications and alterations are possible within the scope of the present invention.

Capability of exploitation in industry

As can be seen from the above description, a multiplex system according to the present invention can be used in a hierarchical data transmission system in which a plurality of signals output by multiplexers are further multiplexed and transmitted to a transmission line, especially an optical transmission line.

Claims

1. A multiplex system including:

a plurality of first multiplexers (11, 12, 1n) in having outputs supplying data signals; and
a second multiplexer (2) for multiplexing a parallel input signal by simply converting the parallel input signal to a serial output signal; characterized by:

a pattern generator (4, 6) for generating an alternating pattern signal in synchronization with the signals output by said first multiplexers (11, 12 ... 1n); and

a plurality of selectors (31, 32 ... 3n; 61, 62 ... 6n; (91, 92 ... 9n)) each operatively connected to said pattern generator (4, 6) said second multiplexer (2) and the output of a corresponding one of said first multiplexers (11, 12 ... 1n), for selecting the data signal output by the corresponding first multiplexer (11, 12 ... 1n) when the corresponding first multiplexer (11, 12 ... 1n) assumes a normal state and selecting the alternating pattern signal when the corresponding first multiplexer (11, 12 ... 1n) assumes a fault state and for outputting signals selected thereby to said second multiplexer (2) as the parallel input signal.



2. A multiplex system according to claim 1, wherein a timing clock signal controls said first multiplexers (11, 12 ... 1n), and wherein said pattern generator (4, 6) comprises a frequency demultiplier (4) for dividing the timing clock signal of said first multiplexers (11, 12 ... 1n) by two.

3. A multiplex system according to claim 1, wherein each of said first multiplexers (11, 12 ... 1n) further outputs a fault indicating signal when in the fault state, and wherein each of the selectors (31, 32 ... 3n) comprises:

an AND gate (311 to 31n) having two input terminals and supplying an output signal at an output terminal, the alternating pattern signal from said pattern generator (4) being supplied to one of the input terminals and the fault indicating signal of the corresponding first multiplexer (11, 12 ... 1n) being input to the other of the input terminals; and

an OR gate (321 to 32n) having two input terminals and an output terminal operatively connected to said second multiplexer (2), the output signal from said AND gate (311 to 31n) being input to one of the input terminals and the data signal from the corresponding first multiplexer (11, 12 ... 1n) being input to the other of the input terminals.

4. A multiplex system according to claim 1, wherein each of the signals output by the selectors (31 to 3n) is input to the second multiplexer (2) via a D-type flip-flop (51 to 5n) for waveform shaping.

5. A multiplex system according to claim 1, wherein each of the selectors (61 to 6n) include a D-type flip-flop (631 to 63n) operated by a timing clock of the first multiplexers (11, 12 ... 1n) and constituted so that the signal output by the corresponding first multiplexer (11, 12 ... 1n) is wave-shaped by the D-type flip-flop (631 to 63n) and supplied to the second multiplexer (2) when the corresponding first multiplexer (11, 12 ... 1n) assumes a normal state, and said pattern generator generates an alternating pattern signal having 1/2 timing clock rate of the first multiplexers (11, 12, ... 1n) by leading the polarity-reversed output signal of the D-type flip-flop (631 to 63n) to a data input terminal thereof said alternating pattern signal being supplied to the second multiplexer (2) when the corresponding first multiplexer (11, 12 ... 1n) is in a fault state.

6. A multiplex system according to claim 5, wherein each selector (61 to 6n) further comprises:

a NOR gate (621 to 62n) having two input terminals, the output signal of the D-type flip-flop (631 to 63n) being input to one terminal and the fault indicating signal of the corresponding first multiplexer (11, 12 ... 1n) being input to the other; and

an OR gate (611 to 61n) having two input terminals, the output signal of the corresponding first multiplexer (11, 12 ... 1n) being input to one terminal and the output signal of the NOR gate

(621 to 62n) being input to the other, and supplying the output signal thereof to the data input terminal of the D-type flip-flop (631 to 63n).

7. A multiplex system according to claim 3, wherein said pattern generator comprises:

an AND gate (8) having a plurality of input terminals, the fault indicating signals from each first multiplexer (11, 12 ... 1n) being input to a corresponding input terminal of said AND gate (8);

a D-type flip-flop (63) for supplying the alternating pattern signal as an output signal to said selectors (91, 92 ... 9n);

a NOR gate (62) having two input terminals, the output signal of the D-type flip-flop (63) being input to one terminal and the output signal from said AND gate (8) being input to the other; and

an OR gate (61) having two input terminals, the output signal of the NOR gate (62) being input to one terminal and the output signal from said AND gate (8) being input to the other, and supplying the output signal thereof to the data input terminal of the D-type flip-flop (63).

Patentansprüche

1. Multiplexsystem mit einer

—Vielzahl von ersten Multiplexern (11, 12, 1n) mit Datensignale liefernden Ausgängen; und

—einem zweiten Multiplexer (2) zum Multiplexen eines parallelen Eingangssignals durch einfaches Umwandeln des parallelen Eingangssignals in ein Serienaussgangssignal; gekennzeichnet durch

—einen Mustergenerator (4, 6) zum Erzeugen eines alternierenden Mustersignals in Synchronisation mit den durch die ersten Multiplexer (11, 12 ... 1n) ausgegebenen Signalen; und

—eine Vielzahl von Selektoren (31, 32 ... 3n; 61, 62 ... 6n; 91, 92 ... 9n), die jeweils mit dem Mustergenerator (4, 6) und dem zweiten Multiplexer (2) und dem Ausgang eines entsprechenden der ersten Multiplexer (11, 12 ... 1n) betriebsmäßig verbunden sind, zum Auswählen des Datensignals, das durch den entsprechenden ersten Multiplexer (11, 12 ... 1n) ausgegeben wird, wenn der entsprechende erste Multiplexer (11, 12 ... 1n) einen normalen Zustand annimmt, und zum Auswählen des alternierenden Mustersignals, wenn der entsprechende erste Multiplexer (11, 12 ... 1n) einen Fehlerzustand annimmt, und zum Ausgeben von dadurch ausgewählten Signalen an den zweiten Multiplexer (2) als das parallele Eingangssignal.

2. Multiplexsystem nach Anspruch 1, dadurch gekennzeichnet, daß ein Taktgebersignal die ersten Multiplexer (11, 12 ... 1n) steuert, und daß der Mustergenerator (4, 6) einen Frequenzdemultiplizierer (4) zum Teilen des Taktgebersignals der ersten Multiplexer (11, 12 ... 1n) durch zwei enthält.

3. Multiplexsystem nach Anspruch 1, dadurch gekennzeichnet, daß jede der ersten Multiplexer (11, 12 ... 1n) weiter ein einen Fehler andeutendes Signal bei einem Fehlerzustand ausgibt und daß



jeder der Selektoren (31, 32 ... 3n) folgendes enthält:

—ein UND-Gate (311 bis 31n) mit zwei Eingangsanschlüssen und zum Ausgeben eines Ausgangssignals an einem Ausgangsanschluß, wobei das alternierende Mustersignal von dem Mustergenerator (4) an einem der Eingangsanschlüsse abgegeben wird und das Fehler andeutende Signal des entsprechenden ersten Multiplexers (11, 12 ... 1n) an dem anderen der Eingangsanschlüsse eingegeben wird; und

—ein ODER-Gate (321 bis 32n) mit zwei Eingangsanschlüssen und einem mit dem zweiten Multiplexer (2) betriebsmäßig verbundenen Ausgangsanschluß, wobei das Ausgangssignal von dem UND-Gate (311 bis 31n) an einem der Eingangsanschlüsse eingegeben wird und das Datensignal von den entsprechenden ersten Multiplexern (11, 12 ... 1n) an dem anderen der Eingangsanschlüsse eingegeben wird.

4. Multiplexsystem nach Anspruch 1, dadurch gekennzeichnet, daß jedes der von den Selektoren (31 bis 3n) ausgegebenen Signale an dem zweiten Multiplexer (2) über eine Kippschaltung (51 bis 5n) des D-Typs zum Wellenformumwandeln eingegeben wird.

5. Multiplexsystem nach Anspruch 1, dadurch gekennzeichnet, daß jeder der Selektoren (61 bis 6n) eine durch einen Taktgeber der ersten Multiplexer (11, 12 ... 1n) betriebene Kippschaltung (631 bis 63n) eines D-Typs enthält und derart ausgebildet ist, daß das von dem entsprechenden ersten Multiplexer (11, 12 ... 1n) ausgegebene Signal durch die Kippschaltung (631 bis 63n) des D-Typs wellenförmig umgewandelt und an den zweiten Multiplexer (2) geliefert wird, wenn der entsprechende erste Multiplexer (11, 12 ... 1n) einen normalen Zustand annimmt und der Mustergenerator ein alternierendes Mustersignal mit der Hälfte der Taktberggeschwindigkeit der ersten Multiplexer (11, 12 ... 1n) durch Zuführen des polarität-umgekehrten Ausgangssignals der Kippschaltung (631 bis 63n) des D-Typs zu einem Dateneingangsanschluß von diesem erzeugt, wobei das alternierende Mustersignal an den zweiten Multiplexer (2) geliefert wird, wenn der entsprechende erste Multiplexer (11, 12 ... 1n) in einem Fehlerzustand ist.

6. Multiplexsystem nach Anspruch 5, dadurch gekennzeichnet, daß jeder Selektor (61 bis 6n) weiter enthält:

—ein NOR-Gate (621 bis 62n) mit zwei Eingangsanschlüssen, wobei das Ausgangssignal der Kippschaltung (631 bis 63n) des D-Typs an einem Anschluß eingegeben wird und das Fehler andeutende Signal des entsprechenden ersten Multiplexers (11, 12 ... 1n) an dem anderen eingegeben wird; und

—ein ODER-Gate (611 bis 61n) mit zwei Eingangsanschlüssen, wobei das Ausgangssignal des entsprechenden ersten Multiplexers (11, 12 ... 1n) an einem Anschluß eingegeben wird und das Ausgangssignal des NOR-Gates (621 bis 62n) an dem anderen eingegeben wird, und zum Zuführen des Ausgangssignals desselben an den

Dateneingangsanschluß der Kippschaltung (631 bis 63n) des D-Typs.

7. Multiplexsystem nach Anspruch 3, dadurch gekennzeichnet, daß der Mustergenerator enthält:

—ein UND-Gate (8) mit einer Vielzahl von Eingangsanschlüssen, wobei das Fehler andeutende Signal von jedem ersten Multiplexer (11, 12 ... 1n) an einem entsprechenden Eingangsanschluß des UND-Gates (8) eingegeben wird;

—eine Kippschaltung (63) des D-Typs zum Zuführen des alternierenden Mustersignals als ein Ausgangssignal zu den Selektoren (91, 92 ... 9n);

—ein NOR-Gate (62) mit zwei Eingangsanschlüssen, wobei das Ausgangssignal der Kippschaltung (63) des D-Typs an einem Anschluß eingegeben wird und das Ausgangssignal von dem UND-Gate (8) an dem anderen eingegeben wird; und

—ein ODER-Gate (61) mit zwei Eingangsanschlüssen, wobei das Ausgangssignal des NOR-Gates (62) an einem Anschluß eingegeben wird und das Ausgangssignal von dem UND-Gate (8) an dem anderen eingegeben wird, und zum Zuführen dessen Ausgangssignals zu dem Dateneingangsanschluß der Kippschaltung (63) des D-Typs.

Revendications

1. Système multiplex comportant:

plusieurs premiers multiplexeurs (11, 12, 1n) comprenant des sorties qui délivrent des signaux de données; et

un second multiplexeur (2) destiné à multiplexer un signal d'entrée en parallèle en convertissant simplement le signal d'entrée en parallèle en un signal de sortie en série;

caractérisé par:

un générateur de configuration (4, 6) destiné à produire un signal de configuration alternative en synchronisme avec les signaux émis par lesdits premiers multiplexeurs (11, 12 ... 1n); et

plusieurs sélecteurs (31, 32 ... 3n; 61, 62 ... 6n; 91, 92 ... 9n) connectés chacun en fonctionnement audit générateur de configuration (4, 6), audit second multiplexeur (2) et à la sortie de l'un correspondant desdites premiers multiplexeurs (11, 12 ... 1n), pour sélectionner le signal de données émis par le premier multiplexeur correspondant (11, 12 ... 1n) quand le premier multiplexeur correspondant (11, 12 ... 1n) adopte un état normal et sélectionnant le signal de configuration alternative quand le premier multiplexeur correspondant (11, 12 ... 1n) adopte un état de dérangement et émettant des signaux de sortie qui y sont sélectionnés vers ledit second multiplexeur (2) comme le signal d'entrée en parallèle.

2. Système multiplex selon la revendication 1, dans lequel un signal d'horloge de temporisation commande lesdits premiers multiplexeurs (11, 12 ... 1n) et

dans lequel ledit générateur de configuration (4, 6) comporte un démultiplicateur de fréquence



(4) destiné à diviser par deux le signal d'horloge de temporisation desdits premiers multiplexeurs (11, 12 ... 1n).

3. Système multiplex selon la revendication 1, dans lequel chacun desdits premiers multiplexeurs (11, 12 ... 1n) émet en plus un signal indicateur de dérangement lorsqu'il est en état de dérangement, et

dans lequel chacun des sélecteurs (31, 32 ... 3n) comporte:

une porte ET (311 à 31n) comprenant deux bornes d'entrée et fournissant un signal de sortie à une borne de sortie, le signal de configuration alternative provenant dudit générateur de configuration (4) étant appliqué à l'une des bornes d'entrée et le signal indicateur de dérangement du premier multiplexeur correspondant (11, 12 ... 1n) étant appliqué à l'autre des bornes d'entrée, et une porte OU (321 à 32n) comprenant deux bornes d'entrée et une borne de sortie connectées en fonctionnement audit second multiplexeur (2), le signal de sortie de ladite porte ET (311 à 31n) étant appliqué à l'une des bornes d'entrée et le signal de données provenant du premier multiplexeur correspondant (11, 12 ... 1n) étant appliqué à l'autre desdites bornes d'entrée.

4. Système multiplex selon la revendication 1, dans lequel chacun des signaux émis par les sélecteurs (31 à 3n) est appliqué au second multiplexeur (2) par l'intermédiaire d'un circuit bistable du type D (51 à 5n) pour la conformation de la forme d'onde.

5. Système multiplex selon la revendication 1, dans lequel chacun des sélecteurs (61 à 6n) comporte un circuit bistable du type D (631 à 63n) commandé par une horloge de temporisation des premiers multiplexeurs (11, 12 ... 1n) et constituée de manière que le signal émis par le premier multiplexeur correspondant (11, 12 ... 1n) soit conformé par le circuit bistable du type D (631 à 63n) et soit appliqué au second multiplexeur (2) quand le premier multiplexeur correspondant (11, 12 ... 1n) adopte un état normal et ledit générateur de configuration produisant un signal de configuration alternative ayant la moitié de la fréquence d'horloge de temporisation des premiers multiplexeurs (11, 12 ... 1n) en appliquant le

signal de sortie de polarité inversée du circuit bistable du type D (631 à 63n) à sa borne d'entrée de données, ledit signal de configuration alternative étant appliqué au second multiplexeur (2) quand le premier multiplexeur correspondant (11, 12 ... 1n) est en état de dérangement.

6. Système multiplex selon la revendication 5, dans lequel chaque sélecteur (61 à 6n) comporte en outre:

une porte NON-OU (621 à 62n) comprenant deux bornes d'entrée, le signal de sortie du circuit bistable du type D (631 à 63n) étant appliqué à une borne et le signal indicateur de dérangement du premier multiplexeur correspondant (11, 12 ... 1n) étant appliqué à l'autre, et

une porte OU (611 à 61n) comprenant deux bornes d'entrée, le signal de sortie du premier multiplexeur correspondant (11, 12 ... 1n) étant appliqué à une borne et le signal de sortie de la porte OU (621 à 62n) étant appliqué à l'autre et fournissant son signal de sortie à la borne d'entrée de données du circuit bistable du type D (631 à 63n).

7. Système multiplex selon la revendication 3, dans lequel ledit générateur de configuration comporte:

une porte ET (8) avec plusieurs bornes d'entrée, les signaux indicateurs de dérangement provenant de chaque premier multiplexeur (11, 12 ... 1n) étant appliquées à une borne d'entrée correspondante de ladite porte ET (8);

un circuit bistable du type D (63) destiné à fournir le signal de configuration alternative comme un signal de sortie auxdits sélecteurs (91, 92 ... 9n);

une porte NON-OU (62) avec deux bornes d'entrée, le signal de sortie du circuit bistable du type D (63) étant appliqué à une borne et le signal de sortie de ladite porte (ET) (8) étant appliqué à l'autre; et

une porte OU (61) avec deux bornes d'entrée, le signal de sortie de la porte NON-OU (62) étant appliqué à une borne et le signal de sortie de ladite porte ET (8) étant appliqué à l'autre et fournissant son signal de sortie à la borne d'entrée de données du circuit bistable du type D (63).



* C L M S *