CLAIMS

1. A method for manufacturing a bit line structure, characterized in that, the method comprises:

forming a bit line conductive layer on a surface of a semiconductor substrate, wherein the bit line conductive layer is partially located in a groove in the surface of the semiconductor substrate;

forming a first protective layer on a surface of the bit line conductive layer and the surface of the semiconductor substrate;

forming a first barrier layer on a surface of the first protective layer, wherein a material of the first barrier layer comprises silicon dioxide;

subjecting the surface of the first barrier layer with passivating treatment, wherein the passivating treatment comprises nitrogen plasma treatment;

forming a sacrificial layer on the surface of the first barrier layer, wherein the sacrificial layer is provided with a filling part filled in the groove; and

cleaning and stripping a part, other than the filling part, of the sacrificial layer by using an etching solution.

2. The method for manufacturing the bit line structure according to claim 1, wherein the first barrier layer subjected with the passivating treatment comprises a structure of two thin film layers, wherein the two thin film layers are respectively a first thin film layer adjacent to the first protective layer and a second thin film layer far away from the first protective layer, wherein an etching selection ratio of the sacrificial layer to the

second thin film layer is greater than an etching selection ratio of the sacrificial layer to the first thin film layer when the etching solution comprises phosphoric acid solution.

3. The method for manufacturing the bit line structure according to claim 2, wherein a material of the second thin film layer comprises silicon oxynitride.

4. The method for manufacturing the bit line structure according to claim 1, wherein the first protective layer has a thickness in range of 1 nm to 3 nm, and the first barrier layer has a thickness in range of 2 nm to 8 nm.

5. The method for manufacturing the bit line structure according to claim 1, wherein a material of the first protective layer comprises silicon nitride; and the material of the sacrificial layer comprises silicon nitride.

6. The method for manufacturing the bit line structure according to claim 1, wherein the etching solution comprises phosphoric acid solution; and a temperature of the etching solution is 100°C to 120°C.

7. The method for manufacturing the bit line structure according to claim 1, wherein the etching solution comprises phosphoric acid; and a concentration of the etching solution is 40% to 60%.

8. The method for manufacturing the bit line structure according to claim 1, after cleaning and stripping the part, other than the filling part, of the sacrificial layer by using the etching solution, further comprising:

stripping an exposed portion of the first barrier layer;

forming a second barrier layer on the surface of the bit line conductive layer and the surface of the semiconductor substrate; and

forming a second protective layer on a surface of the second barrier layer.

9. The method for manufacturing the bit line structure according to claim 1, wherein the cleaning and stripping the sacrificial layer by using the etching solution comprises:

pre-cleaning a surface of the sacrificial layer by using a diluted hydrofluoric acid solution, so as to strip an oxide layer from the surface of the sacrificial layer; and

cleaning the sacrificial layer by using phosphoric acid solution, so as to strip the part, other than the filling part, of the sacrificial layer.

10. A method for manufacturing a semiconductor structure, characterized in that, the method comprises:

providing a semiconductor substrate, wherein the surface of the semiconductor substrate is provided with a groove; and

forming a bit line structure on the semiconductor substrate by the method for manufacturing the bit line structure according to any one of claims 1 to 9.

11. The method for manufacturing the semiconductor structure according to claim 10, wherein the passivating treatment on the first barrier layer comprises the following steps:

pre-heating a treatment chamber of treatment equipment;

placing the semiconductor structure with the first barrier layer formed thereon in the treatment chamber;

inputting a reaction medium and subjecting the surface of the first barrier layer with the plasma treatment;

cooling the treatment chamber; and

taking out the semiconductor structure.

12. A semiconductor structure, characterized in that, the semiconductor structure comprises:

a semiconductor substrate, a surface of the semiconductor substrate being provided with a groove;

a bit line conductive layer, the bit line conductive layer being partially located in a groove in the surface of the semiconductor substrate; and

a bit line plug spacer layer, the bit line plug spacer layer being filled in the groove, and the bit line plug spacer layer comprising a first protective layer, a first barrier layer subjected with passivating treatment, and a filling part;

wherein the passivating treatment comprises nitrogen plasma treatment, the first barrier layer subjected with the passivating treatment comprises a structure of two film

layers, wherein the two thin film layers are respectively a first thin film layer adjacent to the first protective layer and a second thin film layer far away from the first protective layer, a material of the first thin film layer comprises silicon oxide, and a material of the second thin film layer comprises silicon oxynitride.

13. The semiconductor structure according to claim 12, wherein the first protective layer has a thickness in range of 1 nm to 3 nm.

14. The semiconductor structure according to claim 12, wherein the first barrier layer has a thickness in range of 2 nm to 8 nm.

15. The semiconductor structure according to claim 12, wherein a material of the first protective layer comprises silicon nitride.

16. The semiconductor structure according to claim 12, wherein a material of the filling part comprises silicon nitride.

17. The semiconductor structure according to claim 12, wherein an etching selectivity of the filling part to the second thin film layer is greater than an etching selectivity of the filling part to the first thin film layer when the etching solution comprises phosphoric acid solution.