



A DIGITAL MULTIPLIER WITH REDUCED SPURIOUS SWITCHING BY MEANS OF LATCH ADDERS

Abstract

[0042] A digital Parallel Multiplier having a Partial Product Generator (3), a First Stage Adder Circuit (81) and a Final Stage Adder Circuit (82), wherein the spurious switching in the First Stage Adder Circuit (81) may be substantially reduced by synchronizing the input signals to the Adders in First Stage Adder Circuit (81). The reduced spurious switching reduces the power dissipation of the Multiplier. The timing of the input signals is synchronized by means of the Latch Adders (41) having a Latch that is an integral part of an Adder. Consequently, power dissipation and hardware overheads of the Latch Adders (41) are low. The Latch Adders (41) may be controlled by Control Signals (44), which may be generated by Control Circuits (71). The application of the Latch Adders (41) may be applied to the Final Stage Adder Circuit (82) to further reduce spurious switching and thereby further reduce the power dissipation.

[0043] FIG. 6 accompanies the abstract.