

What Is Claimed Is:

1. A vertical-type memory device, comprising:

a plurality of gate electrode layers spaced apart from one another and stacked on a substrate, and extending by different lengths in a first direction and forming a staircase structure;

a first interlayer insulating layer covering the staircase structure of the plurality of gate electrode layers; and

a plurality of gate contact plugs penetrating the first interlayer insulating layer and respectively contacting the gate electrode layers,

wherein the plurality of gate electrode layers comprise lower gate electrode layers disposed adjacently to the substrate, and upper gate electrode layers disposed on the lower gate electrode layers so that the lower gate electrode layers are between the substrate and the upper gate electrode layers, ~~and~~

wherein the plurality of gate contact plugs comprise lower gate contact plugs connected to the lower gate electrode layers, and upper gate contact plugs connected to the upper gate electrode layers,

wherein the upper gate contact plugs have top-most portions disposed at a height higher than a height of top surfaces of the lower gate contact plugs, and

wherein the lower gate contact plugs are each integrally formed of a continuous material to extend from a respective lower gate electrode layer to a height above a top surface of the first interlayer insulating layer, and

the upper gate contact plugs are each integrally formed of a continuous material to extend from a respective upper gate electrode layer to a height above the top surface of the first interlayer insulating layer.

2. ~~The vertical-type memory device of claim 1, wherein:~~

~~the lower gate contact plugs are each integrally formed of a continuous material to~~

~~extend from a respective lower gate electrode layer to a height above a top surface of the first interlayer insulating layer; and~~

~~the upper gate contact plugs are each integrally formed of a continuous material to extend from a respective upper gate electrode layer to a height above a top surface of the first interlayer insulating layer.~~

32. The vertical-type memory device of claim 1 ~~or claim 2~~, further comprising:
a plurality of contact studs respectively disposed on the lower gate contact plugs,
wherein the top-most portions of the upper gate contact plugs are disposed at the
same height as a height of top-most portions of the plurality of contact studs.

43. The vertical-type memory device of claim 32, further comprising:
first metal wires respectively disposed on and directly connected to the upper gate
contact plugs and second metal wires respectively disposed on and directly connected to the
plurality of contact studs.

54. The vertical-type memory device of claim 43, wherein the first metal wires
are respectively integrated with the upper gate contact plugs.

65. The vertical-type memory device of any one of claims 1 to 54, wherein the
plurality of gate electrode layers forming the staircase structure have ends including pad
regions having thicknesses greater than thicknesses of other regions of the plurality of gate
electrode layers, and the plurality of gate contact plugs contact the pad regions.

76. The vertical-type memory device of any one of claims 1 to 65, further
comprising:

a lower wiring structure disposed below the substrate; and
through plugs penetrating through the plurality of gate electrode layers and

contacting the lower wiring structure,

wherein the top-most portions of the upper gate contact plugs are disposed at a height higher than a height of top surfaces of the through plugs.

5 ~~8~~7. The vertical-type memory device of any one of claims 1 to ~~7~~6, further comprising:

 a plurality of channel structures penetrating through the plurality of gate electrode layers; and

 a plurality of dummy structures penetrating through at least one of the plurality of
10 gate electrode layers, and disposed adjacently to the plurality of gate contact plugs.

~~9~~8. The vertical-type memory device of claim ~~8~~7, wherein the plurality of dummy structures have the same structure as a structure of the plurality of channel structures, and are electrically connected to the substrate.

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~~10~~9. The vertical-type memory device of claim ~~8~~7, wherein the plurality of channel structures have a structure different from a structure of the plurality of dummy structures, the plurality of channel structures are electrically connected to the substrate, and the plurality of dummy structures are insulated from the substrate.

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~~11~~10. A vertical-type memory device, comprising:

 a memory cell region comprising a plurality of gate electrode layers spaced apart from one another and vertically stacked on a substrate, a first interlayer insulating layer covering the plurality of gate electrode layers, and a plurality of gate contact plugs
25 penetrating the first interlayer insulating layer and respectively contacting the plurality of gate electrode layers,

 wherein the plurality of gate contact plugs comprise a first gate contact plug contacting a lowermost gate electrode layer among the plurality of gate electrode layers, and

a second gate contact plug contacting an uppermost gate electrode layer among the plurality of gate electrode layers, and the first gate contact plug has a top surface having a first height lower than a second height of a top-most portion of the second gate contact plug, and

wherein the first gate contact plug is integrally formed of a continuous material to extend from the lowermost gate electrode layer to a height above a top surface of the first interlayer insulating layer~~the uppermost gate electrode layer~~; and

the second gate contact plug is integrally formed of a continuous material to extend from the uppermost gate electrode layer to a height above the top surface of the first interlayer insulating layer~~the second height~~.

~~12~~11. The vertical-type memory device of claim ~~11~~10, further comprising:

a peripheral circuit region comprising circuit devices and lower wiring structures disposed on a lower substrate below the substrate, wherein the memory cell region is disposed on the peripheral circuit region.

~~13~~12. The vertical-type memory device of claim ~~11~~10 or claim ~~12~~11, wherein the plurality of gate electrode layers extend by different lengths in a first direction and form a staircase structure, ~~and further comprising:~~

~~a~~the first interlayer insulating layer covering covers the staircase structure of the plurality of gate electrode layers, ~~wherein~~

the first gate contact plug penetrates the first interlayer insulating layer to contact the lowermost gate electrode layer, and

the second gate contact plug penetrates the first interlayer insulating layer to contact the uppermost gate electrode layer.

~~14~~13. The vertical-type memory device of claim ~~13~~12, further comprising:

a through region penetrating through the substrate and the plurality of gate electrode layers; and

a through plug penetrating through the through region and connected to a lower wiring structure disposed on a lower substrate below the substrate,

wherein the through plug has a top surface having a height lower than the second height.

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~~15~~14. The vertical-type memory device of any one of claims ~~11~~10 to ~~14~~13, wherein the memory cell region further comprises a contact stud disposed on the first gate contact plug, and the top-most portion of the second gate contact plug is disposed at the same height as a height of a top surface of the contact stud.

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~~16~~15. The vertical-type memory device of any one of claims ~~11~~10 to ~~15~~14, wherein the plurality of gate electrode layers include pad regions and other regions, the pad regions having thicknesses greater than thicknesses of the other regions, and for each gate electrode layer including the lowermost gate electrode layer and uppermost gate electrode layer, a respective gate contact plug contacts a respective pad region.

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~~17~~16. The vertical-type memory device of any one of claims ~~11~~10 to ~~16~~15, further comprising:

a plurality of working channel structures penetrating through the plurality of gate electrode layers; and

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a plurality of dummy channel structures penetrating through at least one of the plurality of gate electrode layers.

~~18~~17. The vertical-type memory device of claim ~~17~~16, wherein the plurality of working channel structures have structures different from the plurality of dummy channel structures, the plurality of working channel structures are electrically connected to the substrate, and the plurality of dummy channel structures are insulated from the substrate.

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1918. The vertical-type memory device of any one of claims 11-10 to 1817, wherein the first gate contact plug comprises a region having a width decreasing towards the substrate, which width then increases.

2019. A vertical-type memory device, comprising:

- a lower substrate;
- circuit devices provided on the lower substrate;
- a lower interlayer insulating layer covering the circuit devices;
- an upper substrate disposed on the lower interlayer insulating layer;
- a first gate electrode layer and a second gate electrode layer spaced apart from each other and stacked on the upper substrate;
- an upper interlayer insulating layer covering the first gate electrode layer and the second gate electrode layer;
- a first gate contact plug and a second gate contact plug penetrating through the upper interlayer insulating layer and respectively contacting the first gate electrode layer and the second gate electrode layer; and
- a through plug penetrating through the first and second gate electrode layers and the upper substrate and electrically connected to the circuit devices,

wherein the first gate contact plug and the through plug have top surfaces having heights lower than a height of a top-most portion of the second gate contact plug, and

wherein the first gate contact plug is integrally formed of a continuous material to extend from the first gate electrode layer to a height above a top surface of the upper interlayer insulating layer, and

the second gate contact plug is integrally formed of a continuous material to extend from the second gate electrode layer to a height above the top surface of the upper interlayer insulating layer.