CLAIMS

What is claimed is:

1. A chip matrix, comprising:

a wafer, wherein the wafer has cutting lines that are evenly distributed on the wafer;

a first silicon oxide layer, wherein the first silicon oxide layer is made of silicon oxide and is formed on an upper surface of the wafer; and

a transition metal oxide layer, wherein the transition metal oxide layer is made of a transition metal oxide and is formed on an upper surface of the first silicon oxide layer, wherein the transition metal oxide layer consists of a plurality of transition metal oxide spots that are unconnected to each other.

2. The chip matrix according to claim 1, wherein:

the plurality of transition metal oxide spots has a thickness of 10 nm to 20 nm; and the first silicon oxide layer has a thickness of 80 nm to 100 nm, preferably 90 nm;

the plurality of transition metal oxide spots is connected with amino groups; and

the first silicon oxide layer located among the plurality of transition metal oxide spots that are unconnected to each other is connected with polyethylene glycol.

3. A chip matrix, comprising:

a wafer, wherein the wafer has cutting lines that are evenly distributed on the wafer;

a first silicon oxide layer, wherein the first silicon oxide layer is made of silicon oxide and is formed on an upper surface of the wafer;

a transition metal oxide layer, wherein the transition metal oxide layer is made of a transition metal oxide and is formed on an upper surface of the first silicon oxide layer; and

a second silicon oxide layer, wherein:

the transition metal oxide layer is of a continuous layer structure, and the second silicon oxide layer is made of silicon oxide and formed on an upper surface of the transition metal oxide layer as a plurality of wells that are connected to each other; or

the transition metal oxide layer consists of a plurality of transition metal oxide spots that are unconnected to each other, and the second silicon oxide layer is formed on the upper surface of the first silicon oxide layer located among the plurality of transition metal oxide spots that are unconnected to each other.

4. The chip matrix according to claim 3, wherein

the wafer is a silicon wafer, the second silicon oxide layer has a thickness ranging from 40 nm to 60 nm, preferably 50 nm, the transition metal oxide layer has a thickness ranging from 5 nm to 15nm, and the first silicon oxide layer has a thickness ranging from 80 nm to 100 nm, preferably 90 nm; or

the wafer is a quartz wafer, the second silicon oxide layer has a thickness ranging from 100 nm to 200 nm, the transition metal oxide layer has a thickness ranging from 10nm to 20nm, and the first silicon oxide layer has a thickness ranging from 80 nm to 100 nm, preferably 90nm.

5. The chip matrix according to claim 3, wherein,

when the transition metal oxide layer is of a continuous layer structure, amino groups are connected to the transition metal oxide layer at a bottom of each well of the second silicon oxide layer; or when the transition metal oxide layer consists of a plurality of transition metal oxide spots, amino groups are connected to the plurality of transition metal oxide spots; and

the second silicon oxide layer is connected with polyethylene glycol.

6. The chip matrix according to claim 2 or 5, wherein the amino groups are connected to at least a part of transition metal oxide molecules in the transition metal oxide layer through chemical bonds;

optionally, the chemical bonds are formed by the at least part of transition metal oxide molecules and phosphate groups of aminophosphonic acid-based compounds.

7. The chip matrix according to claim 2 or 5, wherein the polyethylene glycol is provided by at least one selected from polyethyleneimine-polyethylene glycol and a silane coupling agent containing polyethylene glycol;

when the polyethylene glycol is provided by the polyethyleneimine-polyethylene glycol, and the polyethyleneimine-polyethylene glycol is electrostatically adsorbed on a surface of the first silicon oxide layer or a surface of the second silicon oxide layer; and

when the polyethylene glycol is provided by the silane coupling agent containing polyethylene glycol, and the silane coupling agent containing polyethylene glycol is connected to the first silicon oxide layer or the second silicon oxide layer through a -Si-O-Si- chain.

8. The chip matrix according to any one of claims 1-7, wherein the transition metal oxide comprises at least one of titanium dioxide, zirconium dioxide, tantalum pentoxide, niobium hexaoxide, or hafnium dioxide.

9. A sequencing chip, comprising a chip body, wherein the chip body comprises a number of chip units, wherein each chip unit is a unit of the chip matrix according to any one of claims 2, 5 to 8 along the cutting lines of the wafer.

10. A method for manufacturing the chip matrix according to any one of claims 1-8, the method comprising: performing surface modification on the wafer,

wherein the surface modification comprises: treating a surface of the wafer with a transition metal oxide to form the transition metal oxide layer, wherein the transition metal oxide layer is formed on an upper surface of the first silicon oxide layer, the first silicon oxide layer is provided on the upper surface of the wafer, and the silicon oxide layer is made of silicon oxide, and the wafer has cutting lines evenly distributed on the wafer.

11. The method according to claim 10, wherein the first silicon oxide layer is formed in advance on the upper surface of the wafer by low-temperature plasma chemical vapor deposition, plasma enhanced chemical vapor deposition, sputtering, or atomic layer deposition.

12. The method according to claim 10, wherein the surface modification of the wafer is performed by thin film deposition, photolithography, or etching to form the transition metal oxide layer in form of a continuous layer or in form of arrayed spots.

13. The method according to claim 12, wherein, for the transition metal oxide layer in form of a continuous layer, the method further comprises forming, with silicon oxide, a second silicon oxide layer in form of continuous wells on an upper surface of the transition metal oxide layer;

optionally, for the transition metal oxide layer in form of arrayed spots, the method further comprises depositing silicon oxide between the spots of the transition metal oxide layer to form a second silicon oxide layer.

14. The method according to any one of claims 10-13, further comprising performing amination treatment on the transition metal oxide,

wherein the amination treatment is performed by reacting transition metal oxide with an aminophosphonic acid-based compound.

15. The method according to any one of claims 10-14, further comprising performing a surface modification on the first silicon oxide layer or the second silicon oxide layer to introduce polyethylene glycol on the first silicon oxide layer or the second silicon oxide layer;

wherein the polyethylene glycol is provided by at least one of polyethyleneimine-polyethylene glycol or a silane coupling agent containing polyethylene glycol;

optionally, when the polyethylene glycol is provided by polyethyleneimine-polyethylene glycol, the surface modification is performed by electrostatic adsorption of polyethyleneimine-polyethylene glycol on a surface of the first silicon oxide layer or a surface of the second silicon oxide layer;

optionally, when the polyethylene glycol is provided by the silane coupling agent containing polyethylene glycol, the surface modification is performed by condensation reaction of the silane coupling agent containing polyethylene glycol with hydroxyl groups of the first silicon oxide layer or the second silicon oxide layer, wherein the hydroxyl groups are provided by Si-OH generated after the first silicon oxide layer or the second silicon oxide layer is ionized and adsorbs hydroxide ions in water.

16. A method for manufacturing a sequencing chip, comprising:

assembling a chip unit, wherein the chip unit is obtained by cutting a chip matrix along cutting lines of a wafer layer of the chip matrix, the chip matrix is as defined in any one of claims 2, 5 to 8.

17. The method according to claim 16, wherein said assembling comprises placing the chip unit in a supporting frame including a liquid inlet and outlet, and bonding the chip unit to the supporting frame with a glue or adhesive, a fluid channel being formed between the frame and the chip unit.

18. The method according to claim 17, wherein, when the wafer is a silicon wafer, said assembling comprises: bonding the chip unit to the support frame with an upper surface of the chip unit facing upward, and placing a cover glass on the upper surface of the chip unit to obtain the sequencing chip.

19. The method according to claim 17, wherein, when the wafer is a quartz wafer or a glass wafer, said assembling comprises: bonding the chip unit to the support frame with a lower surface of the chip unit facing upward to obtain the sequencing chip.

20. A sequencing method, comprising performing sequencing using the sequencing chip as defined in claim 9 or manufactured by the method of any one of claims 16-19.