Description

METHOD AND APPARATUS FOR CHANNEL ENCODING AND DECODING IN A COMMUNICATION SYSTEM USING LOW-DENSITY PARITY-CHECK CODES

Technical Field

[1] The present invention relates to a communication system using Low-Density Parity-Check (LDPC) codes. More particularly, the present invention relates to a channel encoding/decoding method and apparatus for generating LDPC codes with various codeword lengths and code rates from an LDPC code given in high-order modulation.

Background Art

[2] In wireless communication systems, link performance significantly decreases due to various noises in the channels, a fading phenomenon, and Inter-Symbol Interference (ISI). Therefore, in order to realize high-speed digital communication systems, which require high data throughput and reliability, such as the next-generation mobile communication, digital broadcasting, and portable Internet, it is important to develop technology for overcoming the channel noises, fading, and ISI. Recently, an intensive study of error-correcting codes has been conducted as a method for increasing communication reliability by efficiently recovering distorted information.

[3] An LDPC code, first introduced by Gallager in 1960s, has lost favor over time due to its implementation complexity which could not be resolved by the technology at that time. However, as the turbo code, which was discovered by Berrou, Glavieux, and Thitimajshima in 1993, exhibits performance levels approximating Shannon's channel limit, research has been conducted on iterative decoding and channel encoding based on a graph along with analyses on performance and characteristics of the turbo code. With this as a momentum, the LDPC code was restudied in the late 1990s, which proved that the LDPC code exhibits performance levels approximating the Shannon's channel limit if the LDPC undergoes decoding by applying iterative decoding based on a sum-product algorithm on a Tanner graph (a special case of a factor graph) corresponding to the LDPC code.

[4] The LDPC code is commonly represented using a graph representation technique, and many characteristics can be analyzed through the methods based on graph theory, algebra, and probability theory. Generally, a graph model of channel codes is useful for description of codes, and by mapping information on encoded bits to vertexes in the graph and mapping relations between the bits to edges in the graph, it is possible to consider the graph as a communication network in which the vertexes exchange predetermined messages through the edges, thus making it possible to derive a natural

decoding algorithm. For example, a decoding algorithm derived from a trellis, which can be regarded as a kind of graph, may include the well-known Viterbi algorithm and a Bahl, Cocke, Jelinek and Raviv (BCJR) algorithm.

[5] The LDPC code is generally defined as a parity-check matrix, and can be expressed using a bipartite graph, which is referred to as a Tanner graph. The bipartite graph is a graph where vertexes forming the graph are divided into two different types, and the LDPC code is represented with the bipartite graph consisting of vertexes, some of which are called variable nodes and the other of which are called check nodes. The variable nodes are one-to-one mapped to the encoded bits.

[6] A graph representation method for the LDPC code will be described with reference to FIGs. 1 and 2.

[7] FIG. 1 illustrates an example of a parity-check matrix H_1 of an LDPC code with 4 rows and 8 columns. Referring to FIG. 1, because the number of columns is 8, the parity-check matrix H_1 signifies an LDPC code that generates a length-8 codeword, and the columns are mapped to 8 encoded bits on a one to one basis.

[8] FIG. 2 illustrates a Tanner graph corresponding to the parity-check matrix H_1 in FIG. 1.

[9] Referring to FIG. 2, the Tanner graph of the LDPC code includes 8 variable nodes x_1 (202), x_2 (204), x_3 (206), x_4 (208), x_5 (210), x_6 (212), x_7 (214), and x_8 (216), and 4 check nodes 218, 220, 222, and 224. An ith column and a jth row in the parity-check matrix H_1 of the LDPC code are mapped to a variable node x_i and a jth check node, respectively. In addition, a value of 1, i.e. a non-zero value, at the point where an ith column and a jth row in the parity-check matrix H_1 of the LDPC code cross each other, indicates that there is an edge between the variable node x_i and the jth check node on the Tanner graph as shown in FIG. 2.

[10] In the Tanner graph of the LDPC code, a degree of the variable node and the check node indicates the number of edges connected to each respective node, and the degree is equal to the number of non-zero entries in a column or row corresponding to the pertinent node in the parity-check matrix of the LDPC code. For example, in FIG. 2, degrees of the variable nodes x_1 (202), x_2 (204), x_3 (206), x_4 (208), x_5 (210), x_6 (212), x_7 (214), and x_8 (216) are 4, 3, 3, 3, 2, 2, 2, and 2, respectively, and degrees of check nodes 218, 220, 222, and 224 are 6, 5, 5, and 5, respectively. In addition, the numbers of non-zero entries in the columns of the parity-check matrix H_1 of FIG. 1, which correspond to the variable nodes in FIG. 2, coincide with their degrees 4, 3, 3, 3, 2, 2, 2, and 2, and the numbers of non-zero entries in the rows of the parity-check matrix H_1 of FIG. 1, which correspond to the check nodes in FIG. 2, coincide with their degrees 6, 5, 5, and 5.

[11] In order to express degree distribution for the nodes of the LDPC code, a ratio of the

number of degree-i variable nodes to the total number of variable nodes is defined as f_i, and a ratio of the number of degree-j check nodes to the total number of check nodes is defined as g_j. For example, for the LDPC code corresponding to FIGs. 1 and 2, $f_2=4/8$, $f_3=3/8$, $f_4=1/8$, and $f_i=0$ for $i\neq 2, 3, 4$; and $g_5=3/4$, $g_6=1/4$, and $g_j=0$ for $j\neq 5, 6$. When a length of the LDPC code, i.e. the number of columns, is defined as N, and the number of rows is defined as $N/2$, the density of non-zero entries in the entire parity-check matrix having the above degree distribution is computed as shown in Equation (1).

[12]

$$\frac{2f_2N+3f_3N+4f_4N}{N\cdot N/2}=\frac{5.25}{N}$$

.....(1)

[13] In Equation (1), as N increases, the density of 1's in the parity-check matrix decreases. Generally, as for the LDPC code, because the codeword length N is inversely proportional to the density of non-zero entries, the LDPC code with a large N has a very low density of non-zero entries. The term "low-density" in the name of the LDPC code originates from the above-mentioned relationship.

[14] Next, with reference to FIG. 3, a description will be made of characteristics of a parity-check matrix of a structured LDPC code applicable to the present invention. FIG. 3 illustrates an LDPC code adopted as the standard technology in Digital Video Broadcasting-Satellite transmission 2nd generation(DVB-S2), which is one of the European digital broadcasting standards.

[15] In FIG. 3, N_1 and K_1 denote a codeword length and an information length (or a length of an information word) of an LDPC code, respectively, and (N_1-K_1) provides a parity length. Further, integers M_1 and q are determined to satisfy $q=(N_1-K_1)/M_1$. Preferably, K_1/M_1 should also be an integer. The parity-check matrix in FIG. 3 will be referred to herein as a first parity-check matrix H_1, for convenience only.

[16] Referring to FIG. 3, a structure of a parity part, i.e. K_1^{th} column through $(N_1-1)^{th}$ column, in the parity-check matrix, has a dual diagonal shape. Therefore, as for degree distribution over columns corresponding to the parity part, all columns have a degree '2', except for the last column having a degree '1'.

[17] In the parity-check matrix, a structure of an information part, i.e. 0th column through $(K_1-1)^{th}$ column, is made using the following rules.

[18] Rule 1: A total of K_1/M_1 column groups are generated by grouping K_1 columns corresponding to the information word in the parity-check matrix into multiple groups each including M_1 columns. A method for forming columns belonging to each column group follows Rule 2 below.

[19] Rule 2: First, positions of '1's in each 0th column in i^{th} column groups (where $i=1,...,K$

$_1/M_1$) are determined. When a degree of a 0th column in each ith column group is denoted by D_i, if positions of rows with 1 are assumed to be

$$R_{i,0}^{(1)}, R_{i,0}^{(2)}, \ldots, R_{i,0}^{(D)}$$

, positions

$$R_{i,j}^{(k)} (k = 1,2,\ldots, D_i)$$

of rows with 1 are defined as shown in Equation (2), in a jth row (where j=1,2,...,M_1-1) in an ith column group.

[20]

$$R_{i,j}^{(k)} = R_{i,(j-1)}^{(k)} + q \bmod (N_1 - K_1),$$
$$k = 1,2,\ldots,D_i, \quad i = 1,\ldots,K_1/M_1, \quad j = 1,\ldots,M_1 - 1$$

. . . . . (2)

[21] According to the above rules, it can be appreciated that degrees of columns belonging to an ith column group are all equal to D_i. For a better understanding of a structure of a DVB-S2 LDPC code that stores information on the parity-check matrix according to the above rules, the following detailed example will be described.

[22] As a detailed example, for N_1=30, K_1=15, M_1=5, and q=3, three sequences for information on the positions of rows with 1 for 0thcolumns in 3 column groups can be expressed as follows. Herein, these sequences are called "weight-1 position sequences."

[23]

$$R_{1,0}^{(1)} = 0, \; R_{1,0}^{(2)} = 1, \; R_{1,0}^{(3)} = 2,$$
$$R_{2,0}^{(1)} = 0, \; R_{2,0}^{(2)} = 11, \; R_{2,0}^{(3)} = 13,$$
$$R_{3,0}^{(1)} = 0, \; R_{3,0}^{(2)} = 10, \; R_{3,0}^{(3)} = 14.$$

[24] Regarding the weight-1 position sequence for 0th columns in each column group, only the corresponding position sequences can be expressed as follows for each column group. For example:

[25] 0 1 2

[26] 0 11 13

[27] 0 10 14.

[28] In other words, the ith weight-1 position sequence in the i^{th}line sequentially represents information on the positions of rows with 1 in the ith column group.

[29] It is possible to generate an LDPC code having the same concept as that of a DVB-S2 LDPC code in FIG. 4, by forming a parity-check matrix using the information cor-

responding to the detailed example, and Rules 1 and 2.

[30] It is known that the DVB-S2 LDPC code designed in accordance with Rules 1 and 2 can be efficiently encoded using the structural shape. Respective steps in a process of performing LDPC encoding using the DVB-S2 based parity-check matrix will be described below by way of example.

[31] In the following description, as a detailed example, a DVB-S2 LDPC code with N_1 =16200, K_1=10800, M_1=360, and q=15 undergoes an encoding process. For convenience, information bits having a length K_1 are represented as

$$(i_0, i_1, \ldots, i_{K_1-1})$$

, and parity bits having a length (N_1-K_1) are expressed as

$$(p_0, p_1, \ldots, p_{N_1-K_1-1})$$

[32] Step 1: An LDPC encoder initializes parity bits as follows:

[33]

$$p_0 = p_1 = \quad = p_{N_1-K_1-1} = 0$$

[34] Step 2: The LDPC encoder reads information on rows where 1 is located in a column group from a 0th weight-1 position sequence out of the stored sequences indicating the parity-check matrix.

[35]

[36] 0 2084 1613 1548 1286 1460 3196 4297 2481 3369 3451 4620 2622

[37]

$$R_{1,0}^{(1)} = 0,\ R_{1,0}^{(2)} = 2048, R_{1,0}^{(3)} = 1613,\ R_{1,0}^{(4)} = 1548,\ R_{1,0}^{(5)} = 1286,$$
$$R_{1,0}^{(6)} = 1460,\ R_{1,0}^{(7)} = 3196,\ R_{1,0}^{(8)} = 4297,\ R_{1,0}^{(9)} = 2481,\ R_{1,0}^{(10)} = 3369,$$
$$R_{1,0}^{(11)} = 3451,\ R_{1,0}^{(12)} = 4620,\ R_{1,0}^{(13)} = 2622.$$

[38] The LDPC encoder updates particular parity bits p_x in accordance with Equation (3), using the read information and the first information bit i_0. Herein, x is a value of

$$R_{1,0}^{(k)}$$

for

$$k = 1,2,\ldots,13$$

[39]

$$p_0 = p_0 \oplus i_0, \quad p_{2084} = p_{2064} \oplus i_0, \quad p_{1613} = p_{1613} \oplus i_0,$$
$$p_{1548} = p_{1548} \oplus i_0, \quad p_{1286} = p_{1286} \oplus i_0, \quad p_{1460} = p_{1460} \oplus i_0,$$
$$p_{3196} = p_{3196} \oplus i_0, \quad p_{4297} = p_{4297} \oplus i_0, \quad p_{2481} = p_{2481} \oplus i_0,$$
$$p_{3369} = p_{3369} \oplus i_0, \quad p_{3451} = p_{3451} \oplus i_0, \quad p_{4620} = p_{4620} \oplus i_0,$$
$$p_{2622} = p_{2622} \oplus i_0$$

. . . . . (3)

[40] In Equation (3),

$$p_x = p_x \oplus i_0$$

can also be expressed as

$$p_x \leftarrow p_x \oplus i_0$$

, and

$$\oplus$$

represents binary addition.

[41] Step 3: The LDPC encoder first determines a value of Equation (4) for the next 359 information bits i_m (where m=1, 2, ..., 359) after i_0.

[42]

$$\{x + (m \bmod M_1) \times q\} \bmod (N_1 - K_1), \quad M_1 = 360, \quad m = 1,2,\ldots,359$$

. . . . . (4)

[43] In Equation (4), $x$is a value of

$$R_{1,0}^{(k)} \text{ for } k = 1,2,\ldots,13.$$

. It should be noted that Equation (4) is similar to Equation (2).

[44] Next, the LDPC encoder performs an operation similar to Equation (3) using the values found in Equation (4). In other words, the LDPC encoder updates parity bits

$$P_{\{x+(m \bmod M_1)\times q\} \bmod (N_1 - K_1)}$$

for i_m. For example, for m=1, i.e. for i_1, the LDPC encoder updates parity bits

$$P_{(x+q) \bmod (N_1 - K_1)}$$

as defined in Equation (5).

[45]

$$p_{15} = p_{15} \oplus i_1, \quad p_{2099} = p_{2099} \oplus i_1, \quad p_{1628} = p_{1628} \oplus i_1,$$
$$p_{1563} = p_{1563} \oplus i_1, \quad p_{1301} = p_{1301} \oplus i_1, \quad p_{1475} = p_{1475} \oplus i_1,$$
$$p_{3211} = p_{3211} \oplus i_1, \quad p_{4312} = p_{4312} \oplus i_1, \quad p_{2496} = p_{2496} \oplus i_1,$$
$$p_{3384} = p_{3384} \oplus i_1, \quad p_{3466} = p_{3466} \oplus i_1, \quad p_{4635} = p_{4635} \oplus i_1,$$
$$p_{2637} = p_{2637} \oplus i_1$$

..... (5)

[46] It is to be noted that q=15 in Equation (5). The LDPC encoder performs the above process for m=1, 2, ..., 359, in the same manner as shown above.

[47] Step 4: As in Step 2, the LDPC encoder reads information of the 1st weight-1 position sequence

$$R_{2,0}^{(k)} \ (k = 1, 2, ..., 13)$$

for a 361st information bit i_{360}, and updates particular parity bits p_x, where x is

$$R_{2,0}^{(k)}$$

. The LDPC encoder updates

$$p_{\{x+(m \bmod M_1)\times q\} \bmod (N_1 - K_1)}, \quad m = 361, 362, ..., 719$$

by similarly applying Equation (4) to the next 359 information bits i_{361}, i_{362}, ..., i_{719} after i_{360}.

[48] Step 5: The LDPC encoder repeats Steps 2, 3, and 4 for all groups each having 360 information bits.

[49] Step 6: The LDPC encoder finally determines parity bits using Equation (6).

[50]

$$p_i = p_i \oplus p_{i-1}, \quad i = 1, 2, ..., N_1 - K_1 - 1$$

..... (6)

[51] The parity bits p_i of Equation (6) are parity bits that have completely undergone LDPC encoding.

[52] As described above, DVB-S2 carries out encoding through the process of Steps 1 to 6.

Disclosure of Invention

Technical Problem

[53] In order to apply the LDPC code to the actual communication system, the LDPC code should be designed to be suitable for the data rate required in the communication system. Particularly, not only in an adaptive communication system employing Hybrid Automatic Retransmission reQuest (HARQ) and Adaptive Modulation and Coding

(AMC), but also in a communication system supporting various broadcast services, LDPC codes having various codeword lengths are needed to support various data rates according to the system requirements.

[54] However, as described above, the LDPC code used in the DVB-S2 system has only two types of codeword lengths due to its limited use, and each type of the LDPC code needs an independent parity-check matrix. For these reasons, there is a long-felt need in the art for a method for supporting various codeword lengths to increase extendibility and flexibility of the system. Particularly, in the DVB-S2 system, transmission of data having several hundreds to thousands of bits is needed for transmission of signaling information. However, because only 16200 and 64800 are available for lengths of the DVB-S2 LDPC code, there is a still a need for support of various codeword lengths. Yet, since storing independent parity-check matrixes for respective codeword lengths of the LDPC code may reduce memory efficiency, there is a need for a scheme capable of efficiently supporting various codeword lengths from the given existing parity-check matrix, without designing a new parity-check matrix.

Technical Solution

[55] An aspect of an embodiment of the present invention is to address at least the above-mentioned problems and/or disadvantages and to provide at least the advantages described below. Accordingly, an aspect of the present invention is to provide a channel encoding/decoding method and apparatus for generating, from a given LDPC code, an LDPC code with a different codeword length using shortening or puncturing determined by considering high-order modulation in a communication system using LDPC codes.

[56] Another aspect of an embodiment of the present invention is to provide a channel encoding/decoding method and apparatus for guaranteeing optimal performance considering a DVB-S2 structure in a communication system using LDPC codes.

[57] In accordance with one aspect of the present invention, a method for encoding a channel in a communication system using a Low-Density Parity-Check (LDPC) code is provided. The method includes determining a number of parity bits for puncturing; dividing the parity bits at predetermined intervals, and determining a number of puncturing parity bits, which are subjected to puncturing within the predetermined intervals; determining a modulation scheme; determining positions of puncturing parity bits corresponding to the determined number of the puncturing parity bits within the predetermined intervals according to the modulation scheme; repeatedly performing puncturing on puncturing parity bits corresponding to the determined positions at the predetermined intervals; and transmitting remaining bits except for the punctured bits according to the modulation scheme.

[58] In accordance with another aspect of the present invention, an apparatus for encoding a channel in a communication system using a Low-Density Parity-Check (LDPC) code is provided. The apparatus includes a puncturing pattern applier for determining a number of parity bits for puncturing, dividing the parity bits at predetermined intervals, determining a number of puncturing parity bits, which are subjected to puncturing within the predetermined intervals, determining a modulation scheme, determining positions of puncturing parity bits corresponding to the determined number of the puncturing parity bits within the predetermined intervals according to the modulation scheme, and repeatedly performing puncturing on puncturing parity bits corresponding to the determined positions at the predetermined intervals; and a transmitter for transmitting remaining bits except for the punctured bits according to the modulation scheme.

[59] In accordance with further another aspect of the present invention, a method for decoding a channel in a communication system using a Low-Density Parity-Check (LDPC) code is provided. The method includes demodulating a signal transmitted from a transmitter; determining whether there are any punctured parity bits in the demodulated signal; determining positions of the punctured parity bits by estimating information about a puncturing pattern when there are punctured parity bits; and decoding data using the positions of the punctured parity bits. The information about the puncturing pattern includes a puncturing pattern obtained by considering a modulation scheme determined by the transmitter.

[60] In accordance with further another aspect of the present invention, an apparatus for decoding a channel in a communication system using a Low-Density Parity-Check (LDPC) code is provided. The apparatus includes a demodulator for demodulating a signal transmitted from a transmitter; a puncturing pattern estimator for determining whether there are any punctured parity bits in the demodulated signal, and determining positions of the punctured parity bits by estimating information about a puncturing pattern when there are punctured parity bits; and a decoder for decoding data using the positions of the punctured parity bits. The information about the puncturing pattern includes a puncturing pattern obtained by considering a modulation scheme determined by the transmitter.

[61] Other aspects, advantages, and salient features of the invention will become apparent to those skilled in the art from the following detailed description, which, taken in conjunction with the annexed drawings, discloses embodiments of the invention.

Advantageous Effects

[62] The embodiments of the present invention can generate a separate LDPC code with a different codeword length by optimizing encoding/decoding performance using in-

formation on a given parity-check matrix in the communication system that uses high-order modulation and LDPC codes.

Brief Description of Drawings

[63] The above and other aspects, features and advantages of certain exemplary embodiments of the present invention will be more apparent from the following description taken in conjunction with the accompanying drawings, in which:

[64] FIG. 1 illustrates an example of a parity-check matrix of a length-8 LDPC code;

[65] FIG. 2 illustrates a Tanner graph for a parity-check matrix of a length-8 LDPC code;

[66] FIG. 3 illustrates a DVB-S2 LDPC code;

[67] FIG. 4 illustrates an example of a parity-check matrix of a DVB-S2 LDPC code;

[68] (a) of FIG. 5 illustrates a signal constellation for QPSK modulation used in a digital communication system;

[69] (b) of FIG. 5 illustrates a signal constellation for 16-QAM modulation used in a digital communication system;

[70] (c) of FIG. 5 illustrates a signal constellation for 64-QAM modulation used in a digital communication system;

[71] FIG. 6 is a block diagram of a transceiver in a communication system using an LDPC code;

[72] FIG. 7 illustrates an example where random puncturing is applied to the LDPC code of FIG. 4;

[73] FIG. 8 illustrates another example where non-random puncturing is applied to the LDPC code of FIG. 4;

[74] FIG. 9 illustrates another example where non-random puncturing is applied to the LDPC code of FIG. 4;

[75] FIG. 10 illustrates another example of a parity-check matrix of a DVB-S2 LDPC code;

[76] FIG. 11 illustrates an example of a puncturing pattern determined by considering BPSK or QPSK transmission in the LDPC code of FIG. 10;

[77] FIG. 12 illustrates an example of a puncturing pattern determined by considering 16-QAM transmission in the LDPC code of FIG. 10;

[78] FIG. 13 illustrates an example of a puncturing pattern determined by considering 64-QAM transmission in the LDPC code of FIG. 10;

[79] FIG. 14 is a flowchart illustrating a method for generating an LDPC code with a different codeword length from a parity-check matrix of a stored LDPC code according to an embodiment of the present invention;

[80] FIG. 15 is a flowchart illustrating an LDPC decoding method in a reception apparatus according to an embodiment of the present invention;

[81] FIG. 16 is a block diagram of a transmission apparatus using a punctured/shortened LDPC code according to an embodiment of the present invention; and

[82] FIG. 17 is a block diagram of a reception apparatus using a punctured/shortened LDPC code according to an embodiment of the present invention.

[83] Throughout the drawings, the same drawing reference numerals will be understood to refer to the same elements, features and structures.

Mode for the Invention

[84] The following description with reference to the accompanying drawings is provided to assist in a comprehensive understanding of embodiments of the invention as defined by the claims and their equivalents. It includes various specific details to assist in that understanding but these are to be regarded as merely exemplary. Accordingly, those of ordinary skill in the art will recognize that various changes and modifications of the embodiments described herein can be made without departing from the scope and spirit of the invention. In addition, descriptions of well-known functions and constructions are omitted for clarity and conciseness.

[85] The terms and words used in the following description and claims are not limited to the bibliographical meanings, but, are merely used by the inventor to enable a clear and consistent understanding of the invention. Accordingly, it should be apparent to those skilled in the art that the following description of embodiments of the present invention are provided for illustration purpose only and not for the purpose of limiting the invention as defined by the appended claims and their equivalents.

[86] It is to be understood that the singular forms "a," "an," and "the" include plural referents unless the context clearly dictates otherwise. Thus, for example, reference to "a component surface" includes reference to one or more of such surfaces.

[87] Reliability difference in high-order modulation will first be described before a description of the present invention. Attention should be paid in designing an LDPC code because reliabilities of bits constituting high-order modulation symbols are different when high-order modulation is used in the communication system requiring LDPC codes with various codeword lengths, unlike in the communication system employing only Binary Phase Shift Keying (BPSK) or Quadrature Phase Shift Keying (QPSK).

[88] In order to explain the reliability difference in high-order modulation, a description of signal constellations for Quadrature Amplitude Modulation (QAM) which is high-order modulation commonly used in communication systems will be provided. A QAM-modulated symbol consists of a real part and an imaginary part, and various modulation symbols may be generated by differentiating magnitudes and signs of their real parts and imaginary parts. QAM will be described together with QPSK modulation to consider the details of QAM characteristics.

[89] (a) of FIG. 5 illustrates a signal constellation for general QPSK modulation.

[90] Referring to (a) of FIG. 5, y_0 determines a sign of a real part while y_1 determines a sign of an imaginary part. That is, a sign of the real part is plus (+) for $y_0=0$, and minus (-) for $y_0=1$. Also, a sign of the imaginary part is plus (+) for $y_1=0$, and minus (-) for $y_1=1$. Since y_0 and y_1 are equal in error occurrence probability as they are sign indication bits that indicate respective signs of the real part and the imaginary part, reliabilities of (y_0, y_1) bits corresponding to one modulation signal are equally important, in QPSK modulation. For $y_{0,q}$ and $y_{1,q}$, the second subscript index q indicates q^{th} outputs of bits constituting a modulation signal.

[91] (b) of FIG. 5 illustrates a signal constellation for general 16-QAM modulation.

[92] Referring to (b) of FIG. 5, the meaning of (y_0, y_1, y_2, y_3), corresponding to bits of one modulation signal, is as follows. Bits y_0 and y_2 determine a sign and a magnitude of the real part, respectively, while bits y_1 and y_3 determine a sign and a magnitude of the imaginary part, respectively. In other words, y_0 and y_1 determine signs of the real part and imaginary part of the modulation signal, while y_2 and y_3 determine magnitudes of the real part and imaginary part of the modulation signal. Because distinguishing a sign of a modulated signal is easier than distinguishing a magnitude of the modulated signal, y_2 and y_3 are higher than y_0 and y_1 in error occurrence probability. Therefore, in terms of non-error occurrence probabilities (i.e. reliabilities) of the bits, $y_0=y_1>y_2=y_3$. That is, bits (y_0, y_1, y_2, y_3) constituting a QAM modulation signal, unlike those of a QPSK modulation signal, have different reliabilities.

[93] In 16-QAM modulation, among the 4 bits constituting a signal, 2 bits determine signs of the real part and imaginary part of the signal and the remaining bits only need to determine magnitudes of the real part and imaginary part of the signal. Thus, orders of (y_0, y_1, y_2, y_3) and a role of each bit are subject to change.

[94] (c) of FIG. 5 illustrates a signal constellation for general 64-QAM modulation.

[95] Of (y_0, y_1, y_2, y_3, y_4, y_5), corresponding to the bits of one modulation signal, bits y_0, y_2 and y_4 determine a magnitude and a sign of the real part, and y_1, y_3 and y_5 determine a magnitude and a sign of the imaginary part. Here, y_0 and y_1 determine signs of the real part and the imaginary part, respectively, and a combination of y_2 and y_4 and a combination of y_3 and y_5 determine magnitudes of the real part and the imaginary part, respectively. Because distinguishing signs of a modulated signal are easier than distinguishing magnitudes of the modulated signal, reliabilities of y_0 and y_1 are higher than reliabilities of y_2, y_3, y_4, and y_5. The bits y_2 and y_3 are determined depending on whether a magnitude of the modulated symbol is greater or less than 4, and the bits y_4 and y_5 are determined according to whether the magnitude of the modulated symbol is closer to 4 or 0 with 2 centered there between, or closer to 4 or 8 with 6 centered there between. Thus, a range in which the magnitude is determined by y_2 and y_3 is 4, while a range for

y_4 and y_5 is 2. As a result, y_2 and y_3 are higher than y_4 and y_5 in reliability. In conclusion, $y_0=y_1>y_2=y_3>y_4=y_5$ in terms of non-error occurrence probabilities (i.e. reliabilities) of the bits.

[96] In 64-QAM modulation, of the 6 bits constituting a signal, 2 bits determine signs of the real part and imaginary part of the signal, and 4 bits only need to determine magnitudes of the real part and imaginary part of the signal. Accordingly, orders of (y_0, y_1, y_2, y_3, y_4, y_5) and a role of each bit are subject to change. Also, in a signal constellation of 256-QAM or higher, the roles and reliabilities of bits constituting a modulation signal are different as described above. A detailed description thereof will be omitted.

[97] Therefore, the present invention provides a method and apparatus for supporting LDPC codes with various codeword lengths suitable for high-order modulation, using a parity-check matrix of a structured LDPC code in a particular form. In addition, the present invention provides an apparatus for supporting various codeword lengths according to high-order modulation in a communication system using an LDPC code in a particular form, and a method for controlling the same. In particular, the present invention provides a method for generating an LDPC code using a parity-check matrix of a given LDPC code, the generated LDPC code being less than the given LDPC code, and an apparatus thereof.

[98] FIG. 6 is a block diagram of a transceiver in a communication system using an LDPC code.

[99] Referring to FIG. 6, a message u is input to an LDPC encoder 611 in a transmitter 610 before being transmitted to a receiver 630. The LDPC encoder 611 encodes the input message u, and outputs the encoded signal c to a modulator 613. The modulator 613 modulates the encoded signal c, and transmits the modulated signal s to the receiver 630 over a wireless channel 620. A demodulator 631 in the receiver 630 demodulates the received signal r, and outputs the demodulated signal x to an LDPC decoder 633. The LDPC decoder 633 finds an estimate

$\underline{u}$

of the message based on the data received through the wireless channel 620 by decoding the demodulated signal x.

[100] The LDPC encoder 611 generates a parity-check matrix according to a codeword length required by a communication system, using a preset scheme. Particularly, in accordance with an embodiment of the present invention, the LDPC encoder 611 may support various codeword lengths using the LDPC code without the separate need for additional stored information.

[101] In accordance with an embodiment of the present invention, a method of acquiring

various codeword lengths from a given LDPC code uses shortening or puncturing. The term "puncturing" as used herein indicates a method that does not transmit a specified part of an LDPC codeword after generating the LDPC codeword from a given particular parity-check matrix by performing LDPC encoding. Hence, a receiver determines that the non-transmitted bits were erased.

[102] For a better understanding of the puncturing, a parity-check matrix of the DVB-S2 LDPC code illustrated in FIG. 3 will be described in more detail below.

[103] Regarding the parity-check matrix of the DVB-S2 LDPC code illustrated in FIG. 3, its total length is N_1, K_1columns in the leading part of the parity-check matrix correspond to information bits

$$(i_0, i_1, \ldots, i_{K_1-1})$$

, and columns in the remaining rear part correspond to length-(N_1-K_1) parity bits

$$(p_0, p_1, \ldots, p_{N_1-K_1-1})$$

[104] Generally, the puncturing can be applied to both the information bits and the parity bits. Although the puncturing and the shortening commonly reduce codeword lengths, the puncturing, unlike the shortening, described herein above, does not limit values of particular bits. The puncturing is a method for simply not transmitting particular information bits or particular parts of generated parity bits, so that a receiver can erase the corresponding bits. In other words, by simply not transmitting bits in N_p predefined positions in a generated length-N_1 LDPC codeword, the puncturing can obtain the same effect as that obtained by transmitting a length-(N_1-N_p) LDPC codeword. Because columns corresponding to the bits punctured in the parity-check matrix are all used intact in a decoding process, with the columns erased, the puncturing is distinct from the shortening.

[105] Further, because position information for the punctured bits can be shared or estimated in common by the transmitter and the receiver when the system is set up, the receiver may merely erase the corresponding punctured bits, before decoding.

[106] In the puncturing technique, because a length of a codeword that the transmitter actually transmits is N_1-N_p and a length of an information word is constantly K_1, the code rate becomes $K_1/(N_1-N_p)$, which is always greater than the first given code rate K_1/N_1.

[107] A description will now be made of a shortening technique and a puncturing technique suitable for the DVB-S2 LDPC code. The DVB-S2 LDPC code, as described above, is an LDPC code having a particular structure. Therefore, compared with the normal LDPC code, the DVB-S2 LDPC code is able to undergo more efficient

shortening and puncturing.

[108] With reference to FIG. 4, a detailed description will be made of characteristics of a DVB-S2 LDPC code to which parity puncturing is applied. It is to be noted that for the DVB-S2 LDPC code of FIG. 4, N_1=30, K_1=15, M_1=5, and q=3, and weight-1 position sequences for 0th columns in three column groups are as follows:

[109] 0 1 2

[110] 0 11 13

[111] 0 10 14

[112] An ith weight-1 position sequence in an ith column sequentially represents information on the positions of rows with 1 in an ith column group.

[113] FIG. 7 illustrates an example where random puncturing is applied to the LDPC code of FIG. 4. Because the parity bits punctured in FIG. 7 are subjected to erasure processing at a decoder, the punctured parity bits, compared with the other non-erased bits, are not greater in a performance improvement effect in an LDPC decoding process, so their reliabilities decrease. Consequently, the other bits directly connected to the punctured parity bits, which are low in reliability, also suffer from a decrease in the performance improvement effect in the decoding process. The decrease in the performance improvement effect increases as the number of edges directly connected to the bits punctured on the Tanner graph increases.

[114] In FIG. 7, for example, a 0th information bit corresponding to a 0th column is directly connected to the punctured parity bit twice, a 3rd information bit corresponding to a 3rd column is directly connected to the punctured parity bit once, and an 8th information bit corresponding to an 8th column is directly connected to the punctured parity bit three times. In this case, the 3rd, 0th, and 8th information bits are superior in the performance improvement effect in order in the decoding process. In other words, when the degrees of the variable nodes are equal to each other, the performance improvement effect decreases as the number of the connected punctured bits increases.

[115] It can be appreciated from FIG. 7 that the numbers of punctured parity bits, which are directly connected to respective information bits, are random due to the random puncturing pattern. Therefore, there is a high probability that reliabilities of respective information bits will also be random. In other words, while some information bits may gain higher-than-needed decoding performance, other information bits may suffer significant performance degradation. This random puncturing pattern may lead to considerable irregularity of the reliabilities of the information bits in the decoding process.

[116] FIG. 8 illustrates a second example where non-random puncturing is applied to the LDPC code of FIG. 4. More specifically, a relatively non-random puncturing pattern in a particular form is applied in the example illustrated in FIG. 8.

[117] Referring to FIG. 8, even though the relatively non-random puncturing pattern is

applied, the connections to the information bits may be significantly irregular according to the corresponding puncturing pattern. The non-random puncturing pattern of FIG. 8 may be more irregular compared with the random puncturing pattern of FIG. 7.

[118] In case of the LDPC code with a parity-check matrix having a particular structure like the DVB-S2 LDPC code, the connections between the information bits and the parity bits punctured according to the puncturing pattern can be significantly changed.

[119] The embodiments of the present invention suggest a puncturing pattern that provides stable decoding performance by maximally suppressing the irregularity of the reliabilities of the information bits in the decoding process using the structural characteristics of the DVB-S2 LDPC code.

[120] FIG. 9 illustrates a third example where non-random puncturing is applied to the LDPC code of FIG. 4. In the example of FIG. 9, a puncturing pattern that maintains a constant interval of 3 between punctured parity bits from q=3, which is one of the constituent variables, is applied to the parity-check matrix illustrated in FIG. 4. As can be seen in FIG. 9, each of the information bits is equally and twice connected to the punctured bit.

[121] The irregularity between the punctured bits and information bits is remarkably reduced when the interval between the punctured parity bits is set according to the value of q due to the structure of the DVB-S2 LDPC code. This is better described with reference to FIG. 3.

[122] Referring to Rules 1 and 2 and FIG. 3, regarding each column group, positions of '1's in the first column in the corresponding column group determine positions of '1's in the remaining columns. Indexes of rows where 1 is located in the remaining columns differ exactly by a multiple of q from an index of a row where 1 is located in the first column, in regard to modulo (N_1-K_1), where N_1 denotes a length of an LDPC codeword and K_1 indicates a length of an information word. More specifically, indexes of rows where 1 is located in two consecutive columns in a particular column group differ from each other exactly by q, for modulo (N_1-K_1).

[123] Another characteristic of the DVB-S2 LDPC code lies in a submatrix corresponding to the parity part in the parity-check matrix. Referring to FIG. 3, the parity part has a structure of a lower triangular matrix in which 1 exists in all of diagonal parts, and in this structure, an ith parity bit corresponds to '1' located in an ith row.

[124] In light of the structural characteristic of the DVB-S2 LDPC code, assuming that particular parity bits are punctured, if parity puncturing is repeated exactly at intervals of q, the number of edges of information bits connected to the parity bits punctured in a particular column group is most regular. For example, assuming that an ith parity bit is punctured for $0 \le i < q$ and an $(i+kq)^{th}$ parity bit is repeatedly punctured for $0 \le k < M_1$, if a

certain information bit is connected to the ith parity bit, this indicates that '1' exists in an ith row for a column corresponding to the information bit. Therefore, it can be understood that '1' exists in the $(i+kq)^{th}$ row in a column corresponding to an information bit which is separated by k from the above information bit among the columns in a column group according to Rule 1 and Rule 2. As a result, the information bit is connected to the punctured $(i+kq)^{th}$ bit.

[125] For the DVB-S2 LDPC code, because degrees of variable nodes corresponding to the entire information word are equal to each other in one column group, and one or less of '1' is distributed in one row, when q-periodic puncturing is applied, the information bits corresponding to one column group are connected to a same number of punctured bits. Therefore, the connections between the punctured bits and the information bits become regular, so that stabilized decoding can be expected in the decoding process.

[126] As described so far, it can be appreciated that for the DVB-S2 LDPC code, the q-periodic puncturing technique can contribute to performance improvement by making the best use of the structural characteristics of the DVB-S2 LDPC code. However, to date, with regard to the optimized puncturing pattern obtained by considering the q-periodic puncturing, only the results obtained by setting BPSK or QPSK are known.

[127] In addition to the q-periodic puncturing method, there are known methods that optimize the performance according to the code rate or codeword length when applying shortening or puncturing to the general LDPC code. However, because the known existing methods of finding a shortening/puncturing pattern perform the optimization process considering only BPSK or QPSK, only one optimized shortening/puncturing pattern could exist for a given LDPC code.

[128] However, the optimized puncturing/shortening pattern obtained when high-order modulation is used and a signal constellation/bit mapping (bit mapping on the signal constellation) scheme has been determined, may differ from that in BPSK or QPSK modulation.

[129] In BPSK or QPSK modulation, because reliabilities of bits constituting a symbol are equal, reliabilities of codeword bits are also equal in the LDPC codeword after it underwent shortening or puncturing, so there is no need to consider a modulation scheme in the process of finding the shortening/puncturing pattern. However, as described above, in high-order modulation such as 16-QAM, 64-QAM and 256-QAM, because reliabilities of bits constituting a symbol are different, when the high-order modulation scheme and the signal constellation/bit mapping scheme are determined, reliabilities of codeword bits in the LDPC codeword after application of shortening or puncturing may be different from those before application of puncturing or shortening.

[130] FIG. 10 illustrates another example of a parity-check matrix of a DVB-S2 LDPC code.

[131] In FIG. 10, N_1=40, K_1=10, M_1=5, and q=6, and weight-1 position sequences for 0th columns in two column groups of an information word are as follows:

[132] 0 5 10 20 25

[133] 7 15 26

[134] An ith weight-1 position sequence in an ith column sequentially represents information on the positions of rows with 1 in an ith column group.

[135] Referring to FIG. 10, a degree of each column corresponding to the first column group is 5, and a degree of each column corresponding to the second column group is 3. Generally, as to an LDPC code, its performance improvement effect is excellent in a decoding process as the degrees increase. Thus, it is commonly expected that performance given after decoding bits corresponding to the first column group would be superior compared to that of the second column group.

[136] With reference to FIG. 11, a brief description will now be made of a puncturing pattern which is suitable when BPSK or QPSK modulation is applied to the LDPC code with a parity-check matrix of FIG. 10. In FIG. 11, y_0 and y_1 indicate each BPSK symbol, or indicate two bits constituting one QPSK symbol. Hence, y_0 and y_1 are equal in reliability on the signal constellation.

[137] Referring to FIG. 11, after a parity bit corresponding to a 5th column in a submatrix corresponding to an arbitrary parity bit is punctured, one parity bit is punctured four times at a period of q. Here, information bits corresponding to degree-5 columns are connected to punctured parity bits through 2 edges, and information bits corresponding to degree-3 columns are not connected to punctured parity bits on the Tanner graph.

[138] Generally, the bits connected to many punctured bits show a poor performance improvement effect in the decoding process. However, in FIG. 11, the degree-5 columns still have 3 edges which are not connected to the punctured bits, so the performance may not be significantly decreased in the decoding process. In addition, since information bits in the degree-3 columns are not directly connected to the punctured parity bits, significant performance degradation may not occur similarly in the decoding process.

[139] It is assumed herein that the degree-5 columns are greater than the degree-3 columns in terms of the performance improvement effect in the decoding process. However, this assumption is valid only for BPSK or QPSK, and cannot always be applied for general high-order modulation.

[140] For example, as illustrated in FIG. 12, 16-QAM modulation can be applied to the LDPC code with the parity-check matrix of FIG. 10. In FIG. 12, y_0 and y_1 indicate high-reliability bits that determine signs of a real part and an imaginary part in a 16-QAM symbol, respectively. That is, the reliability relationship between the bits is defined as $y_0 = y_1 > y_2 = y_3$.

[141] Referring to FIG. 12, degree-5 columns are mapped to y_3 and degree-3 columns are mapped to y_1. In other words, the degree-5 columns are mapped to a lower-reliability bit and the degree-3 are mapped to a higher-reliability bit on the signal constellation.

[142] In this case, it cannot be concluded that the degree-5 columns would have a higher performance improvement effect in the decoding process. The reasons are as follows. In light of the characteristics of the 16-QAM modulation, since the degree-5 columns are mapped to lower-reliability information in a signal received from a channel, their reliability improvement is made very slowly in the decoding process. On the other hand, the degree-3 columns, though they have a low degree, are mapped to lower-reliability information, so the reliability improvement effect occurs very fast.

[143] As described above, it cannot be guaranteed that the bits corresponding to the higher-degree columns always have superior performance in the LDPC code, to which high-order modulation is applied.

[144] Referring back to FIG. 12, in an implementation, after a parity bit corresponding to a 4th column in a submatrix corresponding to an arbitrary parity bit is punctured, one parity bit is punctured four times at a period of q. Here, information bits in both of degree-5 columns and degree-3 columns are connected to punctured parity bits through 1 edge on the Tanner graph.

[145] In the puncturing pattern applied in FIG. 11, the punctured bits are connected only to the degree-5 columns because the performance improvement effect of the degree-5 columns is high in BPSK or QPSK modulation. However, in the puncturing pattern illustrated in FIG. 12, the punctured bits are uniformly distributed considering the difference between reliabilities corresponding to each column group based on the modulation scheme. In an analysis of this case, since the degree-5 columns are connected to only one punctured bit, there is a high probability that no more significant performance degradation will happen. Also, though the degree-3 columns are connected to one punctured bit, they correspond to high-reliability information from a received signal, so the probability is high that the significant performance degradation will not occur.

[146] Similarly, even when 64-QAM modulation is applied to the LDPC code with the parity-check matrix of FIG. 10 as illustrated in fig. 14, the characteristics may be different from those of BPSK, QPSK and 16-QAM. In FIG. 13, y_0 and y_1 indicate high-reliability bits that determine signs of a real part and an imaginary part in a 64-QAM symbol, respectively. That is, reliability relationship between the bits is defined as $y_0 = y_1 > y_2 = y_3 > y_4 = y_5$.

[147] FIG. 13 illustrates an example of a puncturing pattern obtained by considering parity bits corresponding to degree-2 columns. In FIG. 12A for 16-QAM, though 3 bits among the punctured parity bits are connected to the lowest-reliability bits y_2 and y_3,

since the information bits corresponding to the degree-5 or degree-3 columns have good performance, no performance degradation may occur. However, in FIG. 13 where 64-QAM is applied, when too many parity bits are connected to y_4 and $y_5$having very low reliabilities, performance degradation may occur. Hence, the reliabilities corresponding to the parity bits should also be carefully considered.

[148] It should be noted in FIG. 12 and FIG. 13 that when the codeword length of the LDPC code decreases due to shortening or puncturing, orders of bits corresponding to the signal constellation are equal, but the bits decrease in a predetermined ratio. For example, in FIG. 12 and FIG. 13, for an LDPC code, orders (y_3, y_1, y_0, y_2, y_1, y_3, y_2, y_0) and (y_5, y_1, y_3, y_4, y_0, y_2, y_3, y_5, y_1, y_2, y_4, y_0) of bits corresponding to the signal constellations are maintained, but a ratio of bits corresponding to each signal constellation decreases in proportion to a length of the LDPC codeword.

[149] As described in FIGs. 10, 11, 12 and 13, it can be easily expected that the same puncturing pattern could be changed according to the modulation scheme. That is, when a high-order modulation scheme and a signal constellation/bit mapping scheme are determined for a given LDPC code, the optimal puncturing pattern is subject to change according to connections between punctured bits and non-punctured other bits. Thus, different puncturing patterns should be applied according to transmission modulation schemes, in order to minimize the performance degradation caused by puncturing.

[150] The general process for applying the above-described puncturing scheme can be summarized in 5 steps as follows. For convenience, it is assumed herein that N_l indicates a length of an LDPC codeword, each column group includes M_1 columns, and N_p parity bits are subject to puncturing. The following puncturing process is illustrated in fig. 14 in brief.

[151] Puncturing Step 1

[152] A transmission apparatus generates an existing shortened/non-shortened DVB-S2 LDPC codeword in step 1301.

[153] Puncturing Step 2

[154] The transmission apparatus determines the number N_p of parity bits for puncturing in step 1303, and finds

$$A = \left\lfloor \frac{N_p}{M_1} \right\rfloor$$

in step 1305, where

$$\lfloor x \rfloor$$

is the maximum integer which is less than or equal to x.

[155] Puncturing Step 3

[156] The transmission apparatus determines puncturing parity bits

$p_{i_0}, p_{i_1}, \ldots, p_{i_{A-1}}$.

for $0 \le x < A$ and $0 \le i_x < q$ according to a transmission modulation scheme in step 1307. It is assumed that for $0 \le x < q$, values of i_x were previously determined using a density evolution method considering the transmission modulation scheme(herein, a relationship of $A \le q$ is given).

[157] Puncturing Step 4

[158] The transmission apparatus applies puncturing to all parity bits

p_{i_x+kqB}

for $0 \le x < A$ and $0 \le k < M_1$ in step 1307. Here, the constant B is a preset non-zero integer.

[159] Puncturing Step 5

[160] The transmission apparatus additionally punctures the parity bits

p_{i_A+kqB}

for $0 \le k < N_p - AM_1$ in step 1307. Thereafter, the transmission apparatus transmits bits except for the punctured bits in step 1309.

[161] It can be understood from Puncturing Step 1 through Puncturing Step 5 that the puncturing pattern can be defined accurately when the number N_p of bits to be punctured, sequence information defining values of i_x, and a value of q are known.

[162] To describe detailed examples in which the above puncturing steps are performed according to modulation schemes, less than optimal (i.e. suboptimized) puncturing patterns for an DVB-S2 LDPC code with N_1=16200, K_1=7200, M_1=360, and q=25 are shown in Table 1A and Table 1B. A process of selecting the suboptimal puncturing patterns will be described in detail below.

[163] In Table 1A and Table 1B, $(p_0, p_1, p_2, \ldots, p_{8999})$ indicates all parity bits of the DVB-S2 LDPC code, which are enumerated in a row.

[164] Table 1A

[165]

Major variables of DVB-S2 LDPC code	N_1=16200, K_1=7200, M_1=360, q=25
Grouping of parity bits	Define a set P_j satisfying the following characteristics for $0 \le j < q = 25$: $P_j = \{p_k \mid k \equiv j \bmod 25,\ 0 \le k < 9000\}$. The set P_j is a set having 360 parity bits as its entries.
Range of N_p	Puncturing Method
$0 \le N_p < 9000$	For an integer $m = \left\lfloor \frac{N_p}{360} \right\rfloor$, puncture all of parity bits corresponding to m parity bit sets $P_{\pi(0)}, P_{\pi(1)}, \ldots, P_{\pi(m-1)}$, and additionally puncture (N_p-360m) parity bits from among the parity bits corresponding to $P_{\pi(m)}$. Here, π indicates a permutation function that is a puncturing pattern, and the relationships are shown at the bottom of the table.

[166] Table 1B

[167]

π(0)	π(1)	π(2)	π(3)	π(4)	π(5)	π(6)	π(7)	π(8)
π(9)	π(10)	π(11)	π(12)	π(13)	π(14)	π(15)	π(16)	π(17)
π(18)	π(19)	π(20)	π(21)	π(22)	π(23)	π(24)	-	-
Relationship between permutation functions suboptimized on BPSK/QPSK								
6	4	18	9	13	8	15	20	5
17	2	24	10	22	12	3	16	23
1	14	0	21	19	7	11	-	-
Relationship between permutation functions suboptimized on 16QAM								
6	4	13	9	18	8	15	20	5
17	2	24	22	14	23	3	19	10
1	12	0	16	21	7	11	-	-
Relationship between permutation functions suboptimized on 64QAM								
15	3	23	6	13	18	1	9	17
8	5	20	16	22	4	24	14	2
21	12	7	10	19	11	0	-	-

[168] Referring to Table 1A and Table 1B, it can be appreciated that when a length of parity bits to be punctured is determined, the puncturing process based on suboptimal

puncturing patterns is performed through a predetermined process regardless of the modulation scheme, but relationships between permutation functions indicating optimized puncturing patterns are all different according to modulation schemes. That is, when the puncturing method is applied without considering the modulation scheme, significant performance degradation may occur according to modulation schemes.

[169] From the puncturing process, it can also be appreciated that AM_1 parity bits are punctured in Puncturing Step 3 and Puncturing Step 4 and N_p-AM_1 parity bits are punctured in Puncturing Step 5, so that a total of N_p parity bits are punctured.

[170] The suboptimal puncturing patterns shown in Table 1A and Table 1B may not be unique according to conditions for finding the puncturing patterns. Because several selections are possible in the process of selecting the puncturing patterns, which will be described below in detail, many puncturing patterns showing good performance may be available. Actually, puncturing patterns shown in Table 2A and Table 2B can also provide very excellent performance, like the puncturing patterns defined in Table 1A and Table 1B.

[171] Table 2A

[172]

Major variables of DVB-S2 LDPC code	N_1=16200, K_1=7200, M_1=360, q=25
Grouping of parity bits	Define a set P_j satisfying the following characteristics for $0 \le j < q = 25$: $P_j = \{p_k \mid k \equiv j \bmod 25,\ 0 \le k < 9000\}$. The set P_j is a set having 360 parity bits as its entries.
Range of N_p	Puncturing Method
$0 \le N_p < 9000$	For an integer $m = \left\lfloor \frac{N_p}{360} \right\rfloor$, puncture all of parity bits corresponding to m parity bit sets $P_{\pi(0)}, P_{\pi(1)}, \ldots, P_{\pi(m-1)}$, and additionally puncture (N_p-360m) parity bits from among the parity bits corresponding to $P_{\pi(m)}$. Here, π indicates a permutation function that is a puncturing pattern, and the relationships are shown at the bottom of the table.

[173] Table 2B

[174]

π(0)	π(1)	π(2)	π(3)	π(4)	π(5)	π(6)	π(7)	π(8)
π(9)	π(10)	π(11)	π(12)	π(13)	π(14)	π(15)	π(16)	π(17)
π(18)	π(19)	π(20)	π(21)	π(22)	π(23)	π(24)	-	-
Relationship between permutation functions suboptimized on BPSK/QPSK								
6	4	18	9	13	8	15	20	5
17	2	24	10	22	12	3	16	23
1	14	0	21	19	7	11	-	-
Relationship between permutation functions suboptimized on 16QAM								
6	4	13	9	18	8	15	20	5
17	2	22	24	7	12	1	16	23
14	0	21	10	19	11	3	-	-
Relationship between permutation functions suboptimized on 64QAM								
6	15	13	10	3	17	21	8	5
19	2	23	16	24	7	18	1	12
20	0	4	14	9	11	22	-	-

[175] The method of mapping bits corresponding to the signal constellations used in 16-QAM and 64-QAM modulations of Table 2A and Table 2B is the results obtained by applying the same bit mapping schemes as those illustrated in FIG. 12 and FIG. 13.

[176] The DVB-S2 LDPC codeword transmitted after undergoing the puncturing is restored to its original signal from a received signal at a reception apparatus through a decoding process in fig. 15.

[177] Fig. 15 is a flowchart illustrating a reception method in a reception apparatus according to an embodiment of the present invention.

[178] Referring to fig. 15, a reception apparatus determines or estimates a puncturing/ shortening pattern from a received signal in step 1401. Thereafter, the reception apparatus determines in step 1403 whether there are any punctured or shortened bits. In the absence of punctured or shortened bits, the reception apparatus performs decoding in step 1409. However, when there are punctured or shortened bits, the reception apparatus provides the puncturing/shortening pattern to an LDPC encoder 1560, which will be described in connection with fig. 16, in step 1405.

[179] In step 1407, the LDPC encoder 1560 determines that punctured bits are erased bits

and determines that the probability that values of shortened bits will be zero (0) is 1. Thereafter, the LDPC encoder 1560 performs decoding in step 1409.

[180] In the puncturing process, q-periodic puncturing is applied to stabilize performance of the DVB-S2 LDPC code using structural characteristics of the DVB-S2 LDPC code.

[181] A most significant difference between the present invention and the prior art lies in considering reliability of the transmission modulation scheme when determining parity bits to be punctured in Puncturing Step 3. An example of a sequence selection procedure is provided here below to determine the bits to be punctured in the DVB-S2 LDPC code in Puncturing Step 3. The following selection procedure is subject to change, when applied to other LDPC codes.

[182] Selection Process 1

[183] Bits, which are connected, if possible, to a less number of information bits, are first determined.

[184] Selection Process 2

[185] Parity bits to be punctured, which exhibit the most asymptotic performance, are determined from the parity bits determined in Selection Process 1, using a density evolution analysis method that considers both a modulation scheme and degree distribution.

[186] Selection Process 3

[187] Based on the parity bits to be punctured, determined in Selection Process 2, Selection Process 1 and Selection Process 2 are repeated on the bits excluding the already selected bits to be punctured.

[188] Commonly, when the number N_p of bits to be punctured varies greatly, the puncturing patterns optimized based on the value of N_p may have no correlation with each other. In other words, in a system where the value of N_p varies greatly, all of the puncturing patterns optimized based on the value of N_p should be stored separately for optimized performance.

[189] However, although the puncturing patterns obtained by applying the above selection procedure are not guaranteed to be optimal for all cases, they would have relatively stable performance from one puncturing pattern having a regular rule, regardless of a change in the value of N_p, thereby securing the relatively stable performance and easy storage of the puncturing patterns.

[190] For example, supposing that orders of the parity bits to be punctured are set as P_1, P_2, ..., P_q, only a sequence indicating the orders of the parity bits may be stored to enable efficient puncturing for an arbitrary value of N_p through Puncturing Step 1 to Puncturing Step 5.

[191] The puncturing technique may contribute to an increase in a code rate because it can change a length of an LDPC codeword, and reduce the codeword length without

changing an information length. Preferably, the puncturing and the shortening can be applied together to obtain the code rate and codeword length needed in the system.

[192] Assuming, as described above, that a codeword length and an information length of an LDPC code, which is intended to be finally obtained from a given LDPC code with a codeword length N_1 and an information length K_1 through shortening and puncturing, are N_2 and K_2, respectively, if a definition of N_1-N_2=N and K_1-K_2=K is given, the LDPC code with a codeword length N_2 and an information length K_2 can be generated by shortening K bits and puncturing N_p (=N-K) bits from a parity-check matrix of the given LDPC code. In case of the generated LDPC code, for N>0 or K>0, since the code rate is

$$\frac{K_1 - K_s}{N_1 - N_s}$$

, the puncturing and shortening lengths can be set considering N_2 and

$$\frac{K_1 - K_s}{N_1 - N_s}$$

[193] fig. 16 is a block diagram of a transmission apparatus using a punctured/shortened LDPC code according to an embodiment of the present invention.

[194] Referring to fig. 16, a transmission apparatus includes a controller 1510, a shortening pattern applier 1520, an LDPC code parity-check matrix extractor 1540, an LDPC encoder 1560, and a puncturing pattern applier 1580.

[195] The LDPC code parity-check matrix extractor 1540 extracts an LDPC code parity-check matrix that underwent shortening. The LDPC code parity-check matrix can be extracted using a memory, can be given in the transmission apparatus, or can be generated by the transmission apparatus.

[196] The controller 1510 controls the shortening pattern applier 1520 to determine a shortening pattern according to an information length. The shortening pattern applier 1520 inserts bits with a value of 0 in the positions corresponding to shortened bits, or removes columns corresponding to the shortened bits from a parity-check matrix of a given LDPC code. The shortening pattern can determined by extracting a shortening pattern stored in a memory, generating a shortening pattern using a sequence generator (not shown), or obtaining a shortening pattern using a density evolution analysis algorithm for a parity-check matrix and a given information length.

[197] The shortening pattern applier 1520 is optional when shortening is not needed for the code. Further, the controller 1510 controls the puncturing pattern applier 1580 to determine and apply a puncturing pattern according to a modulation scheme and a length of puncturing bits.

[198] The puncturing pattern applier 1580 determines the number of parity bits for puncturing, divides the parity bits at predetermined intervals, determines the number of puncturing bits, which are subjected to puncturing within the predetermined intervals, determines a modulation scheme, determines positions of puncturing parity bits corresponding to the determined number of the puncturing bits within the predetermined intervals according to the determined modulation scheme, and repeatedly performs puncturing on the puncturing parity bits corresponding to the determined positions at the predetermined intervals. The predetermined intervals are determined by dividing a length of the parity bits by a length of one column group in a parity-check matrix.

[199] The remaining bits except for the punctured bits are transmitted to a receiver according to the modulation scheme through a transmission unit (not shown).

[200] The LDPC encoder 1560 performs encoding based on the LDPC code shortened by the controller 1510 and the shortening pattern applier 1520.

[201] fig. 17 is a block diagram of a reception apparatus according to an embodiment of the present invention, in which a signal transmitted from a communication system using a punctured/shortened DVB-S2 LDPC code is received, and restored to user-desired data.

[202] Referring to fig. 17, a reception apparatus includes a controller 1610, a shortening/puncturing pattern determination/estimation unit 1620, a demodulator 1630, and an LDPC decoder 1640.

[203] The demodulator 1630 receives and demodulates a shortened/punctured LDPC code, and provides the demodulated signal to the shortening/puncturing pattern determination/estimation unit 1620 and the LDPC decoder 1640.

[204] The shortening/puncturing pattern determination/estimation unit 1620, under the control of the controller 1610, estimates or determines information about a puncturing/shortening pattern of the LDPC code from demodulated signal, and provides position information of the punctured/shortened bits to the LDPC decoder 1640. The shortening/puncturing pattern determination/estimation unit 1620 can determine or estimate the puncturing/shortening pattern by extracting a puncturing/shortening pattern stored in a memory, generating a puncturing/shortening pattern using a previously implemented generation method, or obtaining a puncturing/shortening pattern using a density evolution analysis algorithm for a parity-check matrix and a given information length. The LDPC decoder 1640 performs erasure processing on the punctured bits and performs decoding thereon.

[205] When the transmission apparatus applies both shortening and puncturing, the shortening/puncturing pattern determination/estimation unit 1620 in the reception apparatus may carry out pattern determination/estimation on the shortening first, perform pattern determination/estimation on the puncturing first, or make pattern de-

termination/estimation on both the shortening and puncturing. The shortening/ puncturing pattern determination/estimation unit 1620 determines presence/absence of puncturing bits in the demodulated signal. When there are puncturing bits, the shortening/puncturing pattern determination/estimation unit 1620 determines positions of the punctured parity bits by estimating information about the puncturing pattern.

[206] The LDPC decoder 1640 decodes data using the determined positions of the punctured parity bits, assuming that the probability that the punctured bits would be zero (0) and the probability that the punctured bits would be 1 are equal to 1/2. Because the probability that values of the shortened bits will be zero is 1 (i.e. 100%), the LDPC decoder 1640 determines whether or not it will allow the shortened bits to take part in its decoding operation depending on the value 1 of the probability that the shortened bits would be zero. When the LDPC decoder 1640 receives information on a length of the shortened DVB-S2 LDPC code by means of the shortening/puncturing pattern determination/estimation unit 1620, the LDPC decoder 1640 restores the user-desired data from the received signals.

[207] As described in connection with fig. 16, the shortening is performed in the input stage of the LDPC encoder 1560 and the puncturing is performed at the output stage of the LDPC encoder 1560. However, in the reception apparatus illustrated in fig. 17, the LDPC decoder 1640 should have information on the puncturing and the shortening simultaneously, to make the decoding possible.

[208] While the invention has been shown and described with reference to a certain exemplary embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims and their equivalents.

Claims:

1. A method for channel decoding using a Low-Density Parity-Check (LDPC) code, the method comprising:

demodulating a signal transmitted from a transmitter;

determining position information of punctured parity bits by estimating information about a predetermined order of parity bit sets to be punctured and the number of parity bit sets; and

decoding data using the positions of the punctured parity bits,

wherein determining position information of punctured parity bits comprises:

determining a number of parity bits to be punctured;

determining a number of parity bit sets to be punctured based on the determined number of parity bits to be punctured; and

acquiring a predetermined order of parity bit sets.

2. The method of claim 1, wherein the predetermined order of parity bit sets to be punctured is determined as 6, 4, 13, 9, 18, 8, 15, 20, 5, 17, 2, 22, 24, 7, 12, 1, 16, 23, 14, 0, 21, 10, 19, 11, 3, when a codeword length is 16200 and an information length is 7200, a modulation scheme is 16-Quadrature Amplitude Modulation (16-QAM).

3. The method of claim 1, wherein the predetermined order of parity bit sets to be punctured is determined as 6, 15, 13, 10, 3, 17, 21, 8, 5, 19, 2, 23, 16, 24, 7, 18, 1, 12, 20, 0, 4, 14, 9, 11, 22, when a codeword length is 16200 and an information length is 7200, a modulation scheme is 64 Quadrature Amplitude Modulation (64-QAM).

4. The method of claim 1, wherein the step of determining positions of the punctured parity bits, comprises:

additionally determining positions of the remaining punctured parity bits when the number of the punctured bits is not a multiple of the number of parity bit sets.

5. The method of claims 1, wherein the number of parity bit sets is determined by below equation:

$$A = \left\lfloor \frac{N_p}{M_1} \right\rfloor,$$

where A denotes the number of parity bit sets for puncturing, N_p denotes a number of parity bits for puncturing, M_1 denotes the number of bits in one parity bit set.

6. The method of claims 5, wherein the parity bit sets are formed by below equation;

$$P_j=\{p_k \mid j \equiv k \bmod q,\ 0 \le k < N_1 - K_1\},$$

where P_j denotes the jth parity bit set, N_1 denotes a length of an LDPC codeword, K_1 denotes a length of an information word, M_1 denotes the number of bits in one parity bit set, q is a value satisfying $q = (N_1 - K_1) / M_1$, where K_1/M_1 is an integer, and $0 \le j < q$.

7. An apparatus for channel decoding using a Low-Density Parity-Check (LDPC) code, the method comprising:

a demodulator for demodulating a signal transmitted from a transmitter;

a puncturing pattern estimator for determining position information of punctured parity bits by estimating information about a predetermined order of parity bit sets to be punctured and the number of parity bit sets; and

a decoder for decoding data using the positions of the punctured parity bits,

wherein determining position information of punctured parity bits comprises:

determining a number of parity bits to be punctured;

determining a number of parity bit sets to be punctured based on the determined number of parity bits to be punctured; and

acquiring a predetermined order of parity bit sets.

8. The apparatus of claim 7, wherein the predetermined order of parity bit sets to be punctured is determined as 6, 4, 13, 9, 18, 8, 15, 20, 5, 17, 2, 22, 24, 7, 12, 1, 16, 23, 14, 0, 21, 10, 19, 11, 3, when a codeword length is 16200 and an information length is 7200, a modulation scheme is 16-Quadrature Amplitude Modulation (16-QAM).

9. The apparatus of claim 7, wherein the predetermined order of parity bit sets to be punctured is determined as 6, 15, 13, 10, 3, 17, 21, 8, 5, 19, 2, 23, 16, 24, 7, 18, 1, 12, 20, 0, 4, 14, 9, 11, 22, when a codeword length is 16200 and an information length is 7200, a modulation scheme is 64 Quadrature Amplitude Modulation (64-QAM).

10. The apparatus of claim 7, wherein the puncturing pattern estimator is adapted to additionally determine positions of the remaining punctured parity bits when the number of the punctured bits is not a multiple of the number of parity bit sets.

11. The apparatus of claims 7, wherein the number of parity bit sets is determined by below equation:

$$A = \left\lfloor \frac{N_p}{M_1} \right\rfloor,$$

where A denotes the number of parity bit sets for puncturing, N_p denotes a number of parity bits for puncturing, M_1 denotes the number of bits in one parity bit set.

12. The apparatus of claims 11, wherein the parity bit sets are formed by below equation;

$$P_j=\{p_k \mid j \equiv k \bmod q,\ 0 \le k < N_1 - K_1\},$$

where P_j denotes the jth parity bit set, N_1 denotes a length of an LDPC codeword, K_1 denotes a length of an information word, M_1 denotes the number of bits in one parity bit set, q is a value satisfying $q = (N_1 - K_1) / M_1$, where K_1/M_1 is an integer, and $0 \le j < q$.

13. A method for channel decoding, substantially as herein described with reference to the accompanying drawings.

14. An apparatus for channel decoding, substantially as herein described with reference to the accompanying drawings.