PIXEL CELL HAVING A GRATED INTERFACE

FIELD OF THE INVENTION

[0001] The present invention relates generally to imaging devices, and particularly to a pixel cell having a grated interface, and a method of forming the pixel cell having a grated interface.

BACKGROUND OF THE INVENTION

[0002] Integrated circuits, including dies, for example, imager dies such as charge-coupled-devices (CCD) and complementary metal oxide semiconductor (CMOS) dies, have commonly been used in photo-imaging applications.

[0003] Imager dies, such as the CMOS imager die, typically contain thousands of pixels in a pixel array on a single chip. Pixels convert light into an electrical signal that can then be stored and recalled by an electrical device such as, for example, a processor. The electrical signals that are stored may be recalled to produce an image on, for example, a computer screen or a printable media.

[0004] Exemplary CMOS imaging circuits, processing steps thereof, and detailed descriptions of the functions of various CMOS elements of an imaging circuit are described, for example, in U.S. Patent No. 6,140,630, U.S. Patent No. 6,376,868, U.S. Patent No. 6,310,366, U.S. Patent No. 6,326,652, U.S. Patent No. 6,204,524, and U.S. Patent No. 6,333,205, each of which being assigned to Micron Technology, Inc. The disclosures of each of the forgoing patents are hereby incorporated by reference in their entirety.

[0005] FIG. 1 illustrates a block diagram of an imager die 10, having a CMOS imager device 8 formed therein. The CMOS imager device 8 has a pixel array 15 that comprises a plurality of pixels arranged in a predetermined number of columns and rows. The pixel cells of each row in the pixel array 15 are all turned on at the same time by a row select line, and the pixel cells of each column are selectively output by respective column select lines. A plurality of row and column lines is provided for the entire pixel array 15. The row lines are selectively activated in sequence by a row driver 1 in response to a row address decoder 2 and the column select lines are selectively activated in sequence for each row activation by a column driver 3 in response to a column address decoder 4. The CMOS imager device 8 is operated by the control circuit 5, which controls the address decoders 2, 4 for selecting the appropriate row and column lines for pixel readout, and row and column driver circuitry 1, 3 for applying driving voltages to the drive transistors of the selected row and column lines.

[0006] The pixel output signals typically include a pixel reset signal V_{rst} taken from a charge storage node when it is reset and a pixel image signal V_{sig}, which is taken from the storage node after charges generated by an image are transferred to the node. The V_{rst} and V_{sig} signals are read by a sample and hold circuit 6 and are subtracted by a differential amplifier 7 that produces a difference signal ($V_{rst} - V_{sig}$) for each pixel cell, which represents the amount of light impinging on the pixels. This difference signal is digitized by an analog-to-digital converter (ADC) 9. The digitized pixel difference signals are then fed to an image processor 11 to form and output a digital image. In addition, as depicted in FIG. 1, the CMOS imager device 8 may be included on a single semiconductor chip to form the imager die 10.

[0007] A partial cross-sectional view of a conventional pixel cell 13 that could be incorporated into the pixel array 15 of FIG. 1 is illustrated in FIG. 2. The illustrated

pixel cell 13 typically includes a photosensor 12 having a p-region 12a and n-region 12b in a p-type substrate 14. The substrate 14 is typically a p-type silicon substrate. The p-region 12a of the photosensor 12 is typically coupled to the potential of the p-substrate 14 for efficient operation of the photosensor 12. The pixel cell 13 also includes a transfer transistor with associated gate 16, a floating diffusion region 18 formed in a more heavily doped p-type well 20, and a reset transistor with associated gate 22. The reset transistor 22 has an associated source/drain region 30 connected to a supply voltage Vaa-pix that is used to reset the floating diffusion region 18 to a predetermined charge level (i.e., supply voltage Vaa-pix level) prior to charge transference.

[0008] In operation, incident light 36 from a light source 38 striking the surface of the p-region 12a of the photosensor 12 generates electrons that are collected in the n-region 12b. When the transfer gate 16 is on, the generated electrons in the n-region 12b are transferred to the floating diffusion region 18 as a result of the potential difference existing between the photosensor 12 and the floating diffusion region 18. The floating diffusion region 18 is coupled to the gate of a source follower transistor 24, which receives the charge stored by the floating diffusion region 18 and transfers a voltage corresponding to the charge to a first source/drain terminal of a row select transistor 26. When a row select control signal RS goes high, the voltage corresponding to the generated charge is transferred to the column line 28 where it is further processed by sample/hold and processing circuits such as the sample and hold circuit 6 (FIG. 1).

[0009] The illustrated pixel cell 13 is formed between two isolation regions, or shallow trench isolation (STI) regions 32. The STI regions 32 prevent crosstalk between adjacent pixels, as pixel cell 13 is only one of hundreds or thousands of pixels that can be incorporate into the pixel array of an imager die (e.g., pixel array 15 of imager die 10 (FIG. 1)).

[0010] The pixel cell 13 is typically formed with an oxide layer 34 over the surface of the substrate 14. Various other layers (not shown) are typically deposited over the pixel cell 13. For example, a tetraethyl orthosilicate ($Si(OC_2H_5)_4$) (TEOS) layer may be deposited over the oxide layer 34. Similarly, a boro-phospho-silicate glass (BPSG) layer could be deposited over the TEOS layer. A metallization layer and insulating layer can also be deposited over the pixel cell 13.

[0011] One adverse effect of depositing the oxide layer 34 over the substrate 14 is the reflection of incident light 36. In operation, incident light 36 from the light source 38 encounters the oxide layer 34 before striking the p-region 12a of the photosensor 12. The index of refraction for the oxide layer can be as low as 1.6; whereas the index of refraction of the substrate 14 (formed of silicon) can be as high as 4.0. The abrupt transition from an index of refraction of 1.6 to 4.0 results in a high percentage of incident light reflection 40. The percentage of incident light 36 that is reflected can be determined using the following formula:

(1) $$\text{Reflection} = |X-Y|^2 / (X+Y)^2;$$

wherein X represents the index of refraction of the oxide layer 34, and Y represents the index of refraction of the substrate 14. In the above-described example, the reflection percentage is $|4.0-1.6|^2 / (4.0+1.6)^2 \sim 18\%$. Therefore, the photosensor 12 fails to capture approximately 18% of the incident light 36 to which it is exposed. This is undesirable.

[0012] Accordingly, there is a desire and need for a pixel cell that can capture a greater percentage of incident light by reducing the percentage of incident light that is reflected.

BRIEF SUMMARY OF THE INVENTION

[0013] The present invention provides a pixel cell that can capture a greater percentage of incident light, as compared to conventional pixels.

[0014] The present invention relates to a pixel cell having a photosensor within a silicon substrate and an oxide layer provided over the photosensor, wherein the oxide layer has a grated interface with the silicon substrate. The grated interface allows a greater percentage of incident light to be captured, which is a vast improvement over the art.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] The above-described features and advantages of the invention will be more clearly understood from the following detailed description, which is provided with reference to the accompanying drawings in which:

[0016] FIG. 1 illustrates a block diagram of a CMOS imager die;

[0017] FIG. 2 illustrates a partial cross-sectional view of a conventional pixel cell;

[0018] FIG. 3 illustrates a partial cross-sectional view of a pixel cell constructed in accordance with an exemplary embodiment of the invention;

[0019] FIG. 4 illustrates a magnified portion of the photosensitive region of the FIG. 3 pixel cell;

[0020] FIGS. 5A and 5B are graphs illustrating the percentage of reflection as a function of varying the depths of the trenches forming the basis of a grated interface and the periods of the grated interface.

[0021] FIGS. 6-8 illustrate stages in fabrication of the FIG. 4 photosensitive region;

[0022] FIG. 9 illustrates a partial cross-sectional view of a pixel cell constructed in accordance with a second exemplary embodiment of the invention;

[0023] FIGS. 10 and 11 illustrate a partial cross-sectional view of a pixel cell constructed in accordance with a third exemplary embodiment of the invention;

[0024] FIG. 12 illustrates a partial cross-sectional view of a pixel cell constructed in accordance with a fourth exemplary embodiment of the invention; and

[0025] FIG. 13 is a schematic diagram of a processor system constructed in accordance with an exemplary embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0026] In the following detailed description, reference is made to the accompanying drawings, which form a part hereof and show by way of illustration specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized, and that structural, logical, and electrical changes may be made without departing from the spirit and scope of the present invention. The progression of processing steps described is exemplary of embodiments of the invention; however, the sequence of steps is not limited to that set forth herein and may be changed as is known in the art, with the exception of steps necessarily occurring in a certain order.

[0027] The terms "semiconductor substrate," "silicon substrate," and "substrate" are to be understood to include any semiconductor-based structure. The semiconductor

structure should be understood to include silicon, silicon-on-insulator (SOI), silicon-on-sapphire (SOS), silicon-germanium, doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. When reference is made to the substrate in the following description, previous process steps may have been utilized to form regions or junctions in or over the base semiconductor or foundation.

[0028] The term "pixel," as used herein, refers to a photo-element unit cell containing a photosensor for converting photons to an electrical signal. For purposes of illustration, a single representative pixel and its manner of formation are illustrated in the figures and description herein; however, typically fabrication of a plurality of like pixels proceeds simultaneously. Accordingly, the following detailed description is not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims.

[0029] The terms "grated interface" or "grating," as used herein, refer to an interface between two material layers, wherein one of the two material layers has at least one trench, and the other of the two material layers is provided within and over the at least one trench.

[0030] Referring now to the figures, where like reference numbers designate like elements, FIG. 3 illustrates an exemplary pixel cell 113 constructed in accordance with an embodiment of the invention. Pixel cell 113 is similar to the FIG. 2 pixel cell 13 with the significant improvement of having a grated interface 135 between an oxide layer 134 and a photosensitive region 152 of the substrate 114 containing a photosensor 112.

[0031] The grated interface 135 of the pixel cell 113 serves to create a hybrid index of refraction between the oxide layer 134 and the substrate 114. In contrast to the FIG. 2

pixel cell 13, when incident light 36 strikes the pixel cell 113, the light does not meet an abrupt transition in the indexes of refraction between the oxide layer 34 (FIG. 2) and the substrate 14 (FIG. 2). Rather, the hybrid index of refraction is higher than that of the oxide layer 134, but lower than that of the silicon substrate 114, thereby decreasing the percentage of incident light reflection 40 (FIG. 2) found in the conventional pixel cell 13 (FIG. 2).

[0032] FIG. 4 illustrates a magnified portion of the photosensitive region 152 (including photosensor 112) of the FIG. 3 pixel cell 113. FIG. 4 illustrates that the oxide layer 134 is provided within and over trenches 144 formed within the substrate 114, thereby forming the grated interface 135. Each grating (measured as the distance from the beginning of one trench 144 to the beginning of the next trench 144 (shown by arrow G)) has a predetermined period that is represented by Λ. The predetermined period Λ of the grating G may be in the range from about 100 nm to about 1000 nm. The trenches 144 also have a predetermined depth, represented by d. The depth d of the trench 144 should be in the range from about 10 nm to about 250 nm.

[0033] It should be noted that the foregoing ranges are only exemplary embodiments of the present invention, and are not limiting in any way. For example, the gratings could have periods Λ longer than 1000 nm or shorter than 100 nm. Similarly, the depth d of the trenches 144 could be deeper than 250 nm or shallower than 10 nm. The actual periods Λ and depths d can be optimized for the particular wavelength of the incident light that is intended to be captured by the photosensor 112. Although illustrated as semi-rectangular, the trenches 144 of FIG. 4 are not so limited. Rather, the actual dimensions of the trenches 144 are dependent upon the intended application.

[0034] FIGS. 5A and 5B are graphs that represent the percentage of reflection of incident light 36 (FIG. 3) as a function of varying the period Λ of the gratings and depth d of the trenches of the exemplary embodiments of the invention. FIG. 5A illustrates the percentage of incident light reflection as a function of varying the period Λ of the grating in the pixel cell 113 of the invention. As illustrated in FIG. 5A, the grating has a constant depth d equal to 100 nm. The percentage of incident light reflection is approximately 18% with no grating, as discussed above with respect to FIG. 2. The percentage of incident light reflection continues to be high where the period Λ is 1000 nm. As the period Λ of the grating is decreased, however, the percentage of incident light reflection is nearly eliminated at a period Λ of 340 nm. As the grating is further decreased, the percentage of incident light reflection increases.

[0035] FIG. 5B illustrates the percentage of incident light reflection as a function of the depth d of the trenches 144 (FIG. 4). As illustrated, the grating has a constant period Λ equal to 340 nm. The incident light reflection decreases as the depth of the trenches 144 (FIG. 4) increases, and is nearly eliminated when the trenches have a depth d of 100 nm. As the depth of the trenches increases after 100 nm, however, the percentage of incident light reflection increases as well. Therefore, the actual periods Λ and depths d could be varied depending upon the desired amount of reflection.

[0036] FIGS. 6-8 illustrate stages of an exemplary method of forming the FIG. 4 photosensitive region 152. FIG. 6 illustrates a photosensor 112 formed within a silicon substrate 114. The photosensor 112 has a first doped region 112a and second doped region 12b formed in the substrate 114. The first doped region 112a of the photosensor 112 is typically coupled to the potential of the substrate 114 for efficient operation. For example, if the substrate 114 is a p-type substrate, the first doped region 112a is typically a p-region. Conversely, the second doped region 112b is typically the other of a p-type or n-type region. For example, if the substrate 114 is a p-type substrate, then

the second doped region 112b is typically an n-type region. It should be noted that the foregoing example is not limiting in any way. For example, the first doped region 112a and the substrate 114 could be doped with n-type dopants, and the second doped region 112b could be doped with a p-type dopant.

[0037] Although illustrated as a photodiode, the photosensor 112 is not intended to be limited in any way. For example, the photosensor 112 could be any photosensitive region capable of converting photons from incident light into electrical charges that can be stored and recalled.

[0038] FIG. 7 illustrates a plurality of trenches 144 formed within the silicon substrate over the photosensor 112. The trenches 144 could be formed by chemical etching, reactive ion etching (RIE), or other techniques for creating a recess in the silicon substrate 114. It should be noted that the foregoing methods of creating the trenches 144 that form the basis for the grated interface are not limiting in any way. For example, the trenches 144 could also be formed by laying a photoresist pattern on the silicon substrate, and creating columns of silicon substrate material by epitaxial growth, where a trench 144 is formed between each of the silicon substrate material columns.

[0039] FIG. 8 illustrates the oxide layer 134 provided over and within the trenches 144, thereby creating the grated interface G having a predetermined period Λ and having a predetermined depth *d*.

[0040] It should be noted that FIGS. 6-8 illustrate only one exemplary method of forming the pixel cell 113, and that the method is not intended to be limiting. For example, the plurality of trenches 144 could be formed prior to forming the photosensor 112 (i.e., before the doping steps described above). It should also be noted that various material layers (not shown) may be deposited over the oxide layer 134. For example, a

tetraethyl orthosilicate ($Si(OC_2H_5)_4$) (TEOS) layer may be deposited over the oxide layer 134. Similarly, a boro-phospho-silicate glass (BPSG) layer could be deposited over the TEOS layer. A metallization layer and insulating layer can also be deposited over the oxide layer 134.

[0041] FIG. 9 illustrates a second exemplary embodiment of the present invention. Pixel cell 213 is similar to the FIG. 3 pixel cell 113, with the exception that a material layer 150 has a grated interface 155 with the oxide layer 134. The grated interface 155 may further decrease the abrupt transition that the incident light 136 (FIG. 3) may encounter as it moves through the material layer 150 to the oxide layer 134. The material layer 150 may have a disparately high or low index of refraction relative to the oxide layer 134, which may result in a high percentage of incident light reflection 40 (FIG. 2). The grated interface may increase the amount of incident light 36 (FIG. 3) that is captured by the photosensor 112.

[0042] FIGS. 10 and 11 illustrate a partial cross-section of a pixel cell 313 constructed in accordance with a third exemplary embodiment of the invention. The FIG. 10 pixel cell 313 is similar to the FIG. 3 pixel cell 113 with the exception that the trenches forming the basis for the grated interface 235 between a silicon substrate 214 and an oxide layer 234 have a blazed (or step-wise) shape, rather than the semi-rectangular shape of the grated interface 135 of the FIG. 3 pixel cell 113. The blazed grating over a photosensitive region 252 of the pixel cell 313 provides for a further decrease in the disparity of indexes of refraction between the oxide layer 234 and the silicon substrate 214. The illustrated blazed interface 235 between the oxide layer 234 and the silicon substrate 214 achieves up to a 30% decrease in the incident light reflected, or a 30% increase in incident light 36 captured by the photosensor 112.

[0043] FIG. 11 illustrates a magnified portion of the photosensitive region 252 of the FIG. 10 pixel cell 313. The silicon substrate 214 has a plurality of trenches 244. The trenches 244 could be formed by any of the methods described above with respect to FIG. 4 (e.g., etching or epitaxial growth). Each of the illustrated trenches 244 has at least three sidewall regions 244a, 244b, 244c. The illustrated trench 244 has a first sidewall region 244a having a predetermined depth represented by d'. The trench 244 also has a second sidewall region 244b having a predetermined depth represented by d''. The predetermined depth d'' of the second sidewall region 244b could have a value less than, equal to, or greater than the depth d' of the first sidewall region 244a. The third sidewall region 244c typically has a predetermined depth represented by d'''. The depth d''' of the third sidewall region 244c typically has a value equal to the depths of the first and second sidewall regions 244a, 244b combined (i.e., $d' + d'' = d'''$). The predetermined depths d', d'', d''' may have a value in the range from about 10 nm to about 250 nm.

[0044] The grating (or the distance from the beginning of one trench to the beginning of the next trench (shown as arrow G')) has a predetermined period that is represented by Λ'. The predetermined period Λ' of the grating G' may be in the range from about 100 nm to about 1000 nm.

[0045] It should be noted that the foregoing ranges are only exemplary embodiments of the present invention, and are not limiting in any way. For example, the gratings G' could have periods Λ longer than 1000 nm or shorter than 100 nm. Similarly, the depths d', d'', d''' of the trenches 244 could be deeper than 250 nm or shallower than 10 nm. The actual periods Λ' and depths d', d'', d''' can be manipulated depending on the intended application.

[0046] FIG. 12 illustrates a pixel cell 413 constructed in accordance with a fourth exemplary embodiment of the invention. The pixel cell 413 has a pinned photodiode 212 having a first doped region 212a and a second doped region 212b, formed below the surface of a substrate 314. The illustrated pixel cell 413 is otherwise similar to the FIG. 3 pixel cell 113 (including the grated interface 135).

[0047] The pixel cells 113, 213, 313, 413 of the invention may be combined with peripheral circuitry on an imager die similar to that illustrated in FIG. 1. For example, the pixel array 15 of the FIG. 1 imager die could include one or more of the pixel cells 113, 213, 313, 413 constructed in accordance with exemplary embodiments of the invention. The imager die having a pixel array with one or more pixel cells 113, 213, 313, 413 of the invention could be included in an imaging device. The imaging device could further be incorporated into a processor system 1100 illustrated in FIG. 13. Examples of processor based systems include, without limitation, computer systems, camera systems, scanners, machine vision systems, vehicle navigation systems, video telephones, surveillance systems, auto focus systems, star tracker systems, motion detection systems, image stabilization systems, and data compression systems for high-definition television, any of which could utilize the invention.

[0048] The system 1100 includes an imaging device 1108 including an imager die having the overall configuration depicted in FIG. 1 with at least one pixel cell of the pixel array 15 (FIG. 1) constructed in accordance with any of the various embodiments of the invention (e.g., pixel cells 113, 213, 313, 413). The system 1100 generally comprises a central processing unit (CPU) 1102, such as a microprocessor, that communicates with an input/output (I/O) device 1106 over a bus 1104. Imaging device 1108 also communicates with the CPU 1102 over the bus 1104. The system 1100 also includes random access memory (RAM) 1110, and can include removable memory 1115, such as flash memory, which also communicates with CPU 1102 over the bus 1104.

Imaging device 1108 may be combined with a processor, such as a CPU, digital signal processor, or microprocessor, with or without memory storage on a single integrated circuit or on a different chip than the processor.

[0049] It should be noted that although the invention has been described with specific references to CMOS pixel cells having a grated interface between the silicon substrate and the oxide layer, the invention has broader applicability and may be used in any imaging apparatus. For example, the present invention may be used in conjunction with charge-coupled-device (CCD) imagers. The above description and drawings illustrate preferred embodiments which achieve the objects, features, and advantages of the present invention. Although certain advantages and preferred embodiments have been described above, those skilled in the art will recognize that substitutions, additions, deletions, modifications and/or other changes may be made without departing from the spirit or scope of the invention. Accordingly, the invention is not limited by the foregoing description but is only limited by the scope of the appended claims.

Claims:

1. A pixel cell comprising:

a photosensor within a silicon substrate comprising at least two trenches; and

an oxide layer comprising at least two trenches provided over said photosensor, said oxide layer trenches and said substrate trenches defining a grated interface to reduce the reflection of incident light.

2. The pixel cell of claim 1, wherein said grated interface is a semi-rectangular grating.

3. The pixel cell of claim 2, wherein said semi-rectangular grating has a period within a range from about 100 nm to about 1000 nm.

4. The pixel cell of claim 3, wherein said grating has a period of 340 nm.

5. The pixel cell of claim 2, wherein said semi-rectangular grating has a depth within a range from about 10 nm to about 250 nm.

6. The pixel cell of claim 5, wherein said grating has a depth of 100 nm.

7. The pixel cell of claim 1, wherein said grated interface is a blazed grating.

8. The pixel cell of claim 7, wherein said blazed grating has a period within a range of about 100 nm to about 1000 nm.

9. The pixel cell of claim 7, wherein said blazed grating has trenches having a first depth and second depth.

10. The pixel cell of claim 9, wherein said first and second depths have a depth within a range from about 10 nm to about 250 nm.

11. The pixel cell of claim 1, wherein said photosensor is a photodiode.

12. The pixel cell of claim 11, wherein said photosensor is a photodiode having first and second doped regions.

13. The pixel cell of claim 12, wherein said first doped region is a p-type region.

14. The pixel cell of claim 13, wherein said second doped region is an n-type region.

15. The pixel cell of claim 11, wherein said photosensor is a pinned photodiode.

16. The pixel cell of claim 1, further comprising a material layer over said oxide layer.

17. The pixel cell of claim 16, wherein said material layer and said oxide layer define a second grated interface.

18. The pixel cell of claim 16, wherein said material layer is a tetraethyl orthosilicate (TEOS) layer.

19. The pixel cell of claim 18, further comprising a boro-phospho-silicate glass (BPSG) layer over said TEOS layer.

20. An integrated circuit comprising:

an array of pixel cells, at least one pixel cell of said array comprising:

a silicon substrate having a photosensor formed therein, and a plurality of trenches located over said photosensor in said silicon substrate; and

an oxide layer comprising a plurality of trenches provided within and over said silicon substrate plurality of trenches to form a grated interface between said oxide layer trenches and said silicon substrate trenches to reduce the reflection of incident light.

21. The integrated circuit of claim 20, wherein said silicon substrate plurality of trenches and said oxide layer plurality of trenches have a substantially semi-rectangular shape.

22. The integrated circuit of claim 21, wherein said semi-rectangular grating has a period within a range from about 100 nm to about 1000 nm.

23. The integrated circuit of claim 22, wherein said semi-rectangular grating has a period of 340 nm.

24. The integrated circuit of claim 21, wherein at least one of said silicon substrate plurality of trenches and said oxide layer plurality of trenches have a predetermined depth within a range of about 10 nm to about 250 nm.

25. The integrated circuit of claim 24, wherein said trench has a depth of 100 nm.

26. The integrated circuit of claim 20, wherein said grated interface is a blazed grating.

27. The integrated circuit of claim 26, wherein a first sidewall region has a first depth, a second sidewall region has a second depth, and a third sidewall region has a third depth.

28. The integrated circuit of claim 27, wherein said first, second, and third depths are within a range from about 10 nm to about 250 nm.

29. The integrated circuit of claim 20, wherein said photosensor is a photodiode.

30. The integrated circuit of claim 29, wherein said photodiode is a pinned photodiode.

31. An image processing system comprising:

a processor;

an imaging device coupled to said processor, said imaging device comprising an imaging array containing a plurality of pixel cells, at least one pixel cell comprising:

a photosensor within a silicon substrate comprising at least two trenches, and

an oxide layer comprising at least two trenches provided over said photosensor, said oxide layer trenches and said substrate trenches defining a grated interface to reduce the reflection of incident light; and

readout circuitry within said semiconductor substrate, said readout circuitry providing signals from said photosensor.

32. The image processing system of claim 31, wherein said grated interface is a semi-rectangular grating.

33. The image processing system of claim 31, wherein said grated interface is a blazed grating.

34. The image processing system of claim 31, wherein said pixel cell further comprises a material layer over said oxide layer.

35. The image processing system of claim 34, wherein said material layer and said oxide layer define a second grated interface.

36. The image processing system of claim 31, wherein said photosensor is a photodiode.

37. The image processing system of claim 31, wherein said photosensor is a pinned photodiode.

38. A method of forming a pixel cell, said method comprising the acts of:

forming a plurality of trenches within a silicon substrate over an area dedicated for a photosensor; and

providing an oxide layer comprising a plurality of trenches within and over said silicon substrate plurality of trenches to form a grated interface between said oxide layer plurality of trenches and said silicon substrate plurality of trenches to reduce the reflection of incident light.

39. The method of claim 38, further comprising the act of forming a photosensor within said silicon substrate within said dedicated area.

40. The method of claim 39, wherein said act of forming a photosensor comprises the act of doping said silicon substrate with p-type and n-type dopants.

41. The method of claim 40, wherein said act of doping results in a pinned photodiode.

42. The method of claim 38, wherein said silicon substrate plurality of trenches is formed by etching said silicon substrate.

43. The method of claim 42, wherein said etching of said silicon substrate is performed by reactive ion etching.

44. The method of claim 42, wherein said etching of said silicon substrate is performed by chemical etching.

45. The method of claim 38, wherein said silicon substrate plurality of trenches is formed by providing a photoresist pattern over said silicon substrate, and forming a plurality of silicon columns.

46. The method of claim 45, wherein said plurality of silicon columns are formed by epitaxial growth.

47. The method of claim 38, wherein said plurality of silicon substrate trenches and said plurality of oxide layer trenches are formed having a substantially semi-rectangular shape.

48. The method of claim 38, wherein at least one of said plurality of silicon substrate trenches and said plurality of oxide layer trenches is formed to have a predetermined depth within a range from about 10 nm to about 250 nm.

49. The method of claim 38, wherein said grated interface has a predetermined period within a range from about 100 nm to about 1000 nm.

50. The method of claim 38, wherein at least one of said plurality of silicon substrate trenches and said plurality of oxide layer trenches is formed to have at least three sidewall regions to define a blazed grated interface between said oxide layer and said substrate.