## DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

Embodiments of the invention encompass methods of forming through substrate interconnects, sometimes referred to in the existing art as through wafer interconnects. In the context of this document, a "through substrate interconnect" is a conductive interconnect extending from a back-side of a semiconductor substrate to integrated circuitry formed on or proximate a front-side of the substrate. Further in the context of this document, the "front-side" of a semiconductor substrate is that one of the two major opposing sides of the substrate (the other being the "back-side") from which the circuit components of the integrated circuitry are primarily fabricated. Further in the context of this document, the term "semiconductor substrate" or "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

Example methods of forming through substrate interconnects are initially described with reference to Figs. 1-5. Referring to Fig. 1, a semiconductor substrate is indicated generally with reference 10, and comprises a first major side 12 and a second major side 14. By way of example only, a thickness range for substrate 10 is from about 700 microns to about 800 microns. Side 12 may comprise a back-side of the semiconductor substrate and side 14 may comprises a front-side of the semiconductor substrate. Yet alternately, side 12 may comprises the front-side of the semiconductor substrate and side 14 may comprise the back-side of the semiconductor substrate. Regardless, semiconductor substrate 10 is depicted as comprising some region 16 and a passivation dielectric layer 18 has been formed thereover. In the context of this document, a "passivation dielectric" is any dielectric material formed over an outer surface of a substrate after completion of most all of the integrated circuit components. Redistribution layers and/or other conductive lines might be formed over passivation dielectric 18, and other insulating and/or passivating layers might be provided thereover as well, but regardless the vast majority of

**CLAIMS**

1. A method of forming a through substrate interconnect sequentially comprising:

forming a via into a semiconductor substrate, the via extending into semiconductive material of the substrate;

applying a liquid dielectric to line at least an elevationally outermost portion of sidewalls of the via relative a side of the substrate from which the via was initially formed;

solidifying the liquid dielectric within the via;

depositing a passivation dielectric over the side of the substrate after forming the via, to within the via, and to bridge over the via to leave a void space within the via inward of the bridging passivation dielectric;

removing all of the passivation dielectric from within the via; and

forming conductive material within the via over the solidified dielectric and forming a through substrate interconnect with the conductive material.

2. The method of claim 1 wherein the applying is of spin-on liquid dielectric in a spin-on manner

3. The method of claim 1 wherein the applying lines all sidewalls of the via with liquid dielectric.

4. The method of claim 1 wherein the applying completely covers a base of the via with liquid dielectric.

5. The method of claim 1 wherein the applying lines all sidewalls of the via with liquid dielectric, and completely covers a base of the via with liquid dielectric.

6. A method of forming a through substrate interconnect, comprising:

forming a via into semiconductive material of a semiconductor substrate from a side of the substrate;

applying a liquid dielectric to line at least an elevationally outermost portion of sidewalls of the via;

solidifying the liquid dielectric within the via;

after solidifying the liquid dielectric, forming a passivation dielectric over the substrate side from which the via was formed and to bridge over the via to leave a void space within the via inward of the bridging passivation dielectric;

removing the passivation dielectric from over the via; and

forming conductive material within the via over the solidified dielectric and forming a through substrate interconnect with the conductive material.

7. The method of claim 6 wherein the removing comprises forming a mask over the passivation dielectric that comprises an opening therethrough to the via and through which the passivation dielectric is removed from over the via by etching.

8. A method of forming a through substrate interconnect, comprising:

forming a via into semiconductive material of a semiconductor substrate from a side of the substrate;

applying a liquid dielectric to line at least an elevationally outermost portion of sidewalls of the via;

solidifying the liquid dielectric within the via;

after solidifying the liquid dielectric, forming a photosensitive passivation dielectric over the substrate side from which the via was formed and at least partially over the via;

removing the photosensitive passivation dielectric from over the via, the removing comprising forming a mask over the photosensitive passivation dielectric that comprises an opening therethrough to the via and through which the photosensitive passivation dielectric is removed from over the via by etching, the mask comprising a photosensitive material of the same composition as that of the photosensitive passivation dielectric; and

forming conductive material within the via over the solidified dielectric and forming a through substrate interconnect with the conductive material.

9. The method of claim 7 wherein the mask comprises a material of different composition as that of the passivation dielectric.

10. The method of claim 6 wherein the forming of the passivation dielectric is not within the via.

11. The method of claim 6 wherein the applying lines all sidewalls of the via with liquid dielectric.

12. The method of claim 6 wherein the applying completely covers a base of the via with liquid dielectric.

13. The method of claim 1 wherein the liquid dielectric is solidified to have a coefficient of thermal expansion which is different from that of the passivation dielectric.

14. The method of claim 8 wherein the composition comprises polyimide.

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The invention claimed is:

1. A method of forming a through substrate interconnect, comprising:

forming a passivation dielectric over a back-side of a semiconductor substrate;

after forming the passivation dielectric, etching through the passivation dielectric and then into semiconductive material of the substrate from the substrate back-side to form a via;

applying a liquid dielectric over the passivation dielectric and into the via to line only an elevationally outermost portion of sidewalls of the via;

solidifying the liquid dielectric within the via;

vapor depositing a dielectric material to within the via to line over the solidified dielectric within the via and to line over sidewall portions of the via received elevationally inward of the solidified dielectric within the via; and

forming conductive material within the via over the vapor deposited dielectric material and forming a through substrate interconnect with the conductive material.

2. The method of claim 1 wherein the liquid and solidified dielectric within the via lines no more than 50% of a combined elevational thickness of the passivation dielectric and the semiconductive material that forms the via.

3. The method of claim 1 wherein the solidified dielectric is thicker than the vapor deposited dielectric material.

4. The method of claim 1 wherein the liquid dielectric has a solidified coefficient of thermal expansion which is between that of the passivation dielectric and the vapor deposited dielectric.

5. The method of claim 1 wherein the vapor deposited dielectric material completely covers all sidewalls of the via elevationally inward of the solidified dielectric that is within the via.

6. The method of claim 5 wherein the via has a base, the vapor deposited dielectric material completely covering all of the via base.

7. The method of claim 6 wherein the liquid dielectric has a solidified coefficient of thermal expansion which is between that of the passivation dielectric and the vapor deposited dielectric.

8. The method of claim 1 wherein the via has a base, the vapor deposited dielectric material not completely covering at least one of a) all sidewall of the via, and b) all of the base.

9. A method of forming a through substrate interconnect, comprising:

forming a passivation dielectric over a front-side of a semiconductor substrate;

after forming the passivation dielectric, etching through the passivation dielectric and then into semiconductive material of the substrate from the substrate front-side to form a via;

applying a liquid dielectric over the passivation dielectric and into the via to line only an elevationally outermost portion of sidewalls of the via;

solidifying the liquid dielectric within the via;

vapor depositing a dielectric material to within the via to line over the solidified dielectric within the via and to line over sidewall portions of the via received elevationally inward of the solidified dielectric within the via; and

forming conductive material within the via over the vapor deposited dielectric material and forming a through substrate interconnect with the conductive material.

10. The method of claim 9 wherein the liquid and solidified dielectric within the via lines no more than 50% of a combined elevational thickness of the passivation dielectric and the semiconductive material that forms the via.

11. The method of claim 9 wherein the solidified dielectric is thicker than the vapor deposited dielectric material.

12. The method of claim 9 wherein the liquid dielectric has a solidified coefficient of thermal expansion which is between that of the passivation dielectric and the vapor deposited dielectric.

13. The method of claim 9 wherein the vapor deposited dielectric material completely covers all sidewalls of the via elevationally inward of the solidified dielectric that is within the via.

14. The method of claim 13 wherein the via has a base, the vapor deposited dielectric material completely covering all of the via base.

15. The method of claim 14 wherein the liquid dielectric has a solidified coefficient of thermal expansion which is between that of the passivation dielectric and the vapor deposited dielectric.

16. The method of claim 9 wherein the via has a base, the vapor deposited dielectric material not completely covering at least one of a) all sidewall of the via, and b) all of the base.