

SELECTIVE SUBSTRATE PROCESSING BASED ON ELECTRODE REGIONS

INCORPORATION BY REFERENCE

[0000] A PCT Request Form is filed concurrently with this specification as part of the present application. Each application that the present application claims benefit of or priority to as identified in the concurrently filed PCT Request Form is incorporated by reference herein in its entirety and for all purposes.

BACKGROUND

[0001] In semiconductor processing, it may be desired that a wafer remains substantially flat. However, during normal operations, a wafer may experience wafer bow. The wafer bow may cause issues such as improper clamping by an electrostatic chuck, inability to be held by a wafer handler, pattern transfer issues during photolithography issues, and others. Processes have been developed to manage wafer bow by keeping the wafer flat within process tolerances. One process includes depositing a film on the backside of the wafer to counteract any stress that may be causing the wafer to bow.

[0002] The background description provided herein is for the purposes of generally presenting the context of the disclosure. Work of the presently named inventors, to the extent it is described in this background section, as well as aspects of the description that may not otherwise qualify as prior art at the time of filing, are neither expressly nor implicitly admitted as prior art against the present disclosure.

SUMMARY

[0003] In one aspect of the present disclosure, an apparatus is disclosed. In some embodiments, the apparatus may be configured to selectively process a semiconductor substrate, and include: a showerhead configured to deliver at least one process gas to a backside of the semiconductor substrate; an electrode having at least a first region and a second region associated therewith; a support structure configured to receive the semiconductor substrate and disposed between the showerhead and the electrode; and a controller coupled to the showerhead and the electrode, and configured to: apply a first amount of power to at least the first region of the electrode, causing at least the first region of the semiconductor substrate to undergo a first process based on the at least one process gas; and apply a second amount of power different from the first amount of power to

at least a second region of the electrode, causing at least the second region the semiconductor substrate to undergo a second process based on the at least one process gas.

[0004] In some variants thereof, based on the application of the first amount of power to the first region and the second amount of power to the second region, a material on the semiconductor substrate may have a spatially varying property on the backside of the semiconductor substrate.

[0005] In another aspect of the present disclosure, a method of selectively processing a semiconductor substrate is disclosed. In some embodiments, the method may include: applying a first amount of power to at least a first region of an electrode, causing at least a first corresponding region of the semiconductor substrate to undergo a first deposition process based on at least one process gas; and applying a second amount of power different from the first amount of power to at least a second region of the electrode, causing at least a second corresponding region the semiconductor substrate to undergo a second deposition process based on the at least one process gas.

[0006] In some variants thereof, based on the application of the first amount of power to the first region and the second amount of power to the second region, a material on the semiconductor substrate may have a spatially varying property on the backside of the semiconductor substrate.

[0007] In some embodiments, the method may include concurrently applying a first amount of power to at least a first region of an electrode and a second amount of power to at least a second region of the electrode, causing at least a first region of the semiconductor substrate corresponding to the first region of the electrode to undergo a first deposition process based on at least one process gas, and at least a second region of the semiconductor substrate corresponding to the second region of the electrode to undergo a second deposition process based on the at least one process gas.

[0008] In some variants thereof, based on the application of the first amount of power to the first region and the second amount of power to the second region, a material on the semiconductor substrate may have a spatially varying property on the backside of the semiconductor substrate.

[0009] These and other features of the disclosed embodiments will be described in detail below with reference to the associated drawings.

BRIEF DESCRIPTION OF DRAWINGS

[0010] FIGS. 1A and 1B show examples of unbowed and bowed semiconductor wafers on an electrostatic chuck.

[0011] FIG. 2 shows example isometric views of various wafer bow shapes.

[0012] FIG. 3 is an illustration of an example of zones associated with an electrode of a substrate processing system for depositing film on a semiconductor substrate, the zones being suitable for “half pipe” bows, according to some embodiments herein.

[0013] FIG. 4 illustrates zones associated with an electrode of a substrate processing system where power is distributed to zones unequally, suitable for “half pipe” bows, and a cross-sectional view of film deposited on a substrate having a “half pipe” bow, according to some embodiments herein.

[0014] FIG. 5 illustrates zones associated with an electrode of a substrate processing system where power is distributed to different zones at different deposition times, suitable for “half pipe” bows, and a cross-sectional view of film deposited on a substrate having a “half pipe” bow, according to some embodiments herein.

[0015] FIG. 6 is an illustration of an example of zones associated with an electrode of a substrate processing system for depositing film on a semiconductor substrate, the zones being suitable for bowl- or umbrella-shaped bows, according to some embodiments herein.

[0016] FIG. 7 illustrates zones associated with an electrode of a substrate processing system where power is distributed to zones unequally, suitable for bowl or umbrella bows, and a cross-sectional view of film deposited on a substrate having a bowl or umbrella bow, according to some embodiments herein.

[0017] FIG. 8 illustrates zones associated with an electrode of a substrate processing system where power is distributed to different zones at different deposition times, suitable for bowl or umbrella bows, and a cross-sectional view of film deposited on a substrate having a bowl or umbrella bow, according to some embodiments herein.

[0018] FIG. 9 illustrates an example configuration of zones associated with an electrode of a substrate processing system, according to some embodiments herein.

[0019] FIGS. 10A and 10B each illustrates a further example configuration of zones associated with an electrode of a substrate processing system, according to some embodiments herein.

[0020] FIG. 11 is a flow diagram of an example method of selectively processing a semiconductor substrate, according to some embodiments.

[0021] FIG. 12 is a flow diagram of another example method of selectively processing a semiconductor substrate, according to some embodiments.

[0022] FIGS. 13 and 14 show block diagrams of example substrate processing systems, according to some embodiments herein.

[0023] FIG. 15A shows an example cross section of an edge of a shower-pedestal.

[0024] FIG. 15B shows a top view of an example carrier ring.

[0025] FIG. 16 is a diagram of a cross-sectional view of a processing system for depositing film on a semiconductor substrate, according to some embodiments herein.

[0026] FIG. 17 shows a schematic of an example process system that may be used to perform the methods described herein.

[0027] FIG. 18A illustrates zones for depositing films having a curved bar profile and a curved channel profile according to various embodiments herein.

[0028] FIGS. 18B and 18C illustrate a side view and exploded side view of a wafer having backside layers having a curved bar profile and a curved channel profile according to various embodiments herein.

DETAILED DESCRIPTION

Terminology

[0029] The following terms are used throughout the instant specification:

[0030] The terms “semiconductor wafer,” “wafer,” “substrate,” “wafer substrate” and “partially fabricated integrated circuit” may be used interchangeably. Those of ordinary skill in the art understand that the term “partially fabricated integrated circuit” can refer to a semiconductor wafer during any of many stages of integrated circuit fabrication thereon. A wafer or substrate used in the semiconductor device industry typically has a diameter of 200 mm, 300 mm, or 450 mm. Examples of wafer materials include silicon (Si), gallium arsenide (GaAs), and silicon germanium (SiGe). Besides semiconductor wafers, other workpieces that may take advantage of the disclosed embodiments include various articles such as printed circuit boards, magnetic recording media, magnetic recording sensors, mirrors, optical elements, display devices or components such as backplanes for pixelated display devices, flat panel displays, micro-mechanical devices and the like. The workpiece may be of various shapes, sizes, and materials.

[0031] A “semiconductor device fabrication operation” as used herein is an operation performed during fabrication of semiconductor devices. Typically, the overall fabrication process includes multiple semiconductor device fabrication operations, each performed in its own semiconductor fabrication tool such as a plasma reactor, an electroplating cell, a chemical mechanical planarization tool, a wet etch tool, and the like. Categories of semiconductor device fabrication operations include subtractive processes, such as etch processes and planarization processes, and

material additive processes, such as deposition processes (e.g., physical vapor deposition, chemical vapor deposition, atomic layer deposition, electrochemical deposition, electroless deposition). In the context of etch processes, a substrate etch process includes processes that etch a mask layer or, more generally, processes that etch any layer of material previously deposited on and/or otherwise residing on a substrate surface. Such an etch process may etch a stack of layers in the substrate.

[0032] “Manufacturing equipment” refers to equipment in which a manufacturing process takes place. Manufacturing equipment often has a process chamber in which the workpiece resides during processing. Typically, when in use, manufacturing equipment performs one or more semiconductor device fabrication operations. Examples of manufacturing equipment for semiconductor device fabrication include deposition reactors such as electroplating cells, physical vapor deposition reactors, chemical vapor deposition reactors, and atomic layer deposition reactors, and subtractive process reactors such as dry etch reactors (e.g., chemical and/or physical etch reactors), wet etch reactors, and ashers.

[0033] “Wafer bow” as used herein may refer to a deformation of a wafer. The deformation may have radial and/or azimuthal components. Examples of types of wafer bow include dome shapes, bowl shapes, dish shapes, potato chip shapes, and saddle shapes. Wafer bow may occur during fabrication, for example, as a result of stress to the wafer during deposition of materials on an active surface of a wafer substrate. Wafer bow may occur during various types of fabrication, such as when large stacks of materials are deposited. Wafer bow may cause complications in subsequent processing steps. For example, the wafer may fail to chuck correctly if an amount of bowing is too large. Moreover, some processing steps (e.g., photolithography) may produce poor results if performed on a wafer that is excessively bowed.

[0034] Wafer bow may be measured as a deviation of the mean or median distance of the surface of the wafer to a reference plane. In some approaches, the point of the median surface of the wafer may be the center point (e.g., in the case of concave or domed bowing), or an edge point of the wafer and/or an average edge point of the wafer (e.g., in the case of warping or convex bowing). In some embodiments, wafer bow may be measured from a reference plane such that when an edge point of the wafer is below the reference plane the edge point is considered to have a negative bow, and when the edge point of the wafer is above the reference plane the edge point is considered to have a positive bow. In some embodiments, positive or negative bow may be measured along a z axis perpendicular to the reference plane.

[0035] In some embodiments, wafer bow may vary between the two principal planar dimensions of a substrate, which are referred to as the x and y directions. For example, wafer bow along the x dimension may be in a positive z direction while wafer bow along the y dimension may be in a

negative z direction. (the z axis being perpendicular to a plane formed by the planar x and y dimensions). FIG. 2 illustrates eight shapes that may be formed based on bowing in x and y dimensions. For example, when bowing is positive along the x and y dimensions, a bowl shape 202 is formed, while when bowing is negative in the x and y dimensions, a dome or umbrella shape 207 is formed. Other shapes include a “half pipe” such as a “taco” shape 203, 205 or a “cannoli” shape 204, 206 when there is substantially no wafer bow in a first dimension while having a positive or negative bow in the planar perpendicular dimension to the first dimension. When wafer bow is positive in one dimension and negative in another dimension, a “saddle” or “potato chip” shape 201, 208 can be formed. These shapes will be referenced and discussed below.

Bowed Wafers

[0036] Semiconductor device fabrication often involves deposition of a stack of layers on a wafer substrate. Typically, most deposition and other processing to form the devices occurs on one side of the substrate, often referred to as the front face or frontside of a wafer. As the deposited layers build up, they can introduce stress in the wafer. A large net tensile or compressive stress can cause the wafer to bow, which is undesirable.

[0037] Bowing is especially likely to occur where large stacks of materials are deposited, for example, in the context of 3D-NAND devices, or where a thick front side layer is deposited. Where bowing is significant, it can deleteriously affect subsequent processing steps. For instance, the wafer may fail to chuck correctly if the bowing is too great. FIGS. 1A and 1B show a wafer on an electrostatic chuck. FIG. 1A shows a wafer 102 on an electrostatic chuck 104. When the wafer 102 is substantially flat for purposes of a particular process operation, e.g., having a bow of about 100 μm (microns) or less, the wafer may be properly clamped, securing the wafer for subsequent processing steps. FIG. 1B shows a bowed wafer 102' on the electrostatic chuck 104. When the bow is significant, the wafer may fail to secure properly on the electrostatic chuck. Wafer bow may cause other problems. For example, certain processing steps (e.g., photolithography) are very precise and produce poor results if the wafer is not substantially flat. The problem may be manifest as lithography defocus.

[0038] One example stack that may cause these problems is a stack having alternating layers of oxide and nitride (e.g., silicon oxide/silicon nitride/silicon oxide/silicon nitride, etc.). Another example of a type of stack likely to cause bowing includes alternating layers of oxide and polysilicon (e.g., silicon oxide/polysilicon/silicon oxide/polysilicon, etc.). Other examples of stack materials that may be problematic include, but are not limited to, tungsten and titanium nitride.

[0039] The materials in the stacks may be deposited through chemical vapor deposition (CVD) techniques such as plasma enhanced chemical vapor deposition (PECVD), low pressure chemical vapor deposition (LPCVD), metal organic chemical vapor deposition (MOCVD), atomic layer deposition (ALD), plasma enhanced atomic layer deposition (PEALD), or through direct metal deposition (DMD), etc. These examples are not intended to be limiting. Certain disclosed embodiments may be useful whenever wafer stress and/or bowing are induced due to material present on the frontside of the wafer.

[0040] The frontside stacks may be deposited to any number of layers and thicknesses. In an example, the stack includes about 20 or more layers, and has a total thickness of about 2 μm to about 4 μm . However, in some cases, multiple-layer stacks have about one hundred or more layers. In some embodiments, multiple-layer stacks may have about five hundred or more layers. In some embodiments, the multiple-layer stacks may have about one thousand or more layers. Such stacks may have a thickness of about 4 μm to 12 μm , for example.

[0041] The stress induced in the wafer by the stack or other frontside deposition may be about -500 MPa to about $+500\text{ MPa}$. In some embodiments, the resulting in a bow is about 150 μm or greater, e.g., about 300 μm and above, about 400 μm and above, or about 200 μm to about 400 μm (for a 300 mm wafer).

[0042] Another cause of wafer bow may be frontside processing which uses thick hardmasks with limited etch selectivity. In these embodiments, at least one of the one or more frontside layers is a hardmask. The thick hardmasks may have an internal stress similar to those described above, e.g., have a magnitude of 0 MPa to about 500 MPa. The stress caused by the hardmask may be tensile stress or compressive. The thick hardmasks may cause wafers to have a significant wafer bow, e.g., about 150 μm or more.

[0043] Various techniques have been devised for combatting bowing. When bowing is more severe, deposition processes may be tuned to reduce or counteract internal stresses in deposited layers. However, any such tuning should not interfere with process requirements for fabricating devices. One commonly used technique to counteract bowing deposits a film on the back side of the wafer.

[0044] Backside deposition may form a high-stress film. If the backside layer has the same type of internal stress (tensile or compressive) and of comparable magnitude to the internal stress created on the frontside, the backside film effectively counteracts and reduces the bow.

[0045] Examples of backside films used to counteract bow include the following: amorphous silicon, silicon oxide, silicon nitride, and silicon oxynitride. Current backside films have high

internal stress and can mitigate the stresses imparted on the wafer from the frontside layers to reduce or eliminate the wafer bow. Generally, backside layers are made of films with high stress.

[0046] Until relatively recently, the backside film thickness remained relatively thin (e.g., under 2 μm) because the bow caused by depositing material on the frontside was relatively modest. Thus, downstream processes at previous technology nodes did not normally experience issues addressed by embodiments herein. However, modern integrated circuit (IC) fabrication techniques may produce substrates having frontside layers that produce much more severe wafer bow compared to previous nodes. For example, some modern processes use thick hardmask layers in operations where the etch selectivity between the hardmask and etched material is limited, yet deep trenches or vias are etched. In another example, frontside stacks have increased the number of layers. For example, in previous nodes stacks may have been about 32 to about 72 layers. Now, stacks may have hundreds or even thousands of layers, increasing the thickness of the frontside layer and the internal stress. Typically wafer bow compensation is achieved by depositing a single backside layer. Due to the increasing magnitude of wafer bow, thicker backside films must be deposited to compensate for wafer bow. This has caused certain issues. Due to large internal forces occurring within thick backside layers, the layers may spontaneously form film cracks. For many film materials (e.g., tensile silicon nitride films), cracks are observed in films of thicknesses necessary to compensate for bow values above a critical bow limit. These bow limits are commonly known as the “bow cracking limit” or “cracking margin.”

[0047] If a crack does form, it may create separations large enough to provide a pathway for contaminants to directly contact the backside of the wafer, potentially damaging it. For example, chemical wet etchants, which are often used to remove backside films, may penetrate through a film crack in a backside film leading to a non-uniform etch or wafer etching, which can cause particles issues such as film flaking. Furthermore, these film cracks may be so severe that they cause the wafer itself to crack, in some cases to a depth twice as great as the film thickness.

[0048] To avoid backside film cracking, wafer bowing may be limited to an amount well below the bow cracking limit of the film. This means that some wafer integration procedures are conducted in stages, with an operation that would normally be conducted in a single step being divided into a series of steps, each introducing a relatively small bow that is compensated by a commensurately thin backside layer. This adds complexity to device manufacturing and decreases overall throughput.

[0049] In some cases, backside film thickness may be relatively uniform because the bow caused by depositing material on the frontside is relatively uniform, forming a bowl or dome shape based on an isotropic internal stress. Thus, depositing a uniform profile film, either with tensile or

compressive internal stress, could mitigate the stressed imparted on a wafer from the frontside layers. However, certain frontside deposition techniques may cause anisotropic stress, such that the internal stress on the front side of the wafer, and hence the resultant bowing, varies in one principal planar dimension compared to another principal planar dimension, e.g., x and y dimensions. In such embodiments, a wafer may have x-bow and y-bow that are different in magnitude as well as direction. A uniform backside layer may insufficiently address such wafer bow.

[0050] Referring again to FIG. 2, eight example shapes that may form based on different combinations of positive or negative bowing along x and y dimensions are illustrated. A bowl 202, umbrella 207, half pipe (such as a taco 203, 205 or a cannoli 204, 206), or saddle shape 201, 208 may be formed depending on whether wafer bow along the x and y dimensions is positive, negative, or substantially non-existent. When a wafer bow shape is a bowl 202 or umbrella 207, a uniform profile film having an isotropic tensile or compressive internal stress may properly mitigate the stress imparted on the wafer from frontside layers. However, when the wafer bow shape is a different shape, an isotropic internal stress would either over or under compensate wafer bow along the x or y direction, or potentially exaggerate wafer bow. For example, an isotropic tensile backside film deposited on a wafer having a negative x-bow and positive y-bow (i.e., saddle shape 201, 208) would mitigate wafer bow along the y dimension, but would increase wafer bow along the x dimension.

[0051] Thus far herein, it has been established and shown that semiconductor substrates such as wafers can have varied bow symmetry along x and/or y directions, where the bowing is induced as a result of, e.g., stress to the wafer during fabrication processes such as deposition of materials. In addition, it has been established that bowing can be counteracted via deposition of film on the substrate, such as on the opposite side (e.g., backside) of the side where stress was created (e.g., frontside). It would be desirable to induce opposing stresses that are customized and targeted according to the stresses present on the other side of the substrate. However, showerheads of substrate processing systems typically do not have the ability to customize film stress in specific areas of the wafer.

[0052] To these ends, disclosed herein are techniques for depositing films selectively in regions or zones of a semiconductor substrate. As an illustrative example, a film (or portion of film) deposited on a portion of the backside of a substrate may have an internal stress and/or a thickness that is different from a film deposited on another portion the backside. That is, some parameters or properties of the backside film that can be customized may include an internal stress and/or a thickness of the film. Different amounts or types of film material may be deposited to tune these

properties. By customizing the internal stress and/or thickness of film as a function of location of the backside of the substrate, the amount of internal stress in different regions of the substrate can spatially vary. In some embodiments, the thickness of film (or other film properties) may be tuned selectively and spatially across the substrate by varying power to specific zones. This approach can be extended to myriad patterns and shapes of zones, as will be described herein. Advantageously, this approach can compensate for various types of bow that may be present in the substrate.

Zones for Selective Deposition

[0053] FIG. 3 is an illustration of an example of zones 312, 314, 316 associated with an electrode 310 of a substrate processing system for depositing film on a semiconductor substrate, according to some embodiments herein. In this example, the zones 312, 314, 316 associated with the electrode 310 may be substantially longer along one axis (e.g., y-axis) and parallel to one another. Hence, each zone may have its own shape and may be positioned relative to other zones, as shown. Such relative positions may be referred to herein as a “pattern.” In some embodiments, the pattern of zones 312, 314, 316 may be suitable for a substrate having “half pipe” bow shape such as a taco shape 302, 306 or a cannoli shape 304. In other words, the bow to be compensated via film deposition has a positive or negative bow along one dimension or axis 308x and substantially no bow along the other, perpendicular dimension or axis. Referring to the taco shape 302 as an illustrative example, there is a bow along axis 308x but not axis 308y.

[0054] FIG. 4 illustrates zones 412, 414, 416 associated with a bottom side of an electrode 410 of a substrate processing system where power is distributed to zones unequally, suitable for “half pipe” bows, and a cross-sectional view of film 430 deposited on a substrate 420 having a “half pipe” bow, according to some embodiments herein. The taco 302, 306 and cannoli 304 as shown in FIG. 3 may be examples of the “half pipe” bows. Zones 412, 414, 416 may be examples of zones 312, 314, 316, respectively, of FIG. 3.

[0055] In some embodiments, the zones 412, 414, 416 associated with the electrode 410 may each receive a corresponding amount of radio frequency (RF) power. That is, RF power may be separately controlled to distinct positions on electrode 410. For example, zones 412 and 416 (labeled “1” and “3”) on the sides of the electrode 410 may receive a first amount of RF power, and middle zone 414 (labeled “2”) in the middle of the electrode 410 may receive a second amount of RF power different from the first amount of RF power. The first and second amounts of power may cause different amounts of plasma to be formed and corresponding amounts of film material 430 to be deposited on the substrate 420, e.g., via a deposition process such as those mentioned above (PECVD, ALD, PEALD, etc.). In this example, the zones 412 and 416 on the sides of the

electrode 410 may receive a substantially similar amount of RF power (the first amount of RF power) because the bow is symmetrical with respect to one axis. As described with respect to the example of the taco shape 302 shown in FIG. 3, a taco or cannoli shape has a bow along one dimension or axis but no bow along the other perpendicular dimension or axis.

[0056] Hence, by distributing power unequally to different zones (e.g., more to the middle zone 414 of electrode 410), an appropriate additional amount of film material 430 can be deposited on corresponding regions of the substrate 420. For example, a strip in the middle region 424 of the substrate 420 may correspond to the middle zone 414 of the electrode 410. The middle zone 414 of the electrode 410 may receive more RF power relative to the other zones 412, 416, and the middle region 424 of the substrate 420 may have more material deposited relative to other, side regions 422, 426 of the substrate 420. A corresponding amount of additional stress can be introduced to the middle region 424 of the substrate 420. More specifically, by depositing an additional amount of material 430 onto middle region 424 of the substrate 420 compared to regions 422, 426 of the substrate 420, the resulting substrate 420 may have a thicker portion 434 of the film material 430 formed in the middle. A thickness difference 438 may exist between the thicker portion 434 (corresponding to the middle region 424) and one or more other portions 432a and/or 432b (corresponding to the regions 422 and/or 426). In some cases, transition portions 436a, 436b may result between the thicker portion 434 and other portions 432a, 432b, where the thickness may taper and change gradually rather than creating a sharp bevel. According to different implementations, the stress may be tensile or compressive, depending on film material. One example of a tensile film material may include high-tensile silicon nitride (SiN). One example of a compressive film material may include high-compression SiN or undoped silicate glass (SiO₂).

[0057] In some embodiments, the thickness difference 438 that results from the uneven application of RF power to the electrode 410 may be up to a specified amount of difference. For example, the thickness difference 438 may be limited to a certain amount relative to the film thickness at the shallower portions (e.g., portions 432a, 432b). In certain example embodiments, the thickness difference 438 may not exceed 6%. That is, in such embodiments, the thickness of portion 434 may only be up to 106% of the thickness of portions 432a, 432b. This thickness difference 438 may arise from a difference in deposition rate between a region with higher RF power and a region with lower RF power; e.g., higher RF power may be applied to middle zone 414 to form thicker film material 430 in the middle region 424, and lower RF power may be applied to region 422 or 426 to form thinner film material 430 at the other portion 432a or 432b, where the difference in thickness is thickness difference 438. However, in other embodiments, other magnitudes or measurements of the limitation may be placed (e.g., lower or higher RF power

differences and thickness difference 438 resulting in a film that is some percent or amount thicker than the shallowest region or than the average layer thickness). This limitation on the thickness difference 438 may be useful to, e.g., meet specifications or requirements (e.g., user needs); conform to requirements of the technology, the tool being used, or downstream applications (e.g., lithography, etching, additional deposition); ensure proper correction of the wafer bow; or have uniformity.

[0058] It will be appreciated that the reverse can be performed where, e.g., the middle region 424 may be shallower than the side regions 422, 426 of the substrate 420. The same principles discussed above may then apply. For example, the thickness of portions 432a, 432b may be up to 106% of the thickness of portion 434.

[0059] Limiting the difference in thickness can be particularly important for subsequent, downstream processing. Downstream processing may involve attaching the substrate to a chuck (e.g., vacuum or electrostatic) that directly contacts the backside surface of the substrate. The substrate must present a very flat front face in these downstream processing operations (e.g., for lithography). While the techniques in the present disclosure can tailor the profile of the material being deposited to the backside layer to compensate for the bow of incoming substrates (making them overall flatter) to address the downstream processing challenge, this overall flatness of the substrate is conducive to proper processing to the extent the backside layer itself (e.g., 430 is uniform. This is because when the substrate attaches to the chuck, a bumpy or non-uniformly thick backside layer could cause the front side of the wafer to be similarly non-uniform.

[0060] FIG. 5 illustrates zones 512, 514, 516 associated with a bottom side of an electrode 510 of a substrate processing system where power is distributed to different zones at different deposition times, suitable for “half pipe” bows, and a cross-sectional view of film 530 deposited on a substrate 520 having a “half pipe” bow, according to some embodiments herein. In some embodiments, the deposition may be a two-step process having a first deposition and a second deposition.

[0061] During a first deposition, a first set of the zones 512, 514, 516 of the electrode 510 may receive RF power. For example, zone 514 of electrode 510 (labeled “2”) may receive RF power during the first deposition of film material on the substrate 520 (e.g., using any of the deposition techniques discussed herein), resulting in a deposition of a portion 532 of film material on or substantially on the corresponding middle region 524 of the substrate 520. No (or low) power may be delivered to the other zones 512, 516 of the electrode 510. Thus, no (or less) film may be deposited on adjacent regions 522, 526 of the substrate 520. In some scenarios, however, there may be at least one tapered portion 533 at edges of the portion 532 of the film material, at

boundaries 523 between the middle region 524 and the adjacent regions 522, 526 of the substrate 520. Plasma or reaction with plasma may not be confined exactly to a specific region or space, resulting in such a tapered portion 533. In some cases, the at least one tapered portion 533 may extend to regions 522, 526, or may have less of film portion 532 material near the boundaries 523. The film portion 532 being “substantially on” the middle region 524 of the substrate 520 may refer to either instance, where there is slightly more or less material than if a vertical edge that could be formed where the boundaries 523 are.

[0062] During a subsequent, second deposition, a second set of the zones 512, 514, 516 of the electrode 510 may receive RF power. In some embodiments, the second set may be different from the first set of the zones 512, 514, 516. For example, zones 512 and 516 of electrode 510 (labeled “1” and “3”) may receive RF power during the second deposition, while zone 514 receives no (or less) RF power. This may result in a deposition of portions 534a and 534b of film material on or substantially on the corresponding side regions 522, 526 of the substrate 520. In some approaches, the thickness of portions 532, 534a and 534b may be substantially the same so as to have a substantially flat film 530 deposited on the substrate 520 after the second deposition.

[0063] In some embodiments, the two-step process may be used to deposit different film material onto different regions. For example, middle region 524 of the substrate 520 may have one type of film deposited, while the side regions 522, 526 may have another type of film deposited. Different types of films may have different mechanical properties, e.g., internal stress (compressive or tensile). Advantageously, depositing film materials having different stress properties may allow correction of the “half pipe” bow on the substrate 520 while keeping the film substantially flat. Further, the rate or total amount of RF power delivered to zone 514 and the rate or total amounts of RF power delivered to respective zones 512 and 516 may be the same or different.

[0064] In some implementations, the second set of the zones 512, 514, 516 receiving RF power may overlap with the first set of the zones 512, 514, 516 receiving RF power. That is, the film deposition that occurs during the second deposition may overlap with the film deposition that occurs during the first deposition. For example, during the second deposition, RF power may be delivered to zone 514 again, along with another zone, such as zone 512 or zone 516. This RF power may be different for each zone so as to tune the thickness of the film deposited in the corresponding regions of the substrate 520. This can allow the profile of the film to be customized further according to the desired film thickness profile or shape to counteract the wafer bow of the substrate 520. In certain cases, the second set may be the same as the first set of the zones 512, 514, 516. That is, the previous deposition may be repeated, which may be useful where, e.g., multiple layers need to be deposited or a certain thickness of film material is desired.

[0065] In some implementations, the two-step process may be used to deposit the same film material onto the different regions at different times. However, the amount of film or deposited or the internal stresses of the deposited materials may be different (e.g., based on different amounts of power applied to the electrode 510 or different deposition conditions). In some cases, this may result in a film thickness profile that appears similar to that shown in FIG. 4, where the thickness (and/or other properties such as internal stress) varies spatially across the substrate. This approach may allow increased adjustability in the thickness on the different regions and/or allow customization subsequent to and based on the result of the first deposition. For instance, the resulting wafer bow correction after the first deposition could be evaluated to determine the thickness or internal stress of the film material that should be deposited next on the substrate 520.

[0066] In some implementations, not all regions of the substrate 520 may have film material on them after the depositions are completed. For example, middle region 524 may have film portion 532, and side region 522 may have film portion 534a. However, side region 526 may not have any film on it, so film portion 534b would be missing or less present (less thick) in this case.

[0067] In some implementations, a one-step process may be used to deposit a film material onto a specific region or regions on the substrate 520. Depending on the configuration of the amount and location of RF power provided to the available zones of electrode 510, this approach may result in a film profile where some regions of the substrate 520 do not have any film material on them, or a film profile similar to that of FIG. 4 where deposited one type of film material covers the entirety of the substrate.

[0068] As can be appreciated, providing different amounts of power to different zones of an electrode of a substrate processing system (as discussed with respect to FIG. 4) and/or providing power to different zones (same or different amounts) at different deposition process steps or at different times (as discussed with respect to FIG. 5) greatly improves the flexibility and customizability of film being deposited on a backside of a substrate, which can advantageously enable compensation of myriad (possibly any) types and shapes of bow.

[0069] It will be further appreciated that the two-step process described above with respect to FIG. 5 is merely illustrative. In various implementations, this approach can be extended to three or more deposition steps using the three regions 522, 524, 526 of the substrate 520, or three or more deposition steps using numerous more regions (e.g., four or more) and myriad patterns of regions, including for different bow shapes, as will be described below.

[0070] FIG. 6 is an illustration of an example of zones 612, 614 associated with an electrode 610 of a substrate processing system for depositing film on a semiconductor substrate, according to some embodiments herein. In this example, the zones 612, 614 associated with the electrode 610

may be arranged as concentric circles or substantially circular shapes. More specifically, zone 612 may be a substantially circular area in the middle of the electrode 610, and zone 614 may be a substantially circular tube or donut shape surrounding the zone 612. In some embodiments, the pattern of zones 612, 614 may be suitable for a substrate having a bowl having a shape of a bowl 602 or an umbrella 604.

[0071] FIG. 7 illustrates zones 712 and 714 associated with a bottom side of an electrode 710 of a substrate processing system where power is distributed to zones unequally, suitable for bowl or umbrella bows, and a cross-sectional view of film 730 deposited on a substrate 720 having a bowl or umbrella bow, according to some embodiments herein. The bowl 602 and umbrella 604 as shown in FIG. 6 may be examples of these bows. Zones 712 and 714 may be examples of zones 612 and 614, respectively, of FIG. 6.

[0072] In some embodiments, the zones 712 and 714 associated with the electrode 710 may each receive a corresponding amount of radio frequency (RF) power. For example, inner zone 712 (labeled “1”) of the electrode 710 may receive a first amount of RF power, and outer zone 714 (labeled “2”) of the electrode 710 surrounding the inner zone 712 may receive a second amount of RF power different from the first amount of RF power. The first and second amounts of power may cause different corresponding amounts of film material 730 to be deposited on the substrate 720, e.g., via a deposition process such as those mentioned above (PECVD, ALD, PEALD, etc.).

[0073] Hence, by distributing power unequally to different zones (e.g., more to the inner zone 712 of electrode 710), an appropriate additional amount of film material 730 can be deposited on corresponding regions of the substrate 720. For example, a circle or substantially circular region in the inner region 722 of the substrate 720 may correspond to the inner zone 712 of the electrode 710. The inner zone 712 of the electrode 710 may receive more RF power relative to the outer zone 714, and the inner region 722 of the substrate 720 may have more material deposited relative to the outer region 724 of the substrate 720. A corresponding amount of additional stress can be introduced to the inner region 722 of the substrate 720. More specifically, by depositing an additional amount of material 730 onto inner region 722 of the substrate 720 compared to outer region 724 of the substrate 720, the resulting substrate 720 may have a thicker portion 734 of the film material 730 formed in its center. A thickness difference 738 may exist between the thicker portion 734 (corresponding to the inner region 722) and surrounding portions 732 (corresponding to the outer region 724). In some cases, transition portions 736 may result between the thicker portion 734 and surrounding portions 732, where the thickness may taper and change gradually rather than creating a sharp bevel. According to different implementations, the stress may be tensile or compressive, depending on film material.

[0074] In some embodiments, the thickness difference 738 that results from the uneven application of RF power to the electrode 710 may be up to a certain amount of difference. For example, the thickness difference 738 may be limited to a certain amount relative to the film thickness at the shallower portions (e.g., surrounding portions 732). In some embodiments, the thickness difference 738 may not exceed 6%. That is, the thickness of portion 734 may only be up to 106% of the thickness of surrounding portions 732. However, other limitations may be placed in other embodiments. This limitation on the thickness difference 738 may be useful to, e.g., meet specifications or requirements; conform to requirements of the technology, the tool, or downstream applications (e.g., lithography, etching, additional deposition); ensure proper correction of the wafer bow; or have uniformity.

[0075] It will be appreciated that the reverse can be performed where, e.g., the inner region 722 may be shallower than the outer region 724 of the substrate 720. The same principles discussed above may then apply. For example, the thickness of portions 732 may be up to 106% of the thickness of portion 734.

[0076] FIG. 8 illustrates zones 812 and 814 associated with a bottom side of an electrode 810 of a substrate processing system where power is distributed to different zones at different deposition times, suitable for bowl or umbrella bows, and a cross-sectional view of film 830 deposited on a substrate 820 having a bowl or umbrella bow, according to some embodiments herein. In some embodiments, the deposition may be a two-step process having a first deposition and a second deposition.

[0077] During a first deposition, a first set of the zones 812 and 814 of the electrode 810 may receive RF power. For example, zone 812 of electrode 810 (labeled "1") may receive RF power during the first deposition of film material on the substrate 820 (e.g., using any of the deposition techniques discussed herein), resulting in a deposition of a portion 832 of film material on or substantially on the corresponding inner region 822 of the substrate 820. No (or low) power may be delivered to the other, outer zone 814 of the electrode 810. Thus, no (or less) film may be deposited on outer region 824 of the substrate 820. In some scenarios, there may be a tapered portion 833 at edges of the portion 832 of the film material, at a boundary 823 along the circumference of the inner region 822 between the inner region 822 and the outer regions 824 of the substrate 820. Plasma or reaction with plasma may not be confined exactly to a specific region or space, resulting in such a tapered portion 833. In some cases, the tapered portion 833 may extend to the outer region 824, or may have less of film portion 832 material near the boundary 823. The film portion 832 being "substantially on" the inner region 824 of the substrate 820 may refer to

either instance, where there is slightly more or less material than if a vertical edge that could be formed where the boundaries 823 are.

[0078] During a subsequent, second deposition, a second set of the zones 812, 814 of the electrode 810 may receive RF power. In some embodiments, the second set may be different from the first set of the zones 812, 814. For example, outer zone 814 of electrode 810 (labeled “2”) may receive RF power during the second deposition, while inner zone 812 receives no (or less) RF power. This may result in a deposition of portion 834 of film material on or substantially on the corresponding outer regions 824 of the substrate 820. In some approaches, the thickness of portions 832 and 834 may be substantially the same so as to have a substantially flat film 830 deposited on the substrate 820 after the second deposition.

[0079] In some embodiments, the two-step process may be used to deposit different film material onto different regions. Depositing film materials having different stress properties may allow correction of the bowl or umbrella bow on the substrate 820 while keeping the film substantially flat. Further, the rate or total amount of RF power delivered to one zone and the rate or total amount of RF power delivered to another zone may be the same or different.

[0080] In some implementations, the second set of the zones 812, 814 receiving RF power may overlap with the first set of the zones 812, 814 receiving RF power. That is, the film deposition that occurs during the second deposition may overlap with the film deposition that occurs during the first deposition. For example, during the second deposition, RF power may be delivered to zone 812 again, along with zone 814. This RF power may be different for each zone so as to tune the thickness of the film deposited in the corresponding regions 822, 824 of the substrate 820. This can allow the profile of the film to be customized further according to the desired film thickness profile or shape to counteract the wafer bow of the substrate 820. In certain cases, the previous deposition may be repeated, which may be useful where, e.g., multiple layers need to be deposited or a certain thickness of film material is desired.

[0081] In some implementations, the two-step process may be used to deposit the same film material onto the different regions at different times. However, the amount of deposition may be different, resulting in a film thickness profile similar to that shown in FIG. 7, where the thickness varies spatially across the substrate.

[0082] In some implementations, not all regions of the substrate 820 may have film material on them after the depositions are completed. For example, inner region 822 may have film portion 832, but outer region 824 may not have any film on it, so film portion 834 would be missing or less present (less thick) in this case.

[0083] In some implementations, a one-step process may be used to deposit a film material onto a specific region or regions on the substrate 820. Depending on the configuration of the amount and location of RF power provided to the available zones of electrode 810, this approach may result in a film profile where some regions of the substrate 820 do not have any film material on them, or a film profile similar to that of FIG. 7 where deposited one type of film material covers the entirety of the substrate.

[0084] It will be appreciated that the two-step process described above with respect to FIG. 8 is merely illustrative. In various implementations, this approach can be extended to three or more deposition steps using the two regions 822, 824 of the substrate 820, or three or more deposition steps using numerous more regions (e.g., three or more regions of substantially concentric circular shape or other shapes) and myriad patterns of regions, including for different bow shapes, as was described above and will be described below.

[0085] FIG. 9 illustrates an example configuration of zones associated with an electrode 910 of a substrate processing system, according to some embodiments herein. A bottom view of the electrode 910 is shown, which may face a substrate and/or components of a substrate processing system (such as a shower-pedestal discussed below). An electrode configured to generate plasma and cause deposition of material may have one or more zones. In examples discussed above, there may be two or more zones for customized control of localized plasma density (and thus control and tune the thickness of deposited film).

[0086] In this example configuration of zones, which is purely for illustrative purposes, there may be numerous zones, 17 in this example. As can be seen, this pattern or “mesh” or zones may include a group of eight (8) sectors or portions of sectors of substantially equal area, each group within respective circular or substantially circular first region 912 and second region 914.

[0087] The 17th zone may be an edge zone having a substantially circular tube shape on the outer edge of the electrode 910. This zone may be defined as a zone between the diameter 916 of the second region 914 and the edge 918 of the electrode 910. The edge zone may be relatively thinner or smaller than the other zones shown. For example, the diameter 916 may be 2 mm smaller than the diameter of the edge 918 of the electrode 910. In other words, there may be a small difference between the diameters of the second region 914 and the edge 918 of the electrode 910, and the corresponding regions of the substrate whose bow is being corrected.

[0088] In some cases, the edge zone may not receive any RF power so that any components of the substrate processing system, such as a tab or other parts of a support structure (e.g., a carrier ring as discussed below), are not affected. There may not be any significant bow at the

corresponding edge region of a bowed substrate either. However, in some cases, power may be applied to the edge zone.

[0089] As yet further examples, FIGS. 10A and 10B each illustrates a further example configuration of zones associated with an electrode of a substrate processing system, according to some embodiments herein.

[0090] FIG. 10A shows an electrode 1010 having two zones 1011 and 1012, similar to electrode 610 shown in FIG. 6, except that the diameter of zone 1011 is closer to the diameter of zone 1012. In fact, electrode 1010 may be an example of electrode 610, and similar approaches may be taken with respect to application of RF power unevenly or at different times or deposition stages.

[0091] FIG. 10B shows an electrode 1020 having four zones 1021 – 1024. Zones 1021 – 1023 are similar to that of electrode 310 shown in FIG. 3, except that there is an edge zone 1024 similar to that of FIG. 9. Similar approaches may be taken with respect to application of RF power to the zones 1021 – 1023 unevenly or at different times or deposition stages. In some cases, as discussed above with respect to FIG. 9, power may or may not be applied to the edge zone 1024.

[0092] As this example configurations of zones shown in FIGS. 9, 10A and 10B are merely illustrative, those having skill in the relevant arts will recognize myriad configurations, shapes, sizes, locations, construction material, applied power, timing of applied power, and other properties of zones of an electrode consistent with this disclosure. There is also no limit to the number of zones. As but examples, it may be possible to configure an electrode to have 36, 360, 720 (or conceivably more) individual sectors or strips or circular areas or other types of zones in total. As shown via above examples of FIGS. 3 – 8, RF power may be applied selectively to different zones, at different times, in different amounts, or a combination thereof. Advantageously, these approaches can allow for highly customized application of material to counteract literally any type of bow, including those having shapes shown in FIG. 2.

Methods

[0093] FIG. 11 is a flow diagram of an example method 1100 of selectively processing a semiconductor substrate, according to some embodiments. One or more of the functions of the method 1100 may be performed by or caused by a computerized apparatus or system. Structure for performing the functionality illustrated in one or more of the blocks shown in FIG. 11 may be performed by hardware and/or software components of such computerized apparatus or system, such as, for example, a controller apparatus, a computerized system, or a computer-readable apparatus including a storage medium storing computer-readable and/or computer-executable instructions that are configured to, when executed by a processor apparatus, cause the at least one

processor apparatus or a computerized apparatus to perform the operations. A controller may be one example of the computerized apparatus or system. A process chamber may be another example of the computerized apparatus or system. Example components of above apparatus are illustrated in FIGS. 13 – 17, and described in more detail elsewhere herein.

[0094] It should also be noted that the operations of FIG. 11 may be performed in any suitable order, not necessarily the order depicted in FIG. 11. Further, the process shown in FIG. 11 may include additional or fewer operations than those depicted in FIG. 11.

[0095] At block 1110, the method 1100 may include applying a first amount of power to at least a first region of an electrode, causing at least a first corresponding region of the semiconductor substrate to undergo a first deposition process based on at least one process gas.

[0096] At block 1120, the method 1100 may include applying a second amount of power different from the first amount of power to at least a second region of the electrode, causing at least a second corresponding region the semiconductor substrate to undergo a second deposition process based on the at least one process gas.

[0097] In some embodiments, based on the application of the first amount of power to the first region and the second amount of power to the second region, a material on the semiconductor substrate comprises a spatially varying property on the backside of the semiconductor substrate.

[0098] In some embodiments, the material may include at least one film; and the first process and the second process collectively may include deposition of the at least one film on the backside of the semiconductor substrate, the backside facing away from a showerhead and the electrode, and facing toward a support structure, e.g., a structure such as a carrier ring configured to support the semiconductor substrate. That is, the showerhead may be above the front side of the semiconductor substrate, and the support structure may be on the backside of the semiconductor substrate.

[0099] As noted elsewhere herein, the backside film may be composed based on different chemistries and substances, and can possess internal stress, such as compressive or tensile stress, which can mitigate or otherwise address bow impacting the substrate. Hence, in some embodiments, the first process may include depositing a first film having a first internal stress on the first region of the semiconductor substrate; and the second process may include depositing a second film having a second internal stress on the second region of the semiconductor substrate; wherein the spatially varying property may include the first and second internal stresses; and wherein the first region and the second region are on the backside of the semiconductor substrate.

[0100] In some embodiments, the spatially varying property may include: a tensile stress or a compressive stress of the material varying between the first region and the second region of the semiconductor substrate; a first thickness of the material at the first region of the semiconductor substrate and a second thickness of the material at the second region of the semiconductor substrate; or a combination thereof. In some implementations, the thickness may vary up to a limit, e.g., up to 6% between the first thickness and the second thickness.

[0101] In some embodiments, the first region and the second region may include substantially parallel areas on the electrode, or concentric substantially circular areas on the electrode, or at least first and second sectors or portions of sectors on the electrode. Examples of these regions are shown in FIGS. 3 – 10B.

[0102] In some embodiments, the application of the first amount of power to the at least the first region of the electrode may occur at a first time, and the application of the second amount of power to the at least the second region of the electrode may occur at a second time different from the first time; and the at least one film comprises a first portion having a thickness that is different from a thickness of a second portion of the at least one film. For example, FIGS. 5 and 8 illustrate processes where first and second deposition steps occur at different times. However, FIGS. 4 and 7 illustrate processes where first and second power could be applied to the electrode at same or different times, influencing the thickness of the deposited film across the substrate.

[0103] In some embodiments, the application of the first amount of power to the at least the first region of the electrode and the application of the second amount of power to the at least the second region of the electrode may occur at least partly simultaneously such that a duration of the application of the first amount of power and a duration of the application of the second amount of power overlap at least partly.

[0104] In some embodiments, the process gas may include at least silane, nitrous oxide, or ammonia

[0105] In some embodiments, the support structure may include one or more portions of a carrier ring. Examples of the support structure and the carrier ring are shown in FIGS. 13 – 16.

[0106] In some embodiments, the method 1100 may optionally include detecting bow or shape of the semiconductor substrate. This may be done using metrology and optical tools configured to measure wafer bow. Other optical tools to detect angular alignment may also be used.

[0107] FIG. 12 is a flow diagram of another example method 1200 of selectively processing a semiconductor substrate, according to some embodiments. One or more of the functions of the method 1200 may be performed by or caused by a computerized apparatus or system. Structure

for performing the functionality illustrated in one or more of the blocks shown in FIG. 12 may be performed by hardware and/or software components of such computerized apparatus or system, such as, for example, a controller apparatus, a computerized system, or a computer-readable apparatus including a storage medium storing computer-readable and/or computer-executable instructions that are configured to, when executed by a processor apparatus, cause the at least one processor apparatus or a computerized apparatus to perform the operations. A controller may be one example of the computerized apparatus or system. A process chamber may be another example of the computerized apparatus or system. Example components of above apparatus are illustrated in FIGS. 13 – 17, and described in more detail elsewhere herein.

[0108] It should also be noted that the operations of FIG. 12 may be performed in any suitable order, not necessarily the order depicted in FIG. 12. Further, the process shown in FIG. 12 may include additional or fewer operations than those depicted in FIG. 12.

[0109] At block 1210, the method 1200 may include applying a first amount of power to at least a first region of an electrode and a second amount of power to at least a second region of the electrode. In some embodiments, applying the first and second amounts of power may be substantially concurrent or simultaneous. Hence, some embodiments of block 1210 may involve concurrently applying a first amount of power to at least a first region of an electrode and a second amount of power to at least a second region of the electrode.

[0110] In some embodiments, block 1210 may further include blocks 1212 and 1214. Block 1212 may include causing at least a first region of the semiconductor substrate corresponding to the first region of the electrode to undergo a first deposition process based on at least one process gas. Block 1214 may include causing at least a second region of the semiconductor substrate corresponding to the second region of the electrode to undergo a second deposition process based on the at least one process gas. In some embodiments, blocks 1212 and 1214 may be caused concurrently by applying the first and second amounts of power at block 1210.

[0111] In some embodiments, the application of the first amount of power to the at least the first region of the electrode and the application of the second amount of power to the at least the second region of the electrode may occur at least partly simultaneously such that a duration of the application of the first amount of power and a duration of the application of the second amount of power overlap at least partly.

[0112] In some embodiments, the material may include a film; the first deposition process and the second deposition process may collectively include deposition of the film on the backside of the semiconductor substrate, the backside facing away from the electrode and facing toward a structure configured to support the semiconductor substrate; and the spatially varying property

may include a first internal stress of a first film deposited on the first region of the semiconductor substrate, a first thickness of the first film, a second internal stress of a second film deposited on the second region of the semiconductor substrate, a second thickness of the second film, or a combination thereof.

[0113] For example, FIGS. 4 and 7 illustrate processes where first and second power could be applied to the electrode at the same time, influencing the thickness of the deposited film across the substrate.

Apparatus

[0114] In some embodiments, FIG. 13 is a block diagram that illustrates a substrate processing system 1300 used to perform processing on a semiconductor substrate 1302 (also referred to herein as a wafer), according to some embodiments. As shown, the substrate processing system 1300 may include a chamber 1334. A center column may be configured to support a pedestal for when a top surface of the semiconductor substrate 1302 is being processed, e.g., a film is being formed on the top surface of the semiconductor substrate 1302, or on the backside of the semiconductor substrate 1302. The pedestal, in accordance with some embodiments disclosed herein, may be referred to as a showerhead-pedestal (“ShoPed”) 1306. A showerhead 1336 may be disposed over the ShoPed 1306.

[0115] In some embodiments, the showerhead 1336 may be electrically coupled to power supply 1338 via a match network 1340. The power supply 1338 may be controlled by a control module 1342, e.g., a controller. In some embodiments, power may be provided to the ShoPed 1306 instead of the showerhead 1336. The control module 1342 may be configured to operate the substrate processing system 1300 by executing process input and control for specific process recipes. Depending on whether the top surface of the semiconductor substrate 1302 is receiving a deposited layer or layer stack or the bottom surface of the semiconductor substrate 1302 is receiving a deposited layer or layer stack, the controller module 1342 may set various operational inputs for a process recipe, such as power levels, timing parameters, process gasses, mechanical movement of a semiconductor substrate 1302, and/or the height of the semiconductor substrate 1302 relative to the ShoPed 1306.

[0116] In some embodiments, the center column may also include lift pins, which are controlled by a lift pin control. Such lift pins may be used to raise the semiconductor substrate 1302 from the ShoPed 1306 to allow an end effector (not shown) to pick the wafer and to lower the semiconductor substrate 1302 after being placed by the end effector. The end effector may also place the semiconductor substrate 1302 over spacers 1344. As will be described below, the spacers 1344

may be sized to provide a controlled separation of the semiconductor substrate 1302 between a top surface of the showerhead 1336 (facing the wafer) and a top surface of the ShoPed 1306 (facing the wafer).

[0117] In some embodiments, the substrate processing system 1332 may further include a first gas manifold 1346 that is connected to first gas sources 1348, e.g., gas chemistry supplies from a facility and/or inert gases. Depending on the processing being performed over a top surface of the semiconductor substrate 1302, the control module 1342 may controls the delivery of first gas sources 1348 via the first gas manifold 1346. The chosen gases may then be flown into the showerhead 1336 and distributed in a space volume defined between a face of the showerhead 1336 that faces that semiconductor substrate 1302 when the wafer is resting over the pedestal.

[0118] In some embodiments, the substrate processing system 1332 may further include a second gas manifold 1350 that is connected to second gas sources 1352, e.g., gas chemistry supplies from a facility and/or inert gases. Depending on the processing being performed over a bottom surface of the semiconductor substrate 1302, the control module 1342 may control the delivery of second gas sources 1352 via the second gas manifold 1350. The chosen gases may then be flown into the showerhead 1336 and distributed in a space volume defined between a face of the ShoPed 1306 that faces an under surface or under side (e.g., backside) of the semiconductor substrate 1302 when the wafer is resting over the spacers 1344. The spacers 1344 may provide for a separation that optimizes deposition to the under surface of the semiconductor substrate 1302, while reducing deposition over the top surface of the semiconductor substrate 1302. In some embodiments, while deposition is targeted for the under surface of the semiconductor substrate 1302, an inert gas may be flown over the top surface of the semiconductor substrate 1302 via the showerhead 1336, which may push reactant gases away from the top surface and enable reactant gases provided from the ShoPed 1306 to be directed to the under surface of the semiconductor substrate 1302.

[0119] In some embodiments, either showerhead 1336 or ShoPed 1306 may have a zonal deposition design similar to that shown in FIG. 18A. For example, gas manifold 1350 may be fluidically linked to control the delivery of gases to either zones 1802 or zone 1804. By controlling the flow of gases to either zones 1802 or zone 1804 films may be deposited as shown in FIGS. 18B and 18C.

[0120] Further, the gases may be premixed or not. Appropriate valving and mass flow control mechanisms may be employed to ensure that the correct gases are delivered during the deposition and plasma treatment phases of the process. Process gases may exit the chamber 1334 via an outlet. A vacuum pump (e.g., a one or two stage mechanical dry pump and/or a turbomolecular pump)

may draw process gases out and maintains a suitably low pressure within the reactor by a close loop-controlled flow restriction device, such as a throttle valve or a pendulum valve.

[0121] In some embodiments, a carrier ring 1354 may encircle an outer region of the ShoPed 1306. When the top surface of the semiconductor substrate 1302 is being processed, e.g., a material is being deposited thereon, the carrier ring 1354 may be configured to sit over a carrier ring support region that is a step down from a wafer support region in the center of the ShoPed 1306. The top surface of the carrier ring 1354 is generally coplanar with the top surface of the semiconductor substrate 1302. The carrier ring 1354 may include an outer edge side of its disk structure, e.g., outer radius, and a wafer edge side of its disk structure, e.g., inner radius, that is closest to where the semiconductor substrate 1302 sits. The carrier ring 1354 may be associated with an inner diameter (ID). The inner diameter may extend to an inner perimeter of the carrier ring and generally surround a substrate (e.g., semiconductor substrate 1302) in a processing chamber. The wafer edge side of the carrier ring 1354 may also include a plurality of contact support structures or “tabs” which may be configured to lift the semiconductor substrate 1302 when the carrier ring 1354 is held by the spacers 1344. The carrier ring 1354 may include a plurality of tabs with a quantity selected from a range to support the semiconductor substrate 1302 during processing. Additional details regarding embodiments of the tabs will follow.

[0122] FIG. 14 is a block diagram that illustrates another substrate processing system 1400 used to perform processing on a semiconductor substrate 1402 (also referred to herein as a wafer), according to some embodiments. In some embodiments, spider forks 1456 may be used to lift and maintain the carrier ring 1454 in its process height, e.g., to allow depositing in the under surface (backside) of the semiconductor substrate 1402. The carrier ring 1454 may therefore be lifted along with the semiconductor substrate 1402. In some implementations, the carrier ring 1454 may be rotated to another station, e.g., in a multi-station system.

[0123] Broadly speaking, the embodiments disclosed herein are for a system to deposit PECVD films on the selective side of the wafer (front and/or back) with dynamic control. Some embodiments may include a dual gas-flowing electrode for defining a capacitively-coupled PECVD system. The system may include a gas-flowing showerhead (e.g., showerhead 1436) and a ShoPed 1406. In some embodiments, the gas-flowing pedestal (i.e., ShoPed) is a combination showerhead and pedestal, which enables deposition on a back-side of the wafer. The electrode geometry combines features of a showerhead, e.g., a gas mixing plenum, holes, hole-pattern, gas jet preventing baffle, and features of a pedestal. Examples of features of a pedestal include an embedded controlled heater, wafer-lift mechanisms, ability to hold plasma suppression rings, and

movability. This enables the transfer of wafers and the processing of gasses with or without RF power from the pedestal.

[0124] In some embodiments, the system may have a wafer lift mechanism that tightly controls parallelism of the substrates against the electrodes. In one example, this may be achieved by setting up the lift mechanism parallel to the two electrodes and controlling manufacturing tolerances, e.g., spindle or lift pins mechanisms. In another example, the lift may be achieved by raising the wafer lift parts. This option may not allow dynamic control of the side that gets deposited.

[0125] In some configurations, the lift mechanism may allow dynamically controlling the substrate position during processing (before plasma, during plasma, after plasma) to control the side of the deposition, profile of the deposition, and deposition film properties. The system may further allow selective enabling/disabling of the side where reactants are flown. One side can flow the reactant and the other side can flow inert gases to suppress the deposition and plasma.

[0126] In some embodiments, the gap between the side of the wafer that does not need plasma/dep may be tightly controlled. This distance may be controlled to suppress plasma. By not controlling the distance, the wafer may be susceptible to plasma damage. For example, the system may allow a minimal gap from about 2 mm to about 0.5 mm, and in another embodiment from about 1 mm to about .05 (limited by the wafer bow), and such gap can be controlled. The gap may be controlled depending on process conditions.

[0127] In some embodiments, the gas-flowing pedestal (i.e., ShoPed) may enable, without limitation: (a) thermal stabilization of the wafer to processing temperature prior to processing; (b) selective design of hole patterns on the ShoPed to selectively deposit film in different areas of the back-side of the wafer; (c) swappable rings can be attached to achieve appropriate plasma confinement and hole pattern; (d) stable wafer transfer mechanisms within chamber and for transferring wafer outside to another chamber or cassette – such as lift pins, RF-coupling features, minimum-contact arrays; (e) implement gas mixing features, e.g., such as inner plenum, baffle and manifold lines openings; and (f) add compartments in the gas-flowing pedestal (i.e., ShoPed) to enable selective gas flow to different regions of the back side of the wafer and control flow rates via flow controllers and/or multiple plenums.

[0128] In another embodiment, dynamic gap control using wafer lift mechanism enables: (a) control of the distance from deposition or reactant flowing electrode to the side of the wafer that needs deposition or in the middle so that both sides can be deposited; and (b) the lift mechanism to control the distance dynamically during the process (before plasma, during plasma, after plasma) to control the side of the deposition, profile of the deposition, and deposition film properties. In another embodiment, for a deposition mode used to deposit on the backside of the wafer, film edge

exclusion control is highly desirable to avoid lithography-related overlay problems. The lift mechanism used in this system is done via a carrier ring 1454 that has a design feature to shadow the deposition on the edge. This specifies the edge exclusion control via the design and shape of the carrier ring.

[0129] FIG. 15A shows a cross-sectional view of an edge region of the ShoPed 1506 (e.g., 1306, 1406). This view provides a cross-sectional representation of a carrier ring 1554 (e.g., 1354, 1454), which has a carrier ring inner radius 1554a and a carrier ring outer radius 1554b. In some embodiments, the carrier ring 1554 includes support extensions 1554c, which extend below the substantial flat surface of the carrier ring 1554.

[0130] The support extensions 1554c are configured to mate and sit within support surfaces defined into a top surface of the spacers 1544. The support surfaces provide a complementary mating surface for the support extensions 1554c, such that the carrier ring 1554 is prevented from sliding or moving when supported by the spacers 1544. Although three spacers are shown as spacers 1544 are shown in FIG. 15, it is envisioned that any number of spacers may be provided, so long as the carrier ring can be supported substantially parallel to the surface of the ShoPed 1506, and spacing is defined for supporting semiconductor substrate 1502 at a spaced apart relationship from a top surface of the ShoPed 1506.

[0131] Further shown is that a top surface of the ShoPed 1506 will include a hole pattern 1506a that is distributed throughout the surface to provide even distribution and output of gases during operation. In one embodiment, the hole pattern 1506a is distributed in a plurality of concentric rings that start at the center of the top surface of the ShoPed 1506 and extend to an outer periphery of the ShoPed 1506. At least one hole pattern 1506a is provided at an edge hole region 1507 of the hole pattern, and orifices defined in the edge hole region 1507 are preferably angled to provide gases non-perpendicular to the surface of the ShoPed 1506.

[0132] In one example, the angle or tilt at which the orifices in the edge hole region 1507 is defined to tilt or angle away from the center of the ShoPed 1506. In one embodiment, the angle is approximately 45° from horizontal. In other embodiments, the angle can vary between 20° from horizontal to about 80° from horizontal. In one embodiment, by providing the angled orifices in the edge hole region 1507, additional distribution of process gases can be provided during backside deposition of the semiconductor substrate 1502. In one embodiment, the remainder orifices 1506d of the hole pattern 1506a are oriented substantially perpendicular to the surface of the ShoPed 1506 and directed toward the underside of the semiconductor substrate 1502.

[0133] FIG. 15B illustrates that when the semiconductor substrate 1502 is held by the carrier ring 1554, the semiconductor substrate 1502 edge will sit on an edge region closer to the carrier

ring inner radius 1554a of the carrier ring 1554. The surface of the showerhead 1536 facing the top surface of the semiconductor substrate 1502, when positioned using spacers 1544, may be substantially close to prevent deposition during a mode where deposition is being carried out to the backside of the semiconductor substrate 1502.

[0134] By way of example, the distance between the top of the semiconductor substrate 1502 and the surface of the showerhead 1536 is preferably between about 2 mm to about .5 mm, and in some embodiments about 1 mm to about .5 mm, depending on the wafer bow. That is, if the wafer is bowed substantially, the separation will be about .5 mm or larger. If the wafer is not yet bowed substantially, the separation can be less than about .5 mm. In one embodiment, it is preferable that the separation be minimized to prevent deposition on the top side of the substrate when the backside of the substrate is being deposited with a layer of material. In some embodiments, the showerhead 1536 is configured to supply an inert gas flow over the top side of the semiconductor substrate 1502 during when the backside of the substrate is being deposited and deposition gases are being supplied by the ShoPed 1506.

[0135] Any suitable chamber may be used to implement the disclosed embodiments. Example deposition apparatuses include various systems, e.g., ALTUS® and ALTUS® Max, available from Lam Research Corp., of Fremont, California, or any of a variety of other commercially available processing systems.

[0136] FIG. 16 is a diagram of a cross-sectional view of a processing system 1600 for depositing film on a semiconductor substrate, according to some embodiments herein. In some embodiments, the processing system 1600 may include a showerhead 1602, a shower-pedestal (ShoPed) 1604, one or more support structures 1606 (e.g., a carrier ring 1354, 1454, 1554 and/or tabs of a carrier ring, or spider forks 1456). The one or more support structures 1606 may be configured to support a semiconductor substrate 1620. In some implementations, the one or more support structures 1606 may be coupled to the ShoPed 1604 and/or other structures associated with the processing system 1600, e.g., processing chamber wall(s). In some implementations, electrostatic chucking (e.g., bipolar chucking or monopolar chucking) may be used to further secure the semiconductor substrate 1620.

[0137] In some embodiments, the showerhead 1602 may include an electrode 1610 operable by providing RF power to a plurality of zones. For example, there may be two distinct zones configured to receive different amounts of RF power at different or substantially concurrent times (e.g., FIG. 6, 10A). In another example, there may be three distinct zones (e.g., FIG. 3). In other examples, there may be four or more (e.g., FIGS. 9, 10B). The RF power provided to two or more (or in some cases all) of the zones may be the same amount.

[0138] In some implementations, the electrode 1610 may be integrated or embedded into the showerhead 1602. The electrode 1610 may have a specific configuration of zones according to wafer bow and/or other requirements. Examples of zones are discussed above. In certain implementations, however, the electrode 1610 may be a distinct component that may be replaced and installed into the showerhead 1602 without breaking the showerhead 1602. Such interchangeable electrodes may be useful for performing different customized backside film deposition of the type discussed in the present disclosure. For instance, an electrode having three zones may be swapped for one having two zones to correct different types of wafer bow.

[0139] In some embodiments, the ShoPed 1604 may have one or more gas inlets 1605 configured to transport and emit process gas 1607. Examples of process gas 1607 may include silane (SiH_4), nitrous oxide (N_2O), and/or ammonia (NH_3). Inert carrier gases (e.g., argon, neon, or helium) may also be transported through and out of the ShoPed 1604. In some cases, a mixture of process gas and carrier gas may be routed through the showerhead 1602 and emitted therefrom. Different types of film material may be deposited on the semiconductor substrate 1620 based on the type of process gas. The showerhead 1602 may have one or more gas inlets 1603 configured to receive and disperse purge gas 1608, such as nitrogen. Purge gas 1608 flowing along the top or front side of the semiconductor substrate 1620 may be used to prevent the process gas 1607 from the ShoPed 1604 or impurities from reaching the top or front side of the semiconductor substrate 1620.

[0140] In some embodiments, the semiconductor substrate 1620 may be placed and supported at a position that is closer to the showerhead 1602 than to the ShoPed 1604. In example implementation, the distance of the gap 1612 between the showerhead 1602 and the semiconductor substrate 1620 may be about 1 mm, while the distance of the gap 1614 between the ShoPed 1604 and the semiconductor substrate 1620 may be about 12 mm. Various distances may be used. However, it is notable and useful that the gap 1612 is small (e.g., small enough to not allow a plasma to form) and could be much smaller than the gap 1614. This is to prevent plasma 1615 from developing between the showerhead 1602 and the semiconductor substrate 1620 where the front side of the semiconductor substrate 1620 is. That is, the plasma 1615 is encouraged to form at the backside 1625 of the semiconductor substrate 1620, where the backside faces away from the showerhead 1602 and the electrode 1610, and faces toward the ShoPed 1604 and/or support structures 1606. The front side may have sensitive and expensive features (transistors, memory cells, wiring lines, etc.). In some implementations, a flowing purge gas out of holes in the showerhead 1602 may push away any process gas or precursor that might have been left or transported to the front side.

[0141] As already discussed herein, by specifying the amount of RF power provided to different zones of the electrode 1610, and at different times in some implementations, film material having properties varying spatially across the semiconductor substrate 1620 may be formed. Some examples of film properties include internal stress (e.g., tensile stress or a compressive stress) and film thickness.

[0142] FIG. 17 is a schematic of a process system suitable for conducting deposition processes, such as frontside deposition processes, in accordance with embodiments. The system 1700 includes a transfer module 1703. The transfer module 1703 provides a clean, pressurized environment to minimize risk of contamination of substrates being processed as they are moved between various reactor modules. Mounted on the transfer module 1703 is a multi-station reactor 1709 capable of performing ALD, treatment, and CVD according to various embodiments. Multi-station reactor 1709 may include multiple stations 1711, 1713, 1715, and 1717 that may sequentially perform operations in accordance with disclosed embodiments. Stations may include a heated pedestal or substrate support, one or more gas inlets or showerhead or dispersion plate.

[0143] Mounted on the transfer module 1703 may be one or more single or multi-station modules 1707 capable of performing plasma or chemical (non-plasma) pre-cleans, other deposition operations, or etch operations. The module may also be used for various treatments to, for example, prepare a substrate for a deposition process. The system 1700 also includes one or more wafer source modules 1701, where wafers are stored before and after processing. An atmospheric robot (not shown) in the atmospheric transfer chamber 1719 may first remove wafers from the wafer source modules 1701 to loadlocks 1721. A wafer transfer device (generally a robot arm unit) in the transfer module 1703 moves the wafers from loadlocks 1721 to and among the modules mounted on the transfer module 1703.

[0144] In various embodiments, a system controller 1742 is employed to control process conditions during deposition. The system controller 1742 will typically include one or more memory devices and one or more processors. A processor may include a CPU or computer, analog and/or digital input/output connections, stepper motor controller boards, etc.

[0145] The system controller 1742 may control all the activities of the deposition apparatus. The system controller 1742 executes system control software, including sets of instructions for controlling the timing, mixture of gases, chamber pressure, chamber temperature, wafer temperature, radio frequency (RF) power levels, wafer chuck or pedestal position, and other parameters of a particular process. Other computer programs stored on memory devices associated with the system controller 1742 may be employed in some embodiments.

[0146] The depicted embodiment includes a user interface associated with the system controller 1742. The user interface may include a display screen, graphical software displays of the apparatus and/or process conditions, and user input devices such as pointing devices, keyboards, touch screens, microphones, etc.

[0147] System control logic may be configured in any suitable way. In general, the logic can be designed or configured in hardware and/or software. The instructions for controlling the drive circuitry may be hard coded or provided as software. The instructions may be provided by “programming.” Such programming is understood to include logic of any form, including hard coded logic in digital signal processors, application-specific integrated circuits, and other devices which have specific algorithms implemented as hardware. Programming is also understood to include software or firmware instructions that may be executed on a general-purpose processor. System control software may be coded in any suitable computer readable programming language.

[0148] The computer program code for controlling the processes in a process sequence can be written in any conventional computer readable programming language: for example, assembly language, C, C++, Pascal, Fortran, or others. Compiled object code or script is executed by the processor to perform the tasks identified in the program. Also as indicated, the program code may be hard coded.

[0149] The controller parameters relate to process conditions, such as, for example, process gas composition and flow rates, temperature, pressure, cooling gas pressure, substrate temperature, and chamber wall temperature. These parameters are provided to the user in the form of a recipe and may be entered utilizing the user interface.

[0150] Signals for monitoring the process may be provided by analog and/or digital input connections of the system controller 1742. The signals for controlling the process are output on the analog and digital output connections of the system 1700.

[0151] The system software may be designed or configured in different ways. For example, various chamber component subroutines or control objects may be written to control operation of the chamber components necessary to carry out the deposition processes in accordance with the disclosed embodiments. Examples of programs or sections of programs for this purpose include substrate positioning code, process gas control code, pressure control code, and heater control code.

[0152] In some implementations, a system controller 1742 is part of a system, which may be part of the above-described examples. Such systems can include semiconductor processing equipment, including a processing tool or tools, chamber or chambers, a platform or platforms for

processing, and/or specific processing components (a wafer pedestal, a gas flow system, etc.). These systems may be integrated with electronics for controlling their operation before, during, and after processing of a semiconductor wafer or substrate. The electronics may be referred to as the “controller,” which may control various components or subparts of the system or systems. The system controller 1742, depending on the processing requirements and/or the type of system, may be programmed to control any of the processes disclosed herein, including the delivery of processing gases, temperature settings (e.g., heating and/or cooling), pressure settings, vacuum settings, power settings, radio frequency (RF) generator settings in some systems, RF matching circuit settings, frequency settings, flow rate settings, fluid delivery settings, positional and operation settings, wafer transfers into and out of a tool and other transfer tools and/or load locks connected to or interfaced with a specific system.

[0153] Anisotropic internal stress may be accomplished by depositing curved bar profile and curved channel profile films. FIGS. 18A – 18C illustrate curved bar and curved channel profile films. FIG. 18A is a top-side view of a semiconductor substrate (wafer) 1806 having a center zone 1804 and edge zones 1802. FIGS. 18B and 18C present a side view and exploded side view, respectively, along the x dimension of the wafer 1806 having a curved bar profile film 1808 and a curved channel profile film 1807. A film may be deposited such that the film is substantially deposited in either center zone 1804 or edge zones 1802. A film deposited substantially in center zone 1804 will have curved bar profile 1808, while a film deposited substantially in edge zones 1802 will have curved channel profile 1807. While films may be deposited substantially in either center zone 1804 or edge zones 1802, it should be understood that some deposition may occur across the wafer and in the other zone. Furthermore, the shapes of the curved bar profile and curved channel profile are mere examples and variations in profile shape may occur. In some embodiments, center zone 1804 may also be referred to as a curved bar profile deposition zone. In some embodiments, edge zones 1802 may also be referred to as a curved channel profile deposition zone.

[0154] The curved bar profile film 1808 has a decreasing thickness along an x dimension from center to edge of wafer 1806 and a uniform thickness along a y dimension of the wafer. Conversely, the curved channel profile film 1807 has an increasing thickness along the x dimension from center to edge of wafer 1806 and a uniform thickness along a y dimension of the wafer. Together, curved bar profile film 1808 and curved channel profile film 1807 may form a uniform profile film that is substantially flat.

[0155] As film 1807 and film 1808 are deposited independently, each film may be deposited under conditions to have a different internal stress. For example, curved bar profile film 1808 may

have a compressive internal stress, while curved channel profile film 1807 may have a tensile internal stress. As film stresses may be superimposed, the stacked film may have a compressive internal stress in areas of the film having a small x/large y coordinate, i.e., corresponding to center zone 1804, while the stacked film also has a tensile internal stress in areas of the film having a large x/small y coordinate, i.e., coordinating to edge zones 1802.

[0156] While films 1807 and 1808 are discussed herein as having opposite types of internal stress, e.g., one film has a compressive internal stress and the other film has a tensile internal stress, in some embodiments both films may have a tensile or compressive internal stress, but different magnitudes of internal stress. This may address wafers that have different magnitudes of x-bow and y-bow even if the both bows are positive or negative. In some embodiments depositing same type stress films may increase throughput.

System Controllers

[0157] Broadly speaking, a controller may be defined as electronics having various integrated circuits, logic, memory, and/or software that receive instructions, issue instructions, control operation, enable cleaning operations, enable endpoint measurements, and the like. Such controller may be used in or with any of the apparatus described herein. The integrated circuits may include chips in the form of firmware that store program instructions, digital signal processors (DSPs), chips defined as application specific integrated circuits (ASICs), and/or one or more microprocessors, or microcontrollers that execute program instructions (e.g., software). Program instructions may be instructions communicated to the controller in the form of various individual settings (or program files), defining operational parameters for carrying out a particular process on or for a semiconductor wafer or to a system. The operational parameters may, in some embodiments, be part of a recipe defined by process engineers to accomplish one or more processing steps during the fabrication of one or more layers, materials, metals, oxides, silicon, silicon dioxide, surfaces, circuits, and/or dies of a wafer.

[0158] A system controller may be a part of or coupled to a computer that is integrated with, coupled to the system, otherwise networked to the system, or a combination thereof. For example, a system controller may be in the “cloud” or all or a part of a fab host computer system, which can allow for remote access of the wafer processing. The computer may enable remote access to the system to monitor current progress of fabrication operations, examine a history of past fabrication operations, examine trends or performance metrics from a plurality of fabrication operations, to change parameters of current processing, to set processing steps to follow a current processing, or to start a new process. In some examples, a remote computer (e.g. a server) can provide process recipes to a system over a network, which may include a local network or the Internet. The remote

computer may include a user interface that enables entry or programming of parameters and/or settings, which are then communicated to the system from the remote computer. In some examples, the controller receives instructions in the form of data, which specify parameters for each of the processing steps to be performed during one or more operations. It should be understood that the parameters may be specific to the type of process to be performed and the type of tool that the controller is configured to interface with or control. Thus, as described above, the controller may be distributed, such as by including one or more discrete controllers that are networked together and working towards a common purpose, such as the processes and controls described herein. An example of a distributed controller for such purposes would be one or more integrated circuits on a chamber in communication with one or more integrated circuits located remotely (such as at the platform level or as part of a remote computer) that combine to control a process on the chamber.

[0159] Without limitation, example systems may include a plasma etch chamber or module, a deposition chamber or module, a spin-rinse chamber or module, a metal plating chamber or module, a clean chamber or module, a bevel edge etch chamber or module, a physical vapor deposition (PVD) chamber or module, a CVD chamber or module, an ALD chamber or module, an atomic layer etch (ALE) chamber or module, an ion implantation chamber or module, a track chamber or module, and any other semiconductor processing systems that may be associated or used in the fabrication and/or manufacturing of semiconductor wafers.

[0160] As noted above, depending on the process step or steps to be performed by the tool, the controller might communicate with one or more of other tool circuits or modules, other tool components, cluster tools, other tool interfaces, adjacent tools, neighboring tools, tools located throughout a factory, a main computer, another controller, or tools used in material transport that bring containers of wafers to and from tool locations and/or load ports in a semiconductor manufacturing factory.

[0161] A system controller may include various programs. A substrate positioning program may include program code for controlling chamber components that are used to load the substrate onto a pedestal or chuck and to control the spacing between the substrate and other parts of the chamber such as a gas inlet and/or target. A process gas control program may include code for controlling gas composition, flow rates, pulse times, and optionally for flowing gas into the chamber prior to deposition in order to stabilize the pressure in the chamber. A pressure control program may include code for controlling the pressure in the chamber by regulating, e.g., a throttle valve in the exhaust system of the chamber. A heater control program may include code for controlling the

current to a heating unit that is used to heat the substrate. Alternatively, the heater control program may control delivery of a heat transfer gas such as helium to the wafer chuck

[0162] Examples of chamber sensors that may be monitored during deposition include mass flow controllers, pressure sensors such as manometers, and thermocouples located in the pedestal or chuck. Appropriately programmed feedback and control algorithms may be used with data from these sensors to maintain desired process conditions.

[0163] The foregoing describes implementation of disclosed embodiments in a single or multi-chamber semiconductor processing tool. The apparatus and process described herein may be used in conjunction with lithographic patterning tools or processes, for example, for the fabrication or manufacture of semiconductor devices, displays, LEDs, photovoltaic panels, and the like. Typically, though not necessarily, such tools/processes will be used or conducted together in a common fabrication facility. Lithographic patterning of a film typically includes some or all of the following steps, each step provided with a number of possible tools: (1) application of photoresist on a workpiece, i.e., substrate, using a spin-on or spray-on tool; (2) curing of photoresist using a hot plate or furnace or UV curing tool; (3) exposing the photoresist to visible or UV or x-ray light with a tool such as a wafer stepper; (4) developing the resist so as to selectively remove resist and thereby pattern it using a tool such as a wet bench; (5) transferring the resist pattern into an underlying film or workpiece by using a dry or plasma-assisted etching tool; and (6) removing the resist using a tool such as an RF or microwave plasma resist stripper.

Conclusion

[0164] Although the foregoing embodiments have been described in some detail for purposes of clarity of understanding, it will be apparent that certain changes and modifications may be practiced within the scope of the appended claims. Embodiments disclosed herein may be practiced without some or all of these specific details. In other instances, well-known process operations have not been described in detail to not unnecessarily obscure the disclosed embodiments. Further, while the disclosed embodiments will be described in conjunction with specific embodiments, it will be understood that the specific embodiments are not intended to limit the disclosed embodiments. It should be noted that there are many alternative ways of implementing the processes, systems, and apparatus of the present embodiments. Accordingly, the present embodiments are to be considered as illustrative and not restrictive, and the embodiments are not to be limited to the details given herein.

CLAIMS

What is claimed is:

1. An apparatus configured to selectively process a semiconductor substrate, the apparatus comprising:
 - a showerhead configured to deliver at least one process gas to a backside of the semiconductor substrate;
 - an electrode having at least a first region and a second region associated therewith;
 - a support structure configured to receive the semiconductor substrate and disposed between the showerhead and the electrode; and
 - a controller coupled to the showerhead and the electrode, and configured to:
 - apply a first amount of power to at least the first region of the electrode, causing at least the first region of the semiconductor substrate to undergo a first process based on the at least one process gas; and
 - apply a second amount of power different from the first amount of power to at least a second region of the electrode, causing at least the second region the semiconductor substrate to undergo a second process based on the at least one process gas;

wherein, based on the application of the first amount of power to the first region and the second amount of power to the second region, a material on the semiconductor substrate comprises a spatially varying property on the backside of the semiconductor substrate.
2. The apparatus of claim 1, wherein:
 - the material comprises at least one film; and
 - the first process and the second process collectively comprise deposition of the at least one film on the backside of the semiconductor substrate, the backside facing away from the showerhead and the electrode, and facing toward the support structure.
3. The apparatus of claim 1, wherein:
 - the first process comprises depositing a first film having a first internal stress on the first region of the semiconductor substrate;
 - the second process comprises depositing a second film having a second internal stress on the second region of the semiconductor substrate;
 - the spatially varying property comprises the first and second internal stresses; and

the first region and the second region are on the backside of the semiconductor substrate.

4. The apparatus of claim 1, wherein the spatially varying property comprises:
a tensile stress or a compressive stress of the material varying between the first region of the semiconductor substrate and the second region of the semiconductor substrate;
a first thickness of the material at the first region of the semiconductor substrate and a second thickness of the material at the second region of the semiconductor substrate; or
a combination thereof.

5. The apparatus of claim 1, wherein the first region and the second region comprise substantially parallel areas on the electrode.

6. The apparatus of claim 1, wherein the first region and the second region comprise concentric substantially circular areas on the electrode.

7. The apparatus of claim 1, wherein the first region and the second region comprise first and second sectors or portions of sectors on the electrode.

8. The apparatus of claim 1, wherein:
the application of the first amount of power to the at least the first region of the electrode occurs at a first time, and the application of the second amount of power to the at least the second region of the electrode occurs at a second time different from the first time; and
the material comprises at least one film that comprises a first portion having a thickness that is different from a thickness of a second portion of the at least one film.

9. The apparatus of claim 1, wherein the application of the first amount of power to the at least the first region of the electrode and the application of the second amount of power to the at least the second region of the electrode occur at least partly simultaneously such that a duration of the application of the first amount of power and a duration of the application of the second amount of power overlap at least partly.

10. The apparatus of claim 1, wherein the process gas comprises at least silane, nitrous oxide, or ammonia.

11. The apparatus of claim 1, wherein the support structure comprises one or more portions of a carrier ring.

12. A method of selectively processing a semiconductor substrate, the method comprising:

applying a first amount of power to at least a first region of an electrode, causing at least a first corresponding region of the semiconductor substrate to undergo a first deposition process based on at least one process gas; and

applying a second amount of power different from the first amount of power to at least a second region of the electrode, causing at least a second corresponding region the semiconductor substrate to undergo a second deposition process based on the at least one process gas;

wherein, based on the application of the first amount of power to the first region and the second amount of power to the second region, a material on the semiconductor substrate comprises a spatially varying property on a backside of the semiconductor substrate.

13. The method of claim 12, wherein:

the material comprises at least one film; and

the first deposition process and the second deposition process collectively comprise deposition of the at least one film on the backside of the semiconductor substrate, the backside facing away from the electrode and facing toward a structure configured to support the semiconductor substrate.

14. The method of claim 12, wherein the spatially varying property comprises:

a tensile stress or a compressive stress of the material varying between the first corresponding region of the semiconductor substrate and the second corresponding region of the semiconductor substrate;

a first thickness of the material at the first corresponding region of the semiconductor substrate and a second thickness of the material at the second corresponding region of the semiconductor substrate; or

a combination thereof.

15. The method of claim 12, wherein the first region and the second region comprise

substantially parallel areas on the electrode, concentric substantially circular areas on the electrode, or first and second sectors or portions of sectors on the electrode.

16. The method of claim 12, wherein:

the application of the first amount of power to the at least the first region of the electrode occurs at a first time, and the application of the second amount of power to the at least the second region of the electrode occurs at a second time different from the first time; and

the material comprises at least one film that comprises a first portion having a thickness that is different from a thickness of a second portion of the at least one film.

17. The method of claim 12, wherein the application of the first amount of power to the at least the first region of the electrode and the application of the second amount of power to the at least the second region of the electrode occur at least partly simultaneously such that a duration of the application of the first amount of power and a duration of the application of the second amount of power overlap at least partly.

18. A method of selectively processing a semiconductor substrate, the method comprising:

concurrently applying a first amount of power to at least a first region of an electrode and a second amount of power to at least a second region of the electrode, causing at least a first region of the semiconductor substrate corresponding to the first region of the electrode to undergo a first deposition process based on at least one process gas, and at least a second region of the semiconductor substrate corresponding to the second region of the electrode to undergo a second deposition process based on the at least one process gas;

wherein, based on the application of the first amount of power to the first region and the second amount of power to the second region, a material on the semiconductor substrate comprises a spatially varying property on a backside of the semiconductor substrate.

19. The method of claim 18, wherein the application of the first amount of power to the at least the first region of the electrode and the application of the second amount of power to the at least the second region of the electrode occur at least partly simultaneously such that a duration of the application of the first amount of power and a duration of the application of the second amount of power overlap at least partly.

20. The method of claim 18, wherein:

the material comprises a film;

the first deposition process and the second deposition process collectively comprise deposition of the film on the backside of the semiconductor substrate, the backside facing away

from the electrode and facing toward a structure configured to support the semiconductor substrate; and

the spatially varying property comprises a first internal stress of a first film deposited on the first region of the semiconductor substrate, a first thickness of the first film, a second internal stress of a second film deposited on the second region of the semiconductor substrate, a second thickness of the second film, or a combination thereof.