CLAIMS

1. A device comprising:

a first circuit coupled to first and second power rails of the device, the first circuit is subject to a latch up event in the presence of a latch up condition, the latch up event includes a low resistance path created between the first and second power rails;

a latch up sensing (LUS) circuit coupled to the first circuit, wherein the LUS circuit is configured to receive a LUS input signal from the first circuit and generates a LUS output signal to the first circuit, wherein

when the input signal is an active latch up signal which indicates the presence of a latch up condition, the LUS circuit generates an active LUS output signal which creates a break in the low resistance path to terminate the latch up event.

2. The device of claim 1 wherein the first circuit includes a pnpn structure.

3. The device of claim 1 wherein the first circuit includes an inverter.

4. The device of claim 3 wherein the inverter includes a parasitic circuit having a first parasitic bipolar transistor Q1 and a second parasitic bipolar transistor Q2.

5. The device of claim 4 wherein the break in the low resistance path is created by switching off Q1.

6. The device of claim 1 wherein the LUS circuit includes first and second transistors coupled in series between the first and second power rails.

7. The device of claim 6 wherein the first power rail is V_{DD} and the second power rail is V_{SS}.

8. The device of claim 6 wherein the first transistor is a p-type MOS transistor and the second transistor is a n-type MOS transistor.

9. The device of claim 6 wherein the first transistor includes first and second terminals, a body and a gate terminal, wherein the first terminal and body of the first transistor are coupled to the first power rail and the second terminal is coupled to an output of the LUS circuit.

10. The device of claim 9 wherein the second transistor includes first and second terminals, a body and a gate terminal, wherein the first terminal and body of the second transistor are coupled to the second power rail and the second terminal of the second transistor is coupled to the gate terminal of the first transistor.

11. The device of claim 10 wherein the gate terminal of the second transistor is coupled to an input of the LUS circuit.

12. A method of forming a device comprising:

providing a substrate for the device;

forming a first circuit on the substrate, the first circuit is coupled to first and second power rails of the device, the first circuit is subject to a latch up event in the presence of a latch up condition, the latch up event includes a low resistance path created between the first and second power rails; and

forming a latch up sensing (LUS) circuit on the substrate, the LUS circuit is coupled to the first circuit, wherein the LUS circuit is configured to receive a LUS input signal from the first circuit and generates a LUS output signal to the first circuit, wherein

when the input signal is an active latch up signal which indicates the presence of a latch up condition, the LUS circuit generates an active LUS output signal which creates a break in the low resistance path to terminate the latch up event.

13. The method of claim 12 wherein forming the first circuit includes forming a pnpn structure on the substrate.

14. The method of claim 12 wherein forming the first circuit includes forming an inverter on the substrate.

15. The method of claim 14 wherein the inverter includes a parasitic circuit having a first parasitic bipolar transistor Q1 and a second parasitic bipolar transistor Q2.

16. The method of claim 15 wherein the break in the low resistance path is created by switching off Q1.

17. The method of claim 12 wherein forming the LUS circuit includes forming first and second transistors coupled in series between the first and second power rails.

18. The method of claim 17 wherein the first power rail is V_{DD} and the second power rail is V_{SS}.

19. The method of claim 17 wherein the first transistor is a p-type MOS transistor and the second transistor is a n-type MOS transistor.

20. A method of forming a device comprising:

providing a substrate for the device;

forming a first circuit on the substrate, the first circuit is coupled to first and second power rails of the device, the first circuit is subject to a latch up event in the presence of a latch up condition, the latch up event includes a low resistance path created between the first and second power rails; and

forming a latch up sensing (LUS) circuit coupled to the first circuit on the substrate, the LUS circuit includes first and second transistors coupled in series between the first and second power rails, wherein the LUS circuit is configured to receive a LUS input signal from the first circuit and generates a LUS output signal to the first circuit, wherein

when the input signal is an active latch up signal which indicates the presence of a latch up condition, the LUS circuit generates an active LUS output signal which creates a break in the low resistance path to terminate the latch up event.

1. A device comprising:

a first circuit directly coupled to both first and second power rails of the device, the first circuit comprises complementary metal oxide semiconductor (CMOS) transistors, the first circuit is subject to a latch up event in the presence of a latch up condition, the latch up event includes a low resistance path created between the first and second power rails;

a latch up sensing (LUS) circuit, wherein the LUS circuit senses a latch up condition in the first circuit and terminates the latch up event when the latch up condition is sensed, the LUS circuit and the first circuit are distinct circuits, the LUS circuit is coupled to the first circuit, wherein the LUS circuit is configured to receive a LUS input signal at a LUS input from the first circuit and generate a LUS output signal at a LUS output to the first circuit, the LUS input signal and LUS output signal comprise voltage signals, wherein

the LUS circuit includes first and second transistors coupled in between the first and second power rails,

the first transistor is a p-type MOS transistor and includes a first p-transistor terminal, a second p-transistor terminal, a p-transistor body, and a p-transistor gate terminal, wherein the first p-transistor terminal is coupled to the first power rail, the second p-transistor terminal is coupled to the LUS output of the LUS circuit, and the p-transistor body is coupled to the first p-transistor terminal,

the second transistor is a n-type MOS transistor and includes a first n-transistor terminal, a second n-transistor terminal, a n-transistor body, and a n-transistor gate terminal, wherein the first n-transistor terminal is coupled to the second power rail, the second n-transistor terminal is coupled to the p-transistor gate terminal, the n-transistor

gate terminal is coupled to the LUS input of the LUS circuit, and the n-transistor body is coupled to the first n-transistor terminal, and

when the input signal is an active latch up signal which indicates the presence of the latch up condition, the LUS circuit generates an active LUS output signal which creates a break in the low resistance path to terminate the latch up event.

2. The device of claim 1 wherein the first circuit includes a pnpn structure.

3. The device of claim 1 wherein the first circuit includes an inverter.

4. The device of claim 3 wherein the inverter includes a parasitic circuit having

a first pnp parasitic bipolar transistor Q1 having a first collector terminal, a first emitter terminal and a first base terminal, and

a second npn parasitic bipolar transistor Q2 having a second collector terminal, a second emitter terminal and a second base terminal.

5. The device of claim 4 wherein:

the LUS output is coupled to the first base terminal; and

the break in the low resistance path is created by switching off Q1.

6. The device of claim 1 wherein the first power rail is V_{DD} and the second power rail is V_{SS}.

7. The device of claim 4 wherein:

the LUS output is coupled to the first base terminal; and

the active LUS output signal switches off Q1 to break the low resistance path to terminate the latch up event.

8. The device of claim 7 wherein the LUS input is coupled to the second base terminal of Q2.

9. A method of forming a device comprising:

providing a substrate for the device;

forming a first circuit on the substrate, the first circuit is directly coupled to both first and second power rails of the device, the first circuit comprises complementary metal oxide semiconductor (CMOS) transistors, the first circuit is subject to a latch up event in the presence of a latch up condition, the latch up event includes a low resistance path created between the first and second power rails; and

forming a latch up sensing (LUS) circuit on the substrate, wherein the LUS circuit senses a latch up condition in the first circuit and terminates the latch up event when the latch up condition is sensed, the LUS circuit and the first circuit are distinct circuits, the LUS circuit is coupled to the first circuit, wherein the LUS circuit is configured to receive a LUS input signal at a LUS input from the first circuit and generates a LUS output signal at a LUS output to the first circuit, the LUS input signal and LUS output signal comprise voltage signals, wherein

forming the LUS circuit includes forming

a first p-type transistor comprising a first p-transistor terminal, a second p-transistor terminal, a p-transistor body, and a p-transistor gate terminal, wherein the first p-transistor terminal is coupled to the first power rail, the second p-transistor terminal is coupled to the LUS output of the LUS circuit, and the p-transistor body is coupled to the first p-transistor terminal, and

a second n-type transistor comprising a first n-transistor terminal, a second n-transistor terminal, a n-transistor body, and a n-transistor gate terminal, wherein the first n-transistor terminal is coupled to the second power rail, the second n-transistor terminal is coupled to the p-transistor gate terminal, the n-transistor gate terminal is coupled to the LUS input of the LUS circuit, and the n-transistor body is coupled to the first n-transistor terminal, and

when the input signal is an active latch up signal which indicates the presence of a latch up condition, the LUS circuit generates an active LUS output signal which creates a break in the low resistance path to terminate the latch up event.

10. The method of claim 9 wherein forming the first circuit includes forming a pnpn structure on the substrate which comprises:

a first pnp parasitic bipolar transistor Q1 having a first collector terminal, a first emitter terminal and a first base terminal;

a second npn parasitic bipolar transistor Q2 having a second collector terminal, a second emitter terminal and a second base terminal; and

wherein the low resistance path is from the first power rail and through the first emitter terminal, first base terminal, second collector terminal, second emitter terminal and to the second power rail.

11. The method of claim 10 wherein forming the first circuit comprises forming an inverter on the substrate.

12. The method of claim 10 wherein the active LUS output signal switches off Q1 to break the low resistance path to terminate the latch up event.

13. The method of claim 10 wherein:

the LUS input is coupled to the second base terminal of Q2;

the LUS output is coupled to the first base terminal of Q1; and

the active LUS output signal switches off Q1 to break the low resistance path to terminate the latch up event.

14. The method of claim 9 wherein the first power rail is V_{DD} and the second power rail is V_{SS}.

15. The method of claim 9 wherein:

the first circuit comprises an inverter which includes a parasitic circuit having

a first pnp parasitic bipolar transistor Q1 having a first collector terminal,

a first emitter terminal and a first base terminal, and

a second npn parasitic bipolar transistor Q2 having a second collector terminal, a second emitter terminal and a second base terminal;

the LUS input is coupled to the second base terminal of Q2;

the LUS output is coupled to the first base terminal of Q1; and

the active LUS output signal switches off Q1 to break the low resistance path to terminate the latch up event.