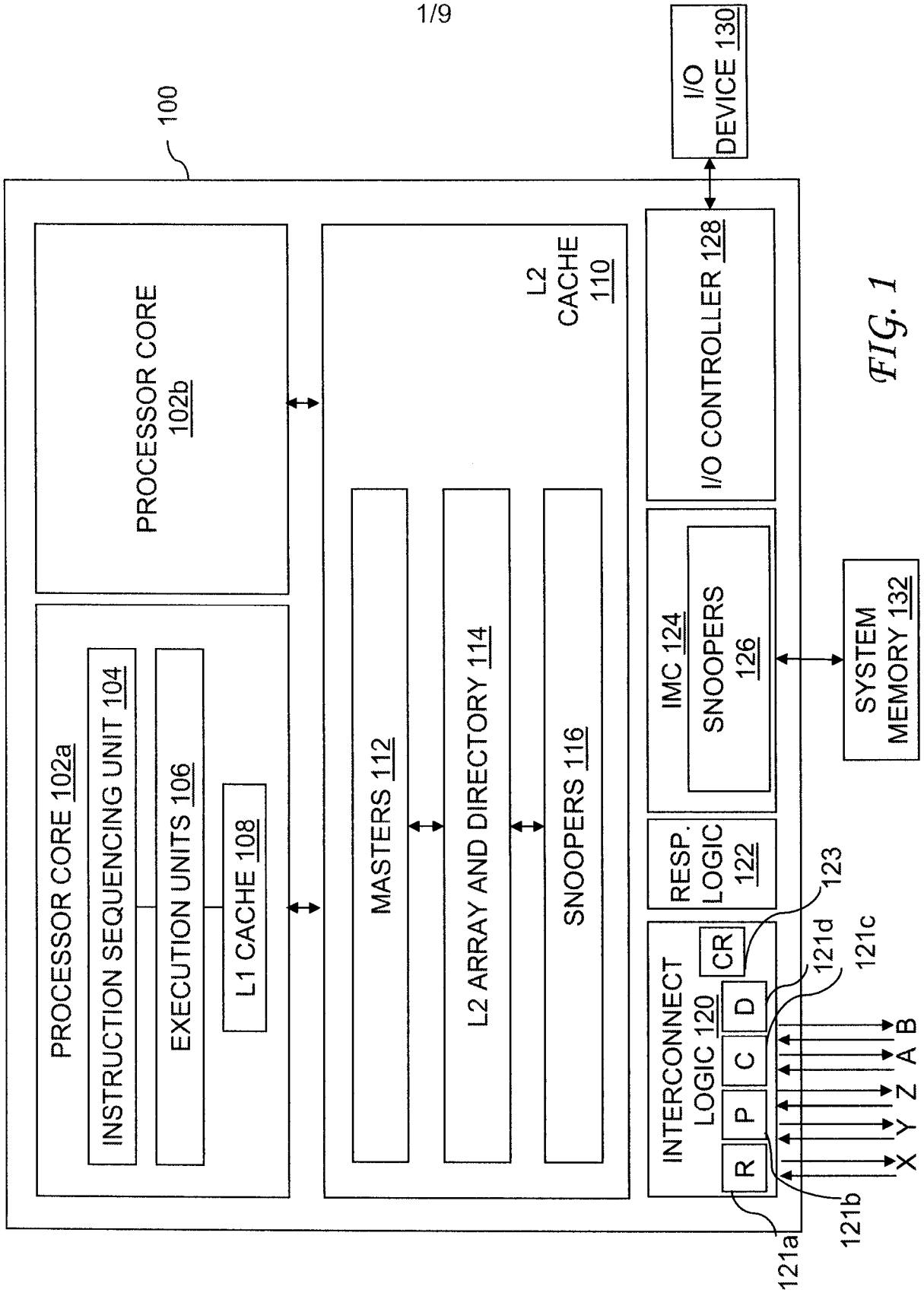
100
I/O DEVICE 130
PROCESSOR CORE 102b
PROCESSOR CORE 102a
INSTRUCTION SEQUENCING UNIT 104
EXECUTION UNITS 106
L1 CACHE 108
L2 CACHE 110
MASTERS 112
L2 ARRAY AND DIRECTORY 114
SNOOPERS 116
I/O CONTROLLER 128
IMC 124
SNOOPERS 126
SYSTEM MEMORY 132
RESP. LOGIC 122
INTERCONNECT LOGIC 120
R
P
C
D
CR
123
121a
121b
121c
121d
X Y Z A B

FIG. 1

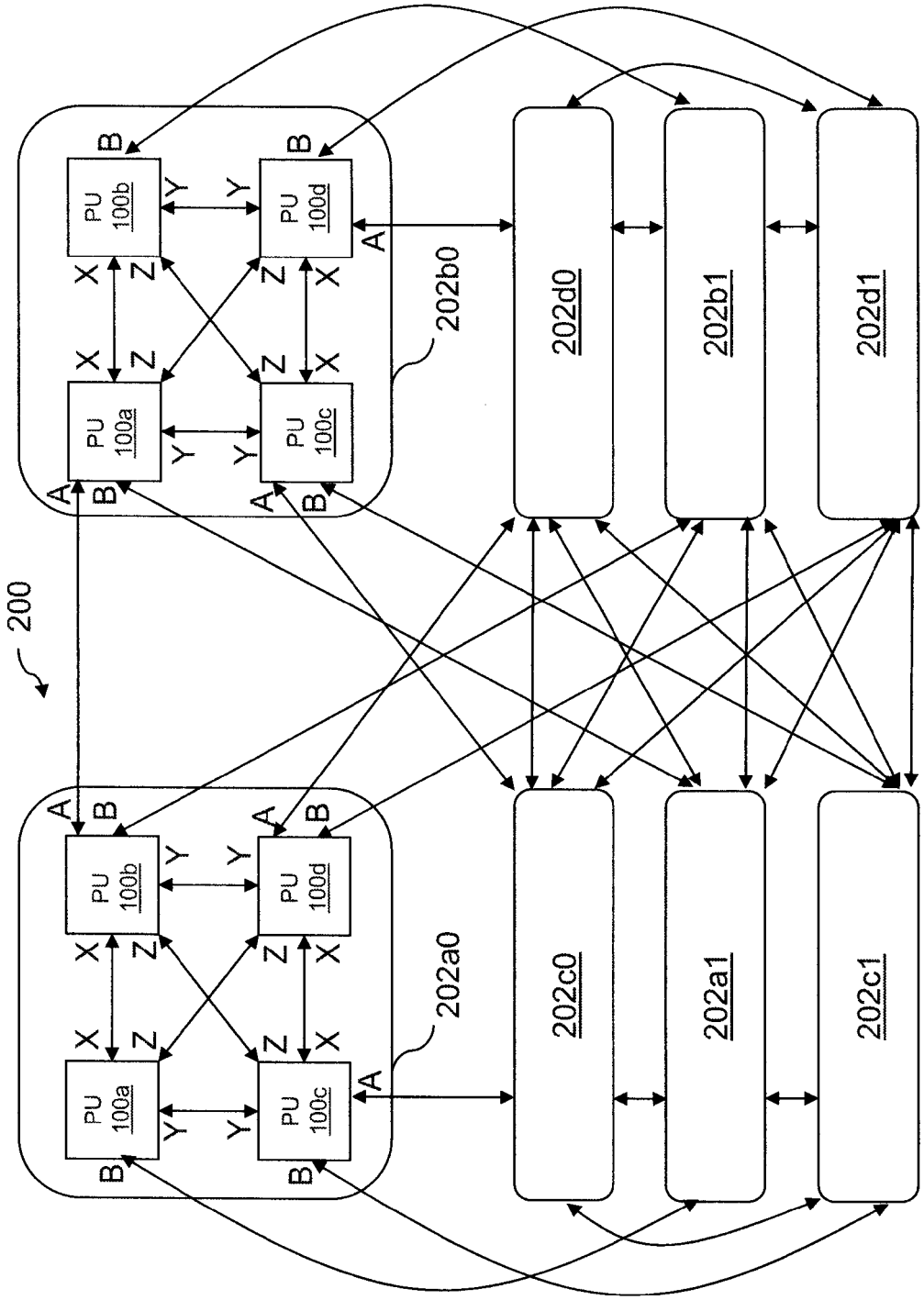
200
PU 100a
PU 100b
PU 100c
PU 100d
202a0
202b0
202c0
202d0
202a1
202b1
202c1
202d1

FIG. 2

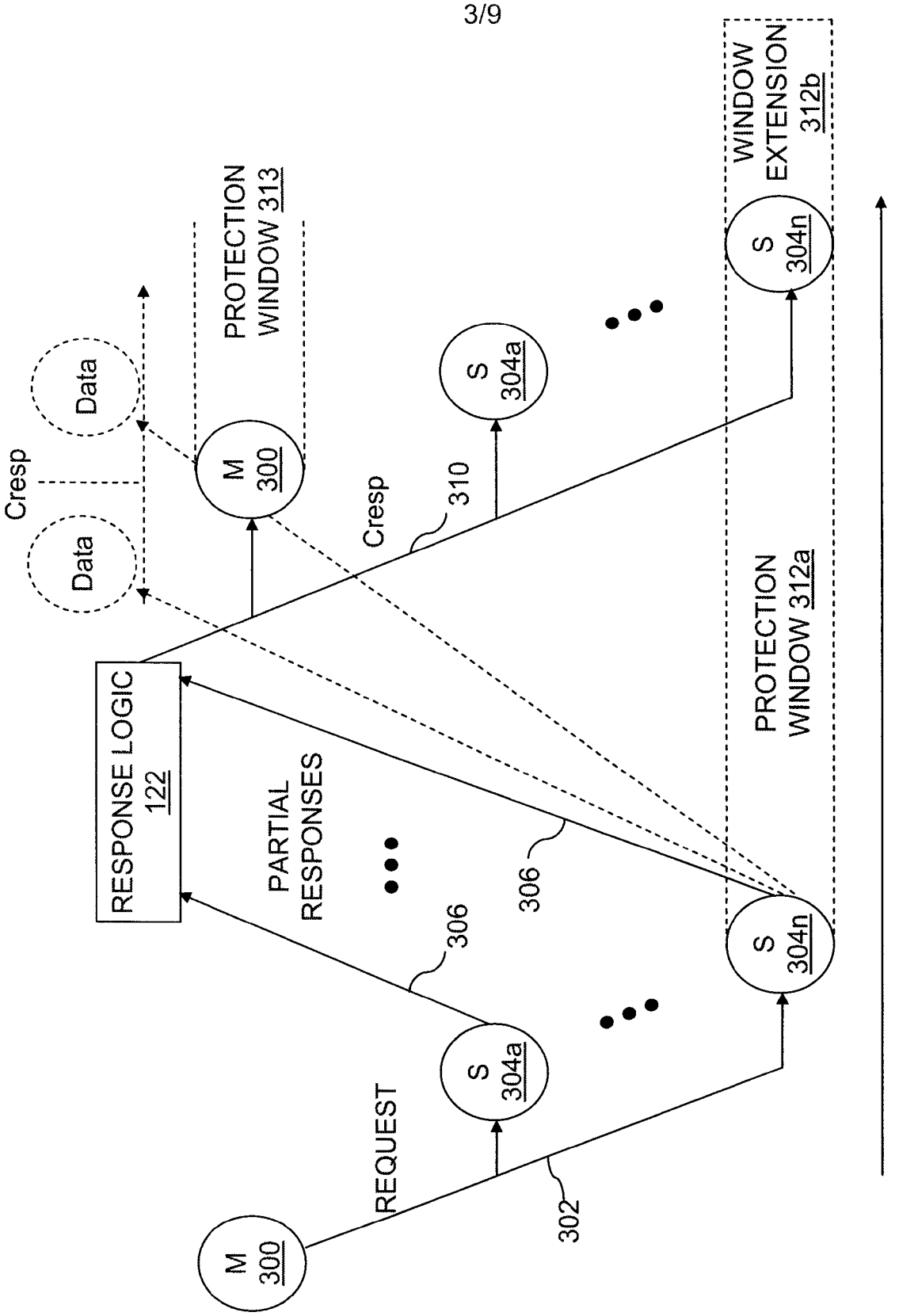
M 300
REQUEST
302
S 304a
S 304n
PARTIAL RESPONSES
306
306
RESPONSE LOGIC 122
Cresp
Data
Data
Cresp
M 300
PROTECTION WINDOW 313
S 304a
310
S 304n
WINDOW EXTENSION 312b
PROTECTION WINDOW 312a
TIME

FIG. 3

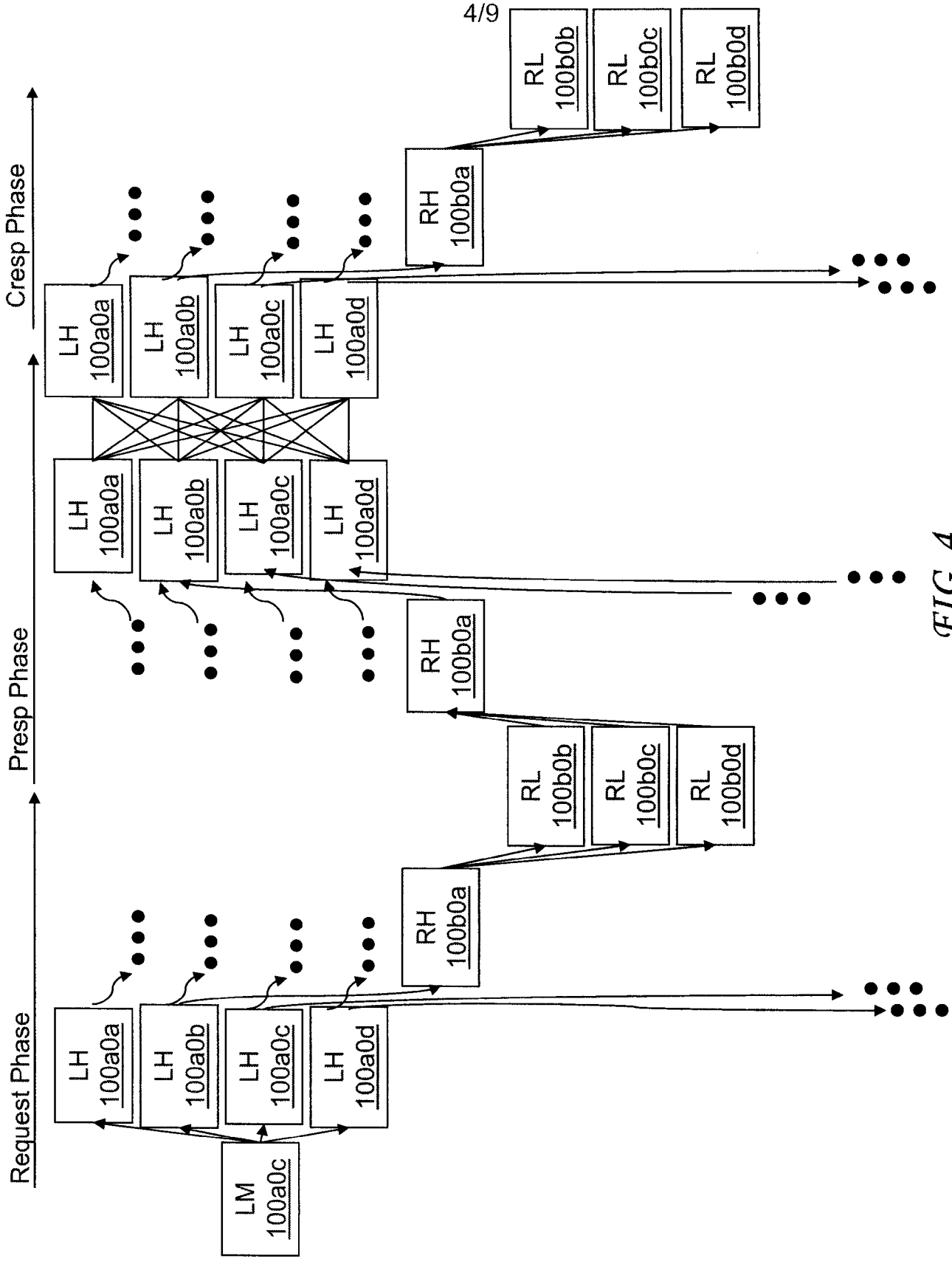
Request Phase
Presp Phase
Cresp Phase
LM 100a0c
LH 100a0a
LH 100a0b
LH 100a0c
LH 100a0d
RH 100b0a
RL 100b0b
RL 100b0c
RL 100b0d

FIG. 4

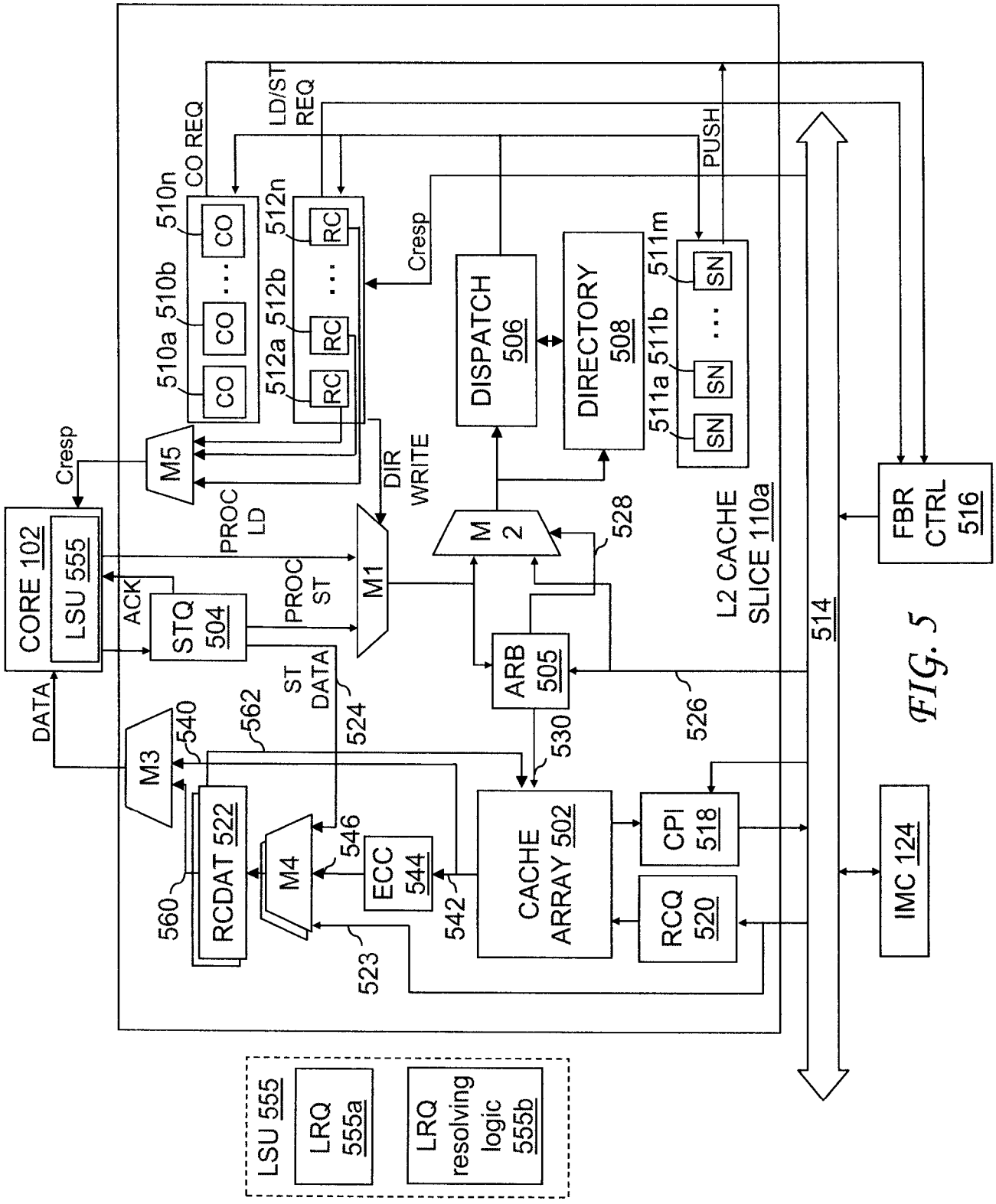
CORE 102
LSU 555
Cresp
DATA
ACK
STQ 504
PROC LD
PROC ST
M5
M1
M3
M4
M 2
ST DATA
DIR WRITE
CO REQ
LD/ST REQ
510a
510b
510n
CO
512a
512b
512n
RC
Cresp
DISPATCH 506
DIRECTORY 508
PUSH
511a
511b
511m
SN
528
ARB 505
526
530
L2 CACHE SLICE 110a
514
FBR CTRL 516
IMC 124
CACHE ARRAY 502
CPI 518
RCQ 520
ECC 544
542
546
RCDAT 522
560
540
562
524
523
LSU 555
LRQ 555a
LRQ resolving logic 555b

FIG. 5

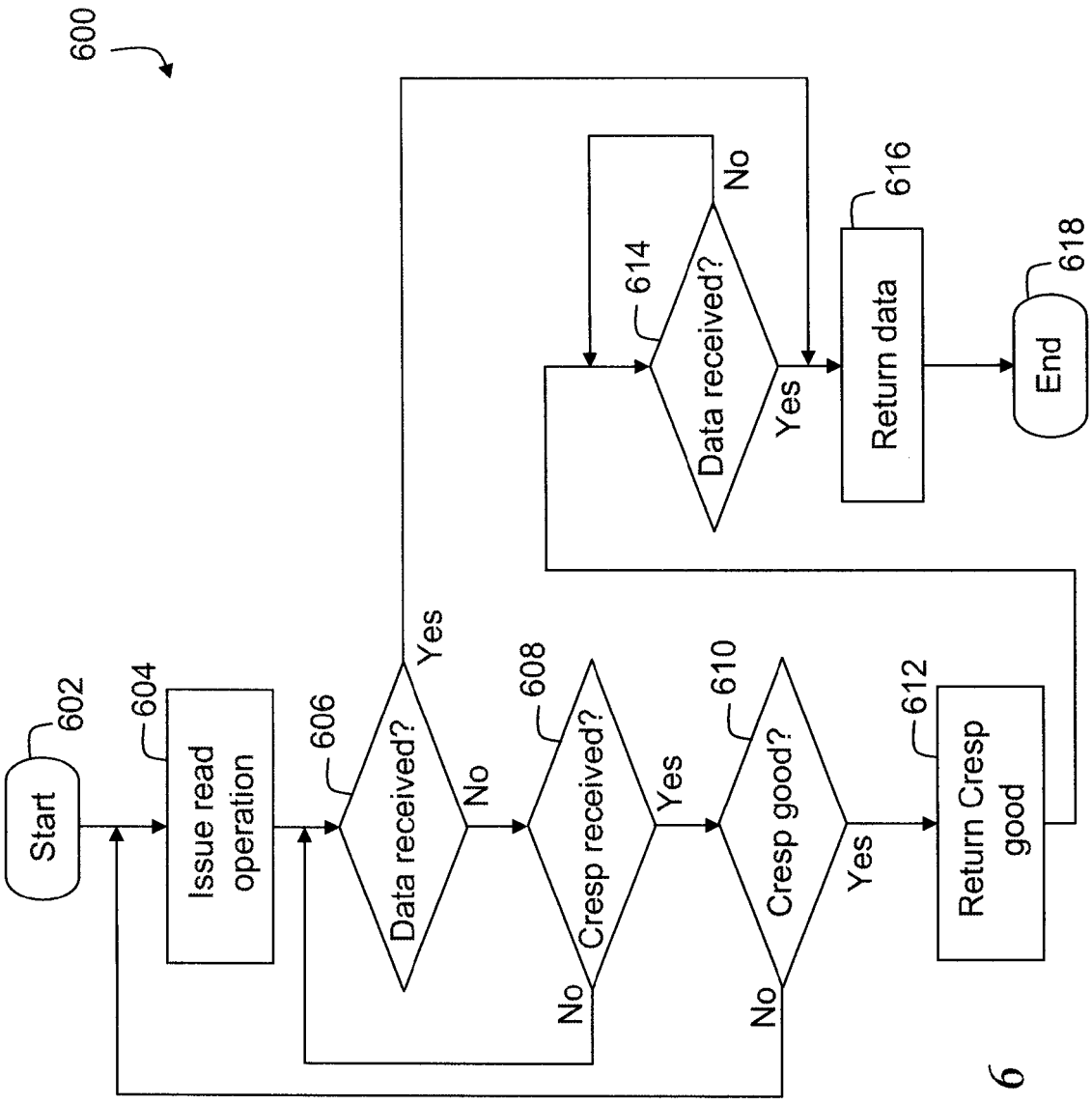
600
Start
602
Issue read operation
604
Data received?
606
Yes
No
Cresp received?
608
Yes
No
Cresp good?
610
Yes
No
Return Cresp good
612
Data received?
614
No
Yes
Return data
616
End
618

FIG. 6

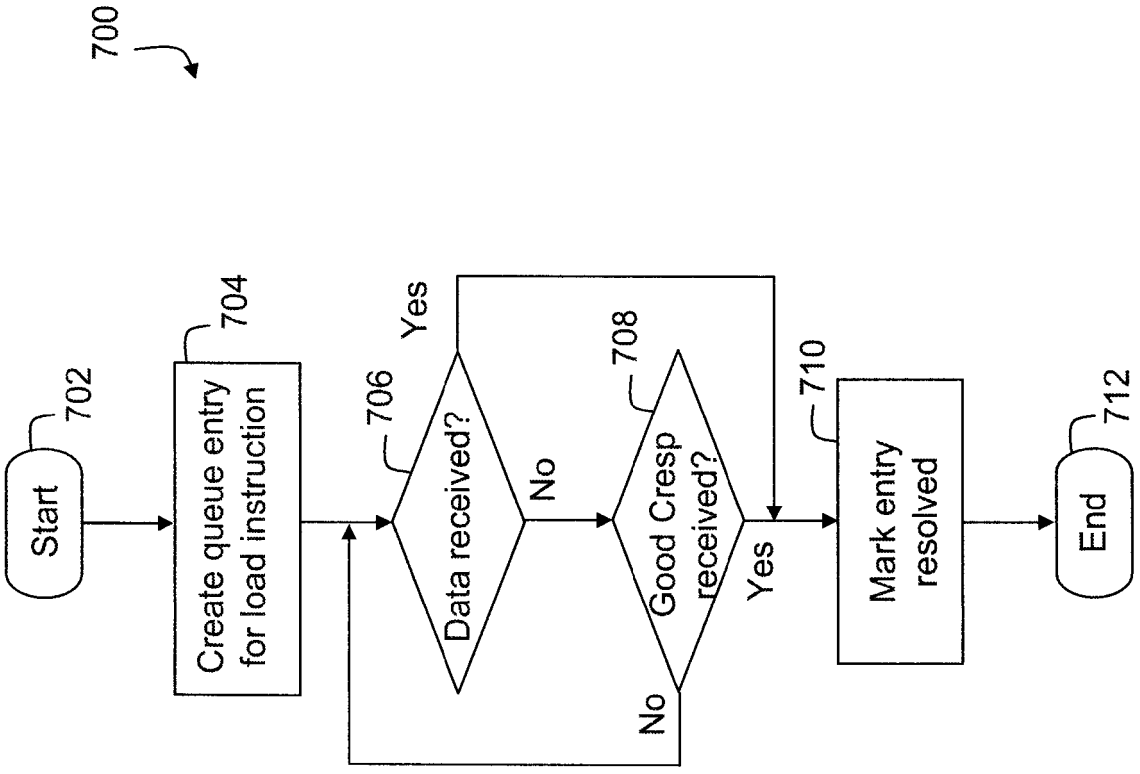
700
Start
702
Create queue entry for load instruction
704
Data received?
706
Yes
No
Good Cresp received?
708
Yes
No
Mark entry resolved
710
End
712

FIG. 7

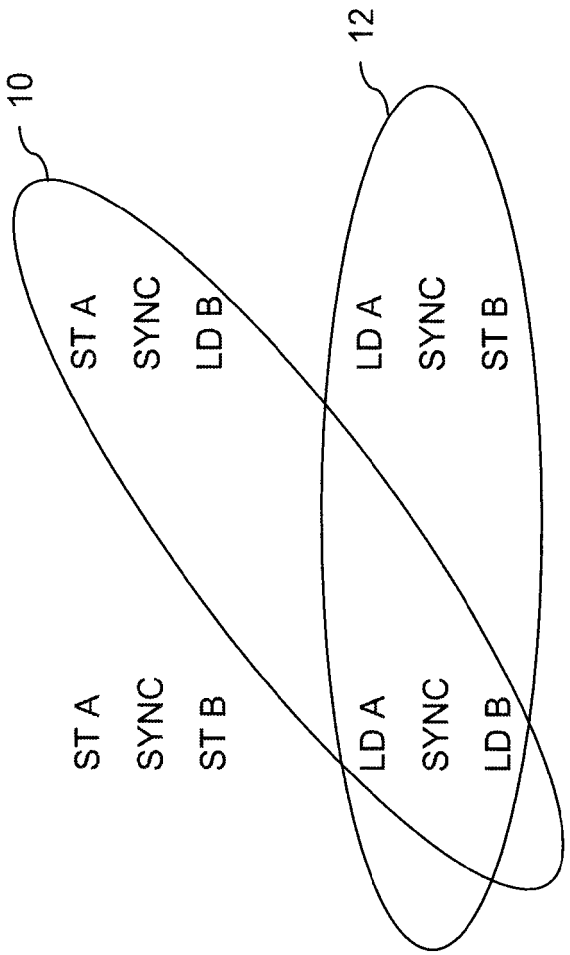

FIG. 8

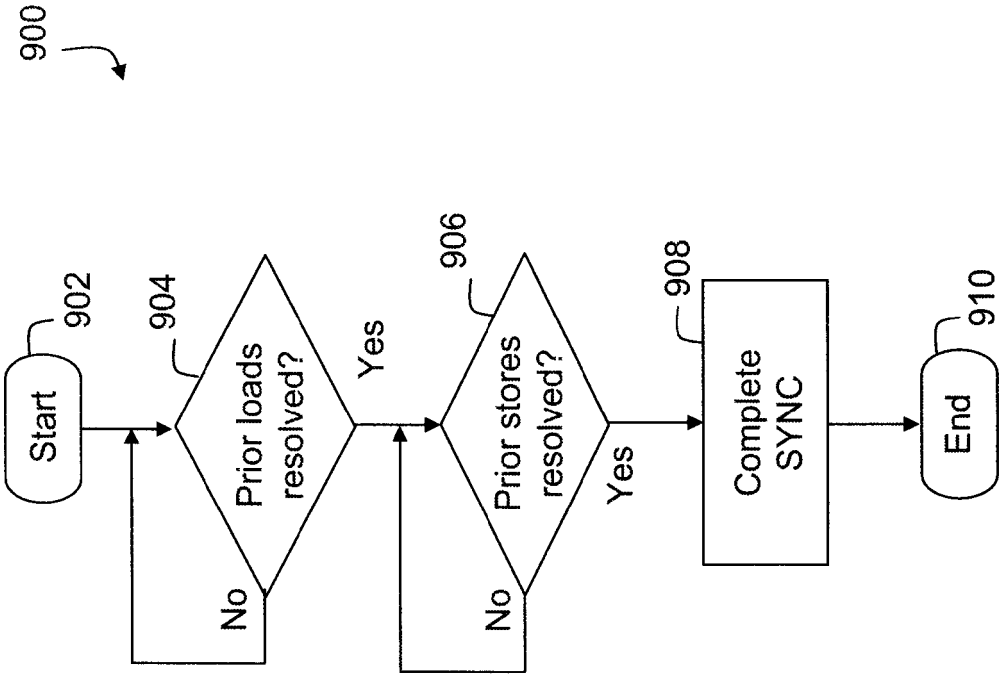
900
Start
902
Prior loads resolved?
904
No
Yes
Prior stores resolved?
906
No
Yes
Complete SYNC
908
End
910

FIG. 9