

The present invention concerns a read circuit for a memory such as an electrically programmable, non-volatile memory of the EPROM or EEPROM type, or any other memory comprising memory cells which are read by the detection of a variation in current or in voltage on the bit line.

In the case, for example, of memories of the EPROM or EEPROM type, each data storage or memory cell element is constituted by a floating gate MOS transistor which can be principally of the FAMOS type (floating gate avalanche injection MOS) or of the SAMOS type (stacked gate avalanche injection MOS). This type of transistor can have two states. Thus, in the case of an n-channel MOS transistor, in a first state no charge or a positive charge is trapped at the floating gate. A conduction channel can exist between source and drain. The transistor is then conducting and behaves as a closed switch. In a second state, electrons are trapped at the floating gate. They therefore prevent the creation of a conduction channel in the substrate between source and drain. In this case, the transistor is inhibited and behaves as an open switch.

In order to programme a floating gate MOS transistor, voltages higher than the normal operating voltage must be applied in suitable manner to the control gate and one of the electrodes, so that the floating gate can absorb and retain a charge of electrons. This charge of electrons at the floating gate raises the conduction threshold on the control gate of the transistor. On the other hand, in order to read a memory programmed in this way, a voltage which is lower than the threshold voltage of the programmed floating gate MOS transistors but higher than the minimum voltage of the non-programmed transistors, must be applied to the control gate. This read voltage enables detection of the conducting or inhibited state of the transistor. In general, the floating gate MOS transistor is connected by one of its electrodes to a bit line biased in voltage by a generator. Its other electrode is connected to earth or to a low voltage. The bit line is also connected to a current or voltage sensor. This sensor measures the current delivered in the line by the generator. Thus, if the memory cell has not been programmed, the floating gate MOS transistor is conducting and, when a read voltage is applied which is above the threshold voltage of the non-programmed transistors, the transistor is brought into conduction. A variation in the current or a drop in the voltage is then detected on the sensor. In the second case, when the memory cell has been programmed, charges are trapped at the floating gate of the transistor. The read voltage applied to the control gate is, in this case, in the opposite direction to the

potential barrier created in the conduction channel by the charges stored in the floating gate. However, this is insufficient to alter the conduction of the channel, and the transistor remains inhibited. Consequently, the sensor at the end of the bit line detects no variation in current or in voltage.

Thus, with a memory of the EPROM type as described above, it is possible to read the contents of a memory cell according to the consumption of the circuit, in particular when the memory is read bit by bit.

This is particularly inconvenient in the case of memories used for receiving confidential data, since it is then easy to detect during reading the content of these data.

An object of the present invention is to overcome this drawback by proposing a read circuit which always has a consumption of current, whatever the programmed or non-programmed state of the memory cell read.

Consequently, subject matter of the invention is a read circuit for an integrated circuit of the logic circuit type comprising a memory constituted by a matrix of memory cells which is read by the detection of a variation in current or in voltage, the memory cells each being able to be addressed by lines and columns selected by line decoders and column decoders, the read circuit being suitable for connection to the memory cells by a so-called bit line and comprising a precharge circuit for the bit line and a first detection circuit detecting the conduction or the non-conduction of the addressed memory cell, characterised in that it comprises, in parallel with the first detection circuit, a second identical detection circuit, the two detection circuits being connected to a common node point of the bit line by means arranged so that the two detection circuits react in complementary manners for a given state of the bit line in such a manner that, whatever the state of the bit line, the overall current used remains constant.

Different embodiments can be used for this read circuit.

According to a first embodiment, the read circuit comprises a first precharge circuit for the bit line, a first means constituting a switch connected between the first precharge circuit and the first detection circuit, a second means constituting a switch connected by means of an inverter between the first precharge circuit and the second detection circuit, the means constituting the switch being controlled by a read enable signal, the second and the third precharge circuits producing a precharge at the same logic level as the first precharge circuit being respectively connected between each means constituting a switch and the corresponding detection circuit.

According to another embodiment, the read circuit

comprises a first precharge circuit for the bit line, a first means constituting a switch connected between the first precharge circuit and the first detection circuit, a second means constituting a switch connected
5 between the first precharge circuit and the second detection circuit, the means constituting a switch being controlled respectively by a read enable signal and by this signal when inverted, a second precharge circuit producing a precharge at the same logic level
10 as the first precharge circuit being connected between the first means constituting a switch and the first detection circuit, and a third precharge circuit producing a precharge at the inverse logic level being connected between the second means constituting a
15 switch and the second detection circuit.

Other features and advantages of the present invention will emerge from reading the description of various following embodiments, which is given with reference to the attached drawings, in which:

- 20 - Figure 1 shows diagrammatically an EPROM memory comprising a read circuit,
- Figures 2A and 2B show diagrammatically a first embodiment of a read circuit in accordance with the present invention, as well as a timing diagram of the
25 principal control signals for this circuit,
- Figures 3A and 3B show diagrammatically another embodiment of a read circuit in accordance with the present invention, as well as a timing diagram of the main control signals for this circuit, and
30 - Figures 4A and 4B show, respectively, an embodiment of the detection circuits and the voltage-current curve of this circuit.

In order to simplify the description, in the drawings the same elements bear the same reference
35 numbers. On the other hand, the description is given with reference to MOS circuits produced with C MOS technology; it is obvious to the expert that the present invention can be adapted to other technologies, in particular N MOS technology.

40 In Figure 1, an electrically programmable non-volatile memory 1 of the EPROM type is shown. This memory is of the memory cell type constituted by an MOS transistor 2 with a floating gate 5. In particular, the transistor 2 comprises two main electrodes 3 and 4
45 respectively, a floating gate 5 and a control gate 6. A first main electrode, that is, the source in the embodiment shown, is connected to earth, while the other electrode 4, that is, the drain, is connected to a line 7 known as a bit line. The control gate 6 is
50 connected to another connection 8 known as a word line. The bit lines and word lines are arranged in lines and columns so as to determine a matrix including the memory cells as shown in Figure 1. This memory comprises means formed essentially by a line decoder 9

and a column decoder 10, for applying to the lines and columns potentials representing data to be recorded in the memory cells or representing read control of the data recorded in the memory cells. Thus, for reading a memory cell, the corresponding word line 8 is adjusted up to a voltage produced by an output of the line decoder 9. By means of the column decoder 10, a command pulse is sent along the corresponding bit line 7. The MOS transistor 2 becomes conducting or remains inhibited according to whether the charges have or have not been trapped beforehand at the floating gate 5. A read circuit 11 further connected to one end of the bit line 7 by way of the column decoder 10 forming a multiplexer, detects the variation or absence of variation in current. It deduces from this that the memory cell is programmed to "1" or "0" respectively.

There will now be described, with reference to Figure 2A, a first embodiment of a read circuit in accordance with the present invention. This read circuit 11 first comprises a precharge circuit for the bit line 7. This precharge circuit is formed by an N-type MOS transistor 12 in the embodiment shown, one of the electrodes 13 of which transistor is connected to the supply voltage V_{cc} , the other main electrode 14 being connected to a node point N on the bit line 7. On the other hand, the gate 15 of the MOS transistor 12 is connected to the clock CLK of the EPROM memory. Moreover, the read circuit in accordance with the present invention is formed by two parallel branches. The first branch comprises a first means forming a switch constituted by an N-type MOS transistor 16, one of the main electrodes 17 of which is connected to the node point N of the bit line 7 and the other main electrode 18 of which is connected to the input of a first detection circuit 21, the output of which gives the datum which is read. The gate 19 of the MOS transistor 16 is connected to a read enable signal L which can be, for example, the read control signal WL applied to the gate of the delayed memory cell.

On the other hand, the second branch of the read circuit is formed essentially by a second means constituting a switch formed by an MOS transistor 16' identical to the MOS transistor 16, one of the main electrodes 17' of which is connected by way of an inverter 20 to the node point N of the bit line 7 and the other electrode 18' of which is connected at the input of a second detection circuit 21' identical to the circuit 21. The detection circuits 21 and 21' can be formed by two inverters in series. The gate 19' of the MOS transistor 16' is connected to the read enable signal L. This second branch simulates an inverse detection signal of the detection obtained on the first branch so as to obtain simultaneously at each reading the detection of a "1" and a "0", whatever the state of

the memory cell addressed, as will be explained in detail below. On the other hand, at the node point A between the MOS transistor 16 and the detection circuit 21 there is connected a second precharge circuit formed by an N-type MOS transistor 40, one of the electrodes of which is connected to the node point A, the other electrode being connected to the voltage V_{cc} and the gate to the clock signal CLK. This precharge circuit produces a precharge at the same logic level as the first precharge circuit formed by the MOS transistor 12. Moreover, at the node point B between the MOS transistor 16' and the detection circuit 21' there is connected a third precharge circuit formed by an N-type MOS transistor 40', one of the electrodes of which is connected to the node point A, the other electrode being connected to the voltage V_{cc} and the gate to the clock signal CLK. According to another embodiment, the precharge circuits 12, 40, 40' can be produced by P-type MOS transistors, and in this case the gates are connected to a signal CLK.

According to an embodiment which is specific to a memory in hard wired logic, the data obtained at the output of the detection circuits 21 and 21' are sent to comparators formed by exclusive ORs 22, 22' which receive at the input a Din datum for comparison with the datum read, in particular within the framework of the comparison of a confidential code. The result obtained at the output of the exclusive OR 22 gives the result desired. The exclusive logic OR gates can also be replaced by other gates inhibited by a clock which is activated at the end of reading.

The operation of the circuit described above will now be explained with the aid of the timing diagram in Figure 2B.

With the above circuit, when the signal CLK is at the logic level "1", that is to say, during the time 1 in the diagram, the MOS transistors 12, 40 and 40' are conducting, and a precharge of the node points N, A and B is produced at $V_{cc}-V_T$, that is to say, at a logic level "1". When the signal CLK changes back to the logic level "0", the control gate 6 of the floating gate MOS transistor 2 is activated by applying the signal WL to it and, according to the state of the memory cell, the bit line 7 is discharged or not discharged, as shown by the signal BL. Thus, if the memory cell formed by the floating gate MOS transistor 2 has not been programmed (no electrons at the floating gate), the transistor is conducting and, during application of the read voltage W_r corresponding to the supply voltage, the transistor is brought into conduction. In this case, there is discharging of the bit line 7 and the electrode 17 is found to be at a logic level "0", while the electrode 17' is found to be at a logic level "1" due to the inverter 20. When the

signal L changes to the logic level "1" as shown by 3
in the diagram of Figure 3A, the node point A is
positioned at the logic level "0", causing the tripping
of the detection circuit 21, while the node point B
5 remains positioned at the level "1". If, on the other
hand, the floating gate transistor has been programmed,
there is no discharging of the bit line 7. The node
point N remains at the logic level "1", while the
electrode 17' at the output of the inverter 20 is found
10 to be at a logic level "0". When the signal L changes
to "1", the node point A remains unchanged at "1",
while the node point B changes to "0". In this case,
only the detection circuit 21' trips. Since the two
circuits are identical, the consumption is therefore
15 identical in the case of a "0" or a "1" being read.

There will now be described, with reference to
Figure 3A, another embodiment of a read circuit in
accordance with the present invention. This read
circuit comprises a first precharge circuit formed by a
20 P-type MOS transistor 41, one electrode 42 of which is
connected to the node point N' of the bit line 7, the
second electrode being connected to voltage V_{cc} and the
gate to the inverted clock signal CLK. On the other
hand, the read circuit comprises a first branch with a
25 first means forming a switch constituted by an N-type
MOS transistor 23, one of the main electrodes 24 of
which is connected at the node point N' to the bit line
7, and the other main electrode 25 of which is
connected to a first detection circuit 35. The gate 26
30 of the MOS transistor 23 is connected to a read enable
signal L. A precharge circuit is connected to the node
point A' at the output of the MOS transistor 23. More
specifically, this precharge circuit is formed, in the
embodiment shown, by a P-type MOS transistor 27, one of
35 the main electrodes 28 of which is connected to the
supply voltage V_{cc} and the other electrode 29 of which
is connected to the node point A' between the electrode
25 of the MOS transistor 23 and the circuit 35. The
gate 30 of the MOS transistor 27 is connected to the
40 inverted clock signal CLK. On the other hand, the read
circuit 11 comprises a second branch with a second
means forming a switch constituted by a P-type MOS
transistor 23', one of the main electrodes 24' of which
is connected at the node point N' to the bit line 7 and
45 the other main electrode 25' of which is connected to a
second detection circuit 35'. The gate 26' of the MOS
transistor 23' is connected by way of an inverter 50 to
the read enable signal L. On the other hand, a
precharge circuit is connected to the node point B'
50 between the electrode 25' and the circuit 35'. This
precharge circuit is formed by an N-type MOS transistor
31, one of the main electrodes 32 of which is connected
to earth V_{ss} , while its other main electrode 33 is
connected to the node point B'. The gate 34 of the MOS

transistor 31 is connected to the clock signal CLK.

The operation of this read circuit will be explained in the following with reference to the timing diagram in Figure 3B.

5 During the time a, the clock signals CLK and $\overline{\text{CLK}}$ are at logic levels "1" and "0" respectively. Because of this, the node points N' and A' are precharged at the supply voltage V_{cc} , while the node point B' is precharged at earth V_{ss} .

10 During the time b, the read command WL applied to the gate of the floating gate MOS transistor forming the memory cell changes to "1". During this period, the contents of the memory cell are read. The node point N' either remains at V_{cc} or discharges at V_{ss} according to the contents of the memory cell, as shown by the signal BL.

15 During the time c, the read enable signal L is positioned at "1". If the node point N' has not been discharged, the node point A' remains positioned at the voltage V_{cc} , while the node point B' trips to the voltage V_{cc} . Contrastingly, if the node point N' has been discharged, the node point A' trips to earth V_{ss} , while the node point B' remains positioned at earth V_{ss} .

20 The detection circuits 35, 35' are, in this embodiment, made up of inverters with C MOS technology, of the type shown in Figure 4A.

25 This inverter is formed, in a known manner, by a P-type MOS transistor 51, one of the electrodes of which is connected to V_{cc} and the other electrode of which is connected to one of the electrodes of an N-type MOS transistor 52; the other electrode of which is connected to earth V_{ss} . The two gates are connected together and connected to the input voltage V_{IN} , and the output S is obtained at the node point between the two transistors.

30 The consumption curve of a C MOS inverter is shown in Figure 4B. From this curve it can be seen that the consumption is the same when V_{IN} changes from V_{cc} to V_{ss} or when V_{IN} changes from V_{ss} to V_{cc} . This property is used in the circuit in Figure 3A in order to obtain the result desired, that is to say, an identical current consumption whatever the state of the memory circuit.

35 The embodiments described above are given by way of example. It is obvious to the expert that they can be modified, in particular in the type of MOS transistors used for the precharge circuits or the circuits forming switches.

40 On the other hand, the present invention is described with reference to an EPROM memory, and it is obvious that it can be applied to an EEPROM memory or to any memory the memory cells of which are read by detecting a variation in current or voltage on the bit line.



Claims

1. Read circuit for an integrated circuit of the logic circuit type comprising a memory (1) constituted by a matrix of memory cells which is read by the detection of a variation in current or in voltage, the memory cells each being able to be addressed by lines and columns selected by line decoders (9) and column decoders (10), the read circuit (11) being suitable for connection to the memory cells by a so-called bit line (7) and comprising a precharge circuit (12, 41) for the bit line and a first detection circuit (21, 35) detecting the conduction or the non-conduction of the addressed memory cell, characterized in that it comprises, in parallel with the first detection circuit, a second identical detection circuit (21', 35'), the two detection circuits being connected to a common node point (N, N') of the bit line by means (20, 16, 16', 40, 40', 23, 23', 27, 31, 50) arranged so that the two detection circuits react in complementary manners for a given state of the bit line in such a manner that, whatever the state of the bit line, the overall current used remains constant.
2. Read circuit according to claim 1, characterized in that it comprises a first precharge circuit (12) for the bit line (7), a first means constituting a switch (16) connected between the first precharge circuit and the first detection circuit (21), a second means constituting a switch (16') connected by means of an inverter (20) between the first precharge circuit and the second detection circuit (21'), the means constituting the switch being controlled by a read enable signal (L), second and third precharge circuits (40, 40') producing a precharge at the same logic level as the first precharge circuit being respectively connected between each means constituting a switch and the corresponding detection circuit.
3. Read circuit according to claim 1, characterized in that it comprises a first precharge circuit (41) for the bit line, a first means constituting a switch (23) connected between the first precharge circuit and the first detection circuit (35), a second means constituting a switch (23') connected between the first precharge circuit and the second detection circuit (35'), the means constituting a switch being controlled respectively by a read enable signal (L) and by this signal when inverted, a second precharge circuit (27) producing a precharge at the same logic level as the first precharge circuit being connected between the first means constituting a switch (23) and the first detection circuit (35), and a third precharge circuit producing a precharge at the inverse



logic level being connected between the second means constituting a switch (23') and the second detection circuit (35').

- 5 4. Read circuit according to either of claims 2 and 3, characterised in that the means forming switches (16, 16', 23, 23') are constituted by MOS transistors.
- 10 5. Read circuit according to either of claims 2 and 3, characterised in that the detection circuits are constituted by two MOS inverters.
- 15 6. Read circuit according to claim 2, characterised in that the precharge circuits (12, 40, 40') are identical and are each constituted by an N-type MOS transistor, one of whose main electrodes is connected to the supply voltage V_{cc} , the other main electrode being connected to the node point to be charged and the gate being connected to the clock signal CLK.
- 20 7. Read circuit according to claim 2, characterised in that the precharge circuits (12, 40, 40') are identical and are each constituted by a P-type MOS transistor, one of whose main electrodes is connected to the supply voltage V_{cc} , the other main electrode being connected to the node point to be charged and the gate being connected to the inverted clock signal CLK.
- 25 8. Read circuit according to claim 3, characterised in that the first and the second precharge circuits are each constituted by a P-type MOS transistor (27, 41), one of whose main electrodes (28, 43) is connected to the supply voltage V_{cc} , the other main electrode (29, 42) being connected to the node point to be charged and the gate (30, 44) being connected to the inverted clock signal CLK, and the third precharge circuit being constituted by an N-type MOS transistor (31), one of whose main electrodes (32) is connected to earth V_{ss} , the other main electrode (33) being connected to the node point to be charged and the gate (34) being connected to the clock signal CLK.
- 30 9. Read circuit according to any one of claims 2 to 8, characterised in that the read enable signal (L) is constituted by the read command (WL) applied to the delayed memory cell.
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