

Description

The present invention relates to a semiconductor device and, in particular, to a protection diode for protection against a possible negative surge voltage which is applied to a bonding pad.

In a semiconductor device, such as an IC and LSI, a plurality of bonding pads 13 formed of, for example, aluminum are formed on the marginal area of a semiconductor chip 11 as shown in Fig. 1. The pads are connected to a semiconductor device area 12 by a wiring, such as an aluminum, and connected to lead terminals (not shown) by bonding wires (not shown) so that the semiconductor device area 12 is electrically connected to the lead terminals. A negative surge voltage protection diode 14 is formed between the pads 13 as shown in Figs. 2A and 2B to allow a negative surge voltage which is induced from the lead terminal to be grounded. It is required that the diode has the surge withstand voltage of about -250V. The aforementioned diode is manufactured as will be set forth below. A buried layer 15 of first conductive type (N type) having a high impurity concentration is formed, by thermal diffusion, in a protection diode formation area of the P type substrate 22. A first area 21 of N conductivity type lower in impurity concentration than the buried layer 15 is epitaxially grown on the substrate surface. An isolation layer 24 is thermally diffused around a pad formation area in the first area 21 and around a negative surge voltage protection diode 14 in the first area to achieve an element-to-element isolation in which case the isolation layer extends down to the substrate surface. When this is done, an island area and protection diode island area are formed beneath the pad. Then an N type diffusion region 16 and P type diffusion region 17 near to the diffusion region 16 are formed on the island area of a protection diode, serving as a cathode and anode, respectively. In this way, an insulating oxide film 25 is formed on the surface of the N type first area 21, isolation layer 24, N type diffusion region 16 and P type diffusion region 17. Of the oxide film 25, those portions overlying the N type diffusion layer 16 and P type diffusion layer 17 are etched to form a hole in the diffusion regions 16 and 17. Aluminum is evaporated over the pad formation area and over the respective diffusion layers to provide a pad 13 extending up to the N type diffusion region 16 as well as an electrode 18 connected to the P type diffusion layer 17.

In the semiconductor device thus manufactured, the protection diode 14 comprises the diffusion region 16 electrically connected to the pad 13 and diffusion region 17 connected to the electrode 18. Upon the generation of a negative surge current from the lead terminal to the pad 13, it flows into the N type diffusion region 16. Since the N type diffusion region and P type diffusion region provide a PN junction, the

electric current flows into the P type diffusion region 17 and a potential is taken out of the pad via the electrode 18. Upon applying a surge voltage between, for example, the voltage 18 and a ground terminal no surge current flows across the semiconductor area 12, thus preventing a breakage of the semiconductor device.

In the aforementioned conventional semiconductor device, the diode area including the N type region 16 and P type region 17 has to be secured independently of the pad area because a withstand voltage of about -250V is necessary. That is, an island area which is secured for the protection diode requires a third to a half of the island area underlying the pad 13, thus offering a bar to a reduction in a pad-to-pad distance and hence to an improvement in an integration density.

An object of the present invention is to provide a semiconductor device which can improve an integration density by forming a protection diode without providing any extra protection diode island area.

Another object of the present invention is to provide a semiconductor device which can be simplified in its structure by utilizing an element isolation layer as an area of second conductivity type for a protection diode.

JP-A-60-246 668 describes a semiconductor integrated circuit having an input protective circuit including a conductive pad and diodes. A first p-type region is formed in a semiconductor substrate; the interconnection pad is formed on a patterned insulating layer on the substrate; and a second p-type region is formed underneath the pad and in electrical contact thereto.

According to the present invention there is provided a semiconductor device constituting a protection diode for protecting a semiconductor device area against a negative surge voltage applied to an interconnection pad, comprising: a first semiconductor layer of first conductivity type formed on a semiconductor substrate of second conductivity type; an interconnection pad formed on a patterned insulating layer formed on said first layer and electrically connected to said semiconductor device area; said diode comprising a second region of said first conductivity type formed in said first semiconductor layer substantially beneath a first opening in said patterned insulating layer beneath a region of said interconnection pad not utilized for wire bonding and electrically connected to the pad, said second region having an impurity concentration higher than that of said first layer; an area of second conductivity type formed in a region of said first layer around said pad and extending down to said substrate surface; and an electrode formed over said second conductivity type area, and electrically connected to the second conductivity type area via a second opening in said patterned insulating layer.

In the disclosure of the present specification and claims as set out below, the term "effective bonding portion" represents a bonding area of a pad and "non-effective bonding portion" a non-bonding area of the pad.

Upon the application of a negative surge voltage to the resultant diode an electric current flows from the second region of first conductivity type into an area of second conductivity type and from there toward an outside of the pad. This structure obviates the necessity of forming any area of a diode in other than the pad. As a result it is possible to improve an integrated density.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a plan view diagrammatically showing a semiconductor chip;

Figs. 2A and 2B are a plan view and cross-sectional view, respectively showing a conventional semiconductor device;

Figs. 3A and 3B are a plan view and cross-sectional view, respectively, showing a semiconductor device according to one embodiment of the present invention; and

Figs. 4A and 4B are a plan view and cross-sectional view, respectively, showing a semiconductor device whose second region is formed under an effective bonding area.

A semiconductor device according to the present invention will be explained below in more detail.

Figs. 3A and 3B show a semiconductor device according to one embodiment of the present invention. In these Figures, a P type substrate 22, first area 21 of first conductivity (N type) having a low impurity concentration, and P type isolation area 24 are of the same type as those of the conventional semiconductor device. For this reason, the same reference numerals are employed to designate parts or elements corresponding to those shown in Figs. 3A and 3B. Further explanation of the aforementioned embodiment will, therefore, be omitted. A rectangular pad 26 has a circular effective bonding area 28 as indicated by a broken line in Fig. 3A and noneffective bonding areas 28' formed one at each corner of the rectangular pad. Second region 23 of N conductivity type are formed, by diffusion, beneath the noneffective bonding area, that is, one at each corner of the pad and may be formed at any proper position so long as they serve as the noneffective bonding area 28'. As in this embodiment, it is better to form the second region 23 at each corner of the rectangular pad so as to obtain a desired surge withstand voltage. The surge withstand voltage is not affected even if the effective bonding area 28 is somewhat partly covered by the second area 23. An insulating film 25 of about 500nm (5000 Å) thick is formed on the major surface of the first area 21. A hole is formed, by photoetching, in that

portion of the insulating film 25 over the isolation area 24 and in a contact portion of the insulating layer 25 which is located between the N type second region 23 and the interconnection pad 26. A mask is formed on those portions other than both the insulating layer area corresponding to an electrode 27 to be formed over the isolation area 24 and insulating layer area corresponding to the pad 26. Aluminum is evaporated on the resultant structure to form the aforementioned electrode 27 and pad 26. The semiconductor device is thus manufactured as a protection diode 24 including the second region 23 electrically connected to the pad 26 and isolation layer 24 electrically connected to the electrode 27.

In this way, a PN junction is formed with the N type second region 23 as the cathode and P type isolation layer 24 as the anode. Upon the application of a negative surge voltage of about -250V to the pad 26, a current flows across the PN junction and, via the isolation layer 24, electrode 27 and wire, into an outside portion of the semiconductor device, such as a ground pad, not shown.

According to the embodiment, it is not necessary to form a negative surge voltage protection diode independently of the island portion of the pad 26. If the chip size is fixed relative to the conventional chip size, an area which is employed as an island area for the conventional negative surge voltage protection diode can effectively be utilized to form another semiconductor element, etc., thus ensuring an increase in design latitude and in integration density. It is also possible to reduce a pad-to-pad distance and hence a chip size.

The inventor has researched the possibility of increasing a surge withstand voltage by, as shown in Figs. 4A and 4B, forming a second region 23' beneath an effective bonding area 28 of a first area 21 in which case the second region is formed as having a large area. It has been found that, when a bonding wire is bonded by a bonder to a pad 26, the second region 23' which is formed beneath the pad 26 is destroyed due to a bonding impact so that a desired surge characteristic cannot be obtained. This means that, contrary to the inventor's initial intention, not only the surge withstand voltage is not increased but also a desired surge withstand voltage cannot be obtained.

Although, in the aforementioned embodiment, the pad has been explained as being a single-layer structure, it may be formed as a multi-layer structure. The pad is not restricted to the aforementioned rectangular configuration and may have various proper configurations. According to the configuration, the second region can be formed in a proper location beneath the noneffective bonding area.



Claims

1. A semiconductor device constituting a protection diode for protecting a semiconductor device area against a negative surge voltage applied to an interconnection pad, comprising:

a first semiconductor layer (21) of first conductivity type formed on a semiconductor substrate (22) of second conductivity type;

an interconnection pad (26) formed on a patterned insulating layer (25) formed on said first layer (21) and electrically connected to said semiconductor device area;

said diode comprising a second region (23) of said first conductivity type formed in said first semiconductor layer (21) substantially beneath a first opening in said patterned insulating layer (25) beneath a region of said interconnection pad (26) not utilized for wire bonding and electrically connected to the pad, said second region (23) having an impurity concentration higher than that of said first layer (21);

an area (24) of second conductivity type formed in a region of said first layer (21) around said pad and extending down to said substrate surface; and

an electrode (27) formed over said second conductivity type area (24), and electrically connected to the second conductivity type area (24) via a second opening in said patterned insulating layer (25).

2. The semiconductor device according to claim 1, characterized in that said pad is rectangular in shape, with said second region (23) being formed beneath each corner of the pad (26).

3. The semiconductor device according to claim 1, characterized in that said second conductivity type area (24) serves as an isolation layer for element isolation.

Patentansprüche

1. Halbleitervorrichtung, die eine Schutzdiode zum Schutze eines Halbleitervorrichtungsbereiches gegen einen negativen Spannungsstoß bildet, der an einen Verbindungskontakt-fleck angelegt wird, umfassend:

eine erste Halbleiterschicht (21) eines ersten Leitfähigkeitstyps, die auf einem Halbleitersubstrat (22) eines zweiten Leitungstyps gebildet ist; einen Verbindungsanschlußfleck (26), der auf einer gemusterten Isolierschicht (25) gebildet ist, die auf der ersten Schicht (21) aufgebracht ist und elektrisch mit dem Halbleitervorrichtungsbereich verbunden ist;

wobei die Diode aufweist:

einen zweiten Bereich (23) des ersten Leitungstyps, der in der ersten Halbleiterschicht (21) im wesentlichen unterhalb einer ersten Öffnung in der gemusterten Isolierschicht (25) unter einem für das Drahtbondieren nicht benutzten Bereich des Verbindungsanschlußfleckes (26) gebildet ist und elektrisch an den Kontakt-fleck angeschlossen ist, wobei der zweite Bereich (23) eine Fremdatomkonzentration besitzt, die größer als die der ersten Schicht (21) ist;

einen Bereich (24) eines zweiten Leitfähigkeitstyps, der in einem Bereich der ersten Schicht (21) um den Kontakt-fleck herum gebildet und sich nach unten zur Substratoberfläche erstreckt; und

eine Elektrode (27), die über der Schicht (24) des zweiten Leitfähigkeitstyps gebildet ist und elektrisch an den Bereich (24) des zweiten Leitfähigkeitstyps durch eine zweite Öffnung in der gemusterten Isolierschicht (25) angeschlossen ist.

2. Halbleitervorrichtung nach Anspruch 1, dadurch gekennzeichnet, daß der Kontakt-fleck eine rechteckige Form besitzt, wobei der zweite Bereich (23) unterhalb jeder Ecke des Kontakt-fleckes (26) gebildet ist.

3. Halbleitervorrichtung nach Anspruch 1, dadurch gekennzeichnet, daß der Bereich (24) des zweiten Leitfähigkeitstyps als Isolierschicht für die Elemententrennung dient.

Revendications

1. Dispositif à semiconducteur constituant une diode de protection pour protéger une zone de dispositif à semiconducteur contre une pointe de tension négative appliquée à une plage de connexion, comprenant:

- une première couche de semiconducteur (21) d'un premier type de conductibilité formée sur un substrat de semiconducteur (22) d'un deuxième type de conductibilité;

- une plage de connexion (26) formée sur une couche isolante (25) formée sur ladite première couche (21) et connectée électriquement à ladite zone de dispositif à semiconducteur;

ladite diode comprenant une deuxième région (23) dudit premier type de conductibilité dans ladite première couche de semiconducteur (21) sensiblement sous une première ouverture dans ladite couche isolante formant un motif (25), sous une région de ladite plage de connexion (26) non utilisée pour connecter des fils et connec-



tée électriquement à la plage de connexion, ladite deuxième région (23) ayant une concentration d'impuretés plus forte que celle de ladite première couche (21);

- une zone (24) du deuxième type de conductibilité formée dans une région de ladite première couche (21) autour de ladite plage de connexion et s'étendant vers le bas jusqu'à ladite surface du substrat; et 5
- une électrode (27) formée au-dessus de ladite zone du deuxième type de conductibilité (24) et connectée électriquement à la zone du deuxième type de conductibilité (24) par l'intermédiaire d'une deuxième ouverture dans ladite couche isolante formant un motif (25). 10 15

2. Dispositif à semiconducteur selon la revendication 1, caractérisé en ce que ladite plage de connexion a une forme rectangulaire, ladite deuxième région (23) étant formée sous chaque coin de la plage de connexion (26). 20

3. Dispositif à semiconducteur selon la revendication 1, caractérisée en ce que ladite zone du deuxième type de conductibilité 24 sert de couche isolante pour l'isolement d'éléments. 25

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