ENHANCED STRESS FOR TRANSISTORS

FIELD OF THE INVENTION

[0001] The present invention relates to semiconductor devices, and more particularly, to improving performance of transistors with stress engineering.

BACKGROUND OF THE INVENTION

[0002] Transistors are commonly used in the integrated circuits (ICs). Current ground rules, for example, below 90 nm, require higher carrier mobility. To improve carrier mobility (e.g., electrons or holes), strain engineering has been applied. Generally, inducing a tensile strain in the channel of n-type transistors improves electron mobility while a compressive strain in the channel of p-type transistors improves hole mobility. Various techniques have been proposed to induce the desired stress in the channel region of transistors. One technique includes forming stressors in source/drain regions of a transistor. Other techniques include, for example, providing the desired stress inducing material in the shallow trench isolations (STIs) or over the transistors as etch stop liners (ESLs).

[0003] However, we have discovered that conventional integration schemes applying stress engineering is ineffective. For example, current integration schemes counter the effect of the stress inducing materials, such as relaxing the stress being applied. This can undesirably affect transistor performance.

[0004] In view of the foregoing, it is desirable to provide effective stress inducement to improve transistor performance.

SUMMARY OF THE INVENTION

[0005] The present invention relates to improving transistor performance with stress engineering. In one aspect of the invention, a transistor comprises a gate disposed on a substrate, the gate includes spacers on gate sidewalls. The transistor further comprises diffusion

regions adjacent to the gate, and silicide contacts on the diffusion regions. The silicide contacts are displaced from the spacers by a distance G.

[0006] A transistor which includes a gate disposed on a substrate is presented in another embodiment of the invention. The transistor comprises a channel below the gate and diffusion regions adjacent to the gate separated by the channel. The transistor further includes silicide contacts on the diffusion regions. The silicide contacts being displaced from the channel by a distance G.

[0007] In another aspect of the invention, a method of forming a semiconductor device comprises providing a substrate having a transistor formed thereon. The transistor comprises a gate and first spacers on gate sidewalls. Sacrificial spacers are formed on the gate sidewalls over the first spacers, and contacts are formed adjacent to the gate. The sacrificial spacers are removed, wherein the contacts are displaced from the first spacers by a distance G equal to the width of the sacrificial spacers.

[0008] In another embodiment, a method of forming a semiconductor device comprises providing a gate disposed on a substrate, spacers on sidewalls of the gate and diffusion regions adjacent to the gate. Silicide contacts are formed on the diffusion regions, wherein the silicide contacts are displaced from the spacers by a distance G.

[0009] These and other objects, along with advantages and feature of the present invention herein disclosed, will become apparent through reference to the following description and the accompanying drawings. Furthermore, it is to be understood that the features of the various embodiments described herein are not mutually exclusive and can exist in various combinations and permutations.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] In the drawings, like reference characters generally refer to the same parts throughout the different views. Also, the drawings are not necessarily to scale, emphasis instead generally

being placed upon illustrating the principles of the invention. Various embodiments of the present invention are described with reference to the following drawings, in which:

[0011] Figs. 1a-b show a transistor in accordance with one embodiment of the invention;

[0012] Figs. 2a-i show a process for forming an IC in accordance with one embodiment of the invention;

[0013] Figs. 3a-d show a process for forming an IC in accordance with another embodiment of the invention;

[0014] Figs. 4a-b show SEM images of p-type transistors with and without a gap between transistor sidewall spacers and contacts on the source/drain regions; and

[0015] Fig. 5 shows Ion/Ioff characteristics of p-type transistors with and without a gap between transistor sidewall spacers and contacts on the source/drain regions.

DETAILED DESCRIPTION OF THE INVENTION

[0016] In the following description, details are set forth such as specific materials, parameters, etc. in order to provide a thorough understanding of the present invention. It will be evident, however, that the present invention may be practised without these details. In other instances, well-known process steps, equipment, etc. have not been described in particular detail so as not to obscure the present invention.

[0017] The present invention relates to transistors. The transistors can be incorporated into ICs. The ICs can be any type of IC, for example dynamic or static random access memories, signal processors, or system on chip devices, mixed signal or analog devices such as A/D converters and switched capacitor filters. Other types of ICs are also useful. Such ICs are incorporated in, for example, communication systems and various types of consumer products.

[0018] Figs. 1a-b show a portion of an IC 100 in accordance with one embodiment of the invention. Referring to Fig. 1a, the portion includes a transistor 140 formed in an active region 110 on a substrate 105. In one embodiment, the substrate comprises a silicon substrate. The

substrate, for example, comprises a lightly doped p-type substrate. Other types of substrates, such as silicon-on-insulator (SOI), are also useful. The active region is isolated from other device regions by, for example, shallow trench isolations (STIs) 180. Other types of isolation regions are also useful. The active region includes a doped well 115 of the second type on which a transistor of a first type is formed. In one embodiment, the first type comprises a p-type and the second type comprises n-type. For example, a p-type transistor is formed in a n-type doped well. Forming a n-type transistor in a p-type doped well is also useful.

[0019] The transistor comprises a gate stack 144 on the substrate. The gate stack includes a gate electrode 146 over a gate dielectric 145. Dielectric spacers 152 can be disposed on the sidewalls of the gate stack. The dielectric spacers, for example, are formed from silicon oxide. Other types of dielectric materials, such as silicon nitride or combination of materials, are also useful. Typically, the gate electrode is formed from polysilicon and the gate dielectric is formed from thermal oxide. Other types of materials are also useful. Source/drain diffusion regions 147a-b are located adjacent to the gate beneath the substrate surface. The source/drain diffusion regions are heavily doped with dopants of a first polarity type. For example, p-type transistors comprise p-type dopants in the source/drain diffusion regions while n-type transistors would comprise n-type dopants in the source/drain diffusion regions. Beneath the gate between the source/drain regions is a channel 143 of the transistor.

[0020] In one embodiment, source/drain stressors 165 are disposed in the source/drain regions of the transistors. In one embodiment, a first edge 168 of the stressors is aligned with the outer edge of the spacers. Providing stressors having a first edge which is not aligned with the outer edge of the spacers is also useful. For example, the first edge of the stressors may be aligned with the edge of the gate sidewalls. The edge of the stressor, for example, can be where the channel begins. As shown, a second edge 169 of the stressors abuts the STIs. Providing second stressors which do not abut the STIs is also useful.

[0021] The stressors comprise a first stress to induce the first stress in the channel of the first type transistor. The first stress comprises a compressive stress for a p-type transistor. Alternatively, the first stress can be a tensile stress for a n-type transistor. Other configurations of stress and transistors are also useful. The stressors preferably comprise a crystalline material. For example, silicon germanium can be used to induce a compressive stress. Other types of materials or inducing other types of stress are also useful. For example, silicon carbide can be used to induce a tensile stress.

[0022] Contacts 156 are provided over the diffusion regions and gate electrode. The contacts, for example, comprise metal silicide. The metal silicide can comprise nickel or a nickel alloy, such as nickel-platinum. Other types of metal silicides or conductive materials are also useful. In one embodiment, the contacts on the source/drain diffusion regions are formed by reacting metal with epitaxial silicon. Forming the contacts using other techniques is also useful.

[0023] In accordance with one embodiment of the invention, the metal contacts on the source/drain regions are disposed away from the first edge of the stressors, forming a gap G. Metal silicide contacts relax the stress induced in the channel region by the stressors, counteracting their effect. The gap G displaces the metal contacts away from the first edge of the stressors. This displacement reduces the negative impact of the contacts. In one embodiment, G is sufficient to reduce the relaxation of stress in the channel region due to the contacts. For example, G is about 5 – 30 nm. Preferably, G is about 10 nm. In an alternative embodiment, a second spacer 172 is provided, as indicated by the dotted lines. The second spacer aligns the contacts with a gap G away from the first edge of the stressors.

[0024] A stress layer 185 can be applied on the surface of the substrate covering the transistor, as shown in Fig. 1b. The stress layer, for example, is an etch stop layer (ESL). The stress layer comprises a first stress to induce the first stress on the channel. For example, the stress layer comprises a compressive stress. Other types of stress are also useful. In one

embodiment, the stress layer induces a compressive stress. The ESL stress layer preferably comprises a dielectric material. For example, the stress layer comprises silicon nitride. Other types of stress materials are also useful. Providing an ESL stress layer further enhances the stress induced on the channel of the transistor in addition to the stressors. Providing ESL stress layers without source/drain stressors is also useful.

[0025] Figs. 2a-i show a process for forming a portion of an IC 200 in accordance with one embodiment of the invention. Referring to Fig. 2a, a semiconductor substrate 205 is provided. The substrate, in one embodiment, comprises a lightly doped p-type silicon substrate. Other types of substrates are also useful, for example, silicon-on-insulator (SOI). The substrate is prepared with an active region 210. The active region comprises a heavily doped region 215 with dopants of second polarity type. To form the active region, conventional ion implantation techniques, such as implantation with a mask can be used. Other techniques for forming the active region are also useful.

[0026] Isolating the active regions from other device regions on the substrate are isolation regions 280. The isolation regions, for example, comprise STI regions. Various conventional processes can be employed to form the STI regions. For example, the substrate can be etched using conventional etch and mask techniques to form trenches which are then filled with dielectric material such as silicon oxide. Chemical mechanical polishing (CMP) can be performed to remove excess oxide and provide a planar substrate top surface. Typically, the STI regions are formed before the heavily doped region. Forming other types of isolation regions is also useful.

[0027] Referring to Fig. 2b, the process continues to form the gate layers on the substrate. For example, forming the gate layers comprises sequentially forming a gate dielectric layer 245 and a gate electrode layer 246 on the substrate surface. In one embodiment, the gate dielectric layer comprises thermal oxide. Other types of gate dielectrics are also useful. The gate

electrode layer, for example, comprises polysilicon. Other types of gate electrode materials, such as metal, are also useful. The gate layer, in one embodiment, can comprise a heavily doped polysilicon layer of the first polarity type. The polysilicon can be in-situ doped or doped by ion implantation after deposition, such as during formation of the source/drain diffusion regions. Providing undoped polysilicon is also useful.

[0028] In one embodiment, a cap layer 249 is provided over the gate electrode. The cap layer, for example, comprises a dielectric material such as silicon nitride. Other types of materials are also useful.

[0029] In Fig. 2c, the gate layers are patterned to form a gate stack 244. The gate layers can be patterned using conventional mask and etch techniques. For example, a photoresist mask is deposited and patterned to expose portions of the cap layer. The exposed portions of the cap layer and layers below are etched using an anisotropic etch such as reactive ion etching (RIE), resulting in the gate stack 244.

[0030] The process continues to form source/drain extensions adjacent to the gate stack. The extensions are formed by implanting first type dopants. P-type dopants are implanted for p-type transistors while n-type dopants are implanted for n-type transistors. In one embodiment, the source/drain extensions are formed by halo implants. Other techniques for forming the source/drain extensions are also useful.

[0031] In one embodiment, as shown Fig. 2d, a dielectric layer 251 is deposited on the substrate. The dielectric layer, in one embodiment, comprises silicon oxide. Other types of dielectric materials or combination of dielectric materials are also useful. The dielectric layer is anisotropically etched, for example by RIE, to remove horizontal portions, leaving sidewall spacers 252, as shown in Fig. 2e.

[0032] Referring to Fig. 2e, the substrate is etched to form stressor openings 260 adjacent to the gate stack. In one embodiment, the substrate is etched by RIE. Other techniques for forming

the stressor openings are also useful. The stressor openings, for example, are about 50 – 100 nm deep. In one embodiment, a first edge 268 of the stressor openings is aligned with the outer edge of the spacers and a second edge 269 of the stressor openings is aligned with the STIs.

[0033] Stressors 265 are formed in the stressor openings, as shown in Fig. 2f. In one embodiment, the stressors comprise a crystalline material. The stressors comprise a first stress which induces the first stress on the channel of the transistor. The first stress, in one embodiment, comprises a compressive stress. The stressors can apply a compressive stress in the channel of a p-type transistor. Other types of stresses are also useful, such as tensile stress for n-type transistors.

[0034] The stressors, in one embodiment, are formed by epitaxial growth. The growth fills the openings. For compressive stressors, the material used comprises a lattice parameter larger than that of the substrate in which the stressors are formed. Alternatively, for tensile stressors, the material used comprises a lattice parameter smaller than that of the substrate. Compressively stressed materials include doped SiGe and doped SiGeC, while tensile stressed materials include doped SiC. Other types of compressively or tensile stressed materials are also useful.

[0035] The process continues to form sacrificial spacers over the dielectric spacers. This includes forming a sacrificial layer 271 over the substrate, as shown in Fig. 2f. The sacrificial layer comprises a material which can be etched selectively to the spacers. In one embodiment, the sacrificial layer comprises a dielectric material such as silicon oxide. Other types of materials are also useful. The thickness of the sacrificial layer is sufficient to form the sacrificial spacers. The thickness of the sacrificial layer, for example, is about 5 – 30 nm. Other thicknesses are also useful. Various techniques, such as chemical vapor deposition (CVD) or others, can be used to form the sacrificial layer.

[0036] Referring to Fig. 2g, an anisotropic etch, such as RIE, is performed to remove the horizontal portions of the sacrificial layer. The etch forms sacrificial spacers 272 on sidewalls of

the gate over the spacers. The substrate can optionally be etched to form contact openings 266. The etch, for example, comprises a RIE. The etch advantageously is self-aligned since the STIs and sacrificial spacers serve as a mask.

[0037] In one embodiment, the contact fill 268 is selectively formed in the contact opening as shown in Fig. 2h. The contact fill preferably comprises a crystalline material, such as silicon. Other types of materials, such as polysilicon or amorphous silicon, are also useful. The contact fill fills the contact opening. Forming contact fill can be achieved by, in one embodiment, epitaxial growth. The contact fill facilitates subsequent process to form silicide contacts. After filling the contact opening, the cap layer is removed from the top of the gate stack. A conductive layer 276 is deposited on the substrate. The conductive layer comprises a metal or alloy, such as, for example, nickel, nickel platinum and cobalt.

[0038] Referring to Fig. 2i, a silicide process is performed to form silicide contacts 256 over crystalline layer filling the contact opening and over the gate electrode. The silicide contacts can be formed using conventional processes. Sacrificial spacers are then removed, creating a gap G between the contacts and spacers. The gap G should be sufficient to reduce the negative effect of the metal contacts on the stressors. For example, G is about 5 – 30 nm. Preferably, G is about 10 nm.

[0039] A stress layer (not shown) can be formed over the substrate, covering the transistor. The stress layer, for example, can additionally serve as an ESL. The stress layer comprises a first stress to induce the first stress on the channel. For example, the stress layer comprises a compressive stress. Other types of stress are also useful. In one embodiment, the stress layer induces a compressive stress. The ESL stress layer preferably comprises a dielectric material. For example, the stress layer comprises silicon nitride. Other types of stress materials are also useful. Providing an ESL stress layer further enhances the stress induced on the channel by the stressors.

[0040] Figs. 3a-d show a process of forming a portion of an IC 200 in accordance with another embodiment of the invention. Referring to Fig. 3a, a semiconductor substrate 205 is provided. The substrate is prepared with a transistor, for example, up to the point of processing as described in Fig. 2d. Source/drain diffusion regions 360 are formed by implanting dopants of the first type. For example, p-type dopants are implanted for p-type transistors and n-type dopants are implanted for n-type transistors.

[0041] The process continues to form sacrificial spacers over the dielectric spacers. This includes forming a sacrificial layer 271 over the substrate, as shown in Fig. 3b. The sacrificial layer comprises a material which can be etched selectively to the spacers. In one embodiment, the sacrificial layer comprises a dielectric material such as silicon oxide. Other types of materials are also useful. The thickness of the sacrificial layer is sufficient to form the sacrificial spacers. The thickness, for example, is about 5 – 30 nm . Other thicknesses are also useful. Various techniques, such as chemical vapor deposition (CVD) or others, can be used to form the sacrificial layer.

[0042] Referring to Fig. 3c, an anisotropic etch, such as RIE, is performed to remove the horizontal portions of the sacrificial layer. The etch forms sacrificial spacers 372 on sidewalls of the gate over the spacers. Optionally, the substrate is etched to form contact openings. A crystalline layer, such as silicon is selectively formed by epitaxial growth in the contact opening. Other types of crystalline material are also useful. After filling the contact opening, the cap layer is removed from the top of the gate stack. Metal silicide contacts 256 are formed in the source/drain regions and top of the gate electrode.

[0043] Referring to Fig. 3d, sacrificial spacers are then removed, creating a gap G between the contacts and spacers. The gap displaces the contacts away from the channel of the transistor. In one embodiment, G is about 5 – 30 nm. Preferably, G is about 10 nm. A stress layer 385 is formed over the substrate, covering the transistor. The stress layer, for example, serves as an

ESL. The stress layer comprises a first stress to induce the first stress on the channel. For example, the stress layer comprises a compressive stress. Other types of stress are also useful. In one embodiment, the stress layer induces a compressive stress. The ESL stress layer preferably comprises a dielectric material. For example, the stress layer comprises silicon nitride. Other types of stress materials are also useful. Providing an ESL stress layer further enhances the stress induced on the channel by the stressors. By providing a gap G between the silicide contacts, the ESL stress layer can be located closer to the channel of the transistor. This enhances the stress effects of the stress layer. Furthermore, displacing the contacts away from the channel reduces their stress relaxing effect.

[0044] Fig. 4 shows SEM images of ICs (a) without and (b) with a gap between the sidewall spacers and the metal silicide contacts formed in the source/drain regions. As seen from Fig. 4(a), where no gap is formed, the metal silicide contacts encroach on the channel region of the transistor. This relaxes the stress in the channel region, counteracting the effect of the stressors. In Fig. 4(b), in comparison, the contacts are displaced from the channel region, reducing their negative impact on channel stress.

[0045] Fig. 5 shows Ion/Ioff characteristics of p-type transistors (a) without and (b) with a gap between the sidewall spacers and the metal silicide contacts formed in the source/drain regions. As shown, a 20% improvement in transistor performance can be obtained when the gap is present.

[0046] The invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The foregoing embodiments, therefore, are to be considered in all respects illustrative rather than limiting the invention described herein. Scope of the invention is thus indicated by the appended claims, rather than by the foregoing description, and all changes that come within the meaning and range of equivalency of the claims are intended to be embraced therein.

What is claimed is:

CLAIMS:

1. A transistor comprising:

a gate disposed on a substrate with sidewalls spacers on gate sidewalls;

diffusion regions adjacent to the gate separated by a channel; and

silicide contacts on the diffusion regions, the silicide contacts being displaced from the sidewall spacers by a distance G.

2. The transistor of claim 1 wherein the distance G is about 5 to 30 nm.

3. The transistor of claim 1 further comprising stressors in the diffusion regions, the stressors induce a first stress in the channel of the transistor beneath the gate.

4. The transistor of claim 3 wherein the transistor is a p-type transistor and the first stress is a compressive stress.

5. The transistor of claim 3 wherein the distance G is sufficient to reduce the relaxation of the first stress by the silicide contacts.

6. The transistor of claim 3 wherein the distance G is about 5 to 30 nm.

7. The transistor of claim 1 further comprising a stress layer disposed on the substrate over the transistor.

8. The transistor of claim 7 wherein the distance G is about 5 to 30 nm.

9. The transistor of claim 3 further comprising a stress layer disposed on the substrate over the transistor.

10. The transistor of claim 9 wherein the distance G is about 5 to 30 nm.

11. A method of forming a semiconductor device comprising:

providing a substrate having a transistor formed thereon, the transistor comprises a gate and first spacers on gate sidewalls;

forming sacrificial spacers on the gate sidewalls over the first spacers;

forming contacts adjacent to the gate; and

removing the sacrificial spacers, wherein the contacts are displaced from the first spacers by a distance G equal to the width of the sacrificial spacers.

12. The method of claim 11 wherein the contacts comprise silicide contacts.

13. The method of claim 11 wherein the distance G is about 5 to 30 nm.

14. The method of claim 11 further comprising forming stressors in the diffusion regions, the stressors induce a first stress in a channel region of the transistor beneath the gate.

15. The method of claim 14 wherein the distance G is sufficient to reduce the relaxation of the first stress by the contacts.

16. The method of claim 14 wherein the distance G is about 5 to 30 nm.

17. The method of claim 11 further comprising forming a stress layer on the substrate over the transistor.

18. The method of claim 17 wherein the distance G is about 5 to 30 nm.

19. A method of forming a transistor comprising:

providing a gate disposed on a substrate, spacers on sidewalls of the gate and diffusion regions adjacent to the gate;

forming silicide contacts on the diffusion regions, wherein the silicide contacts are displaced from the spacers by a distance G.

20. A transistor comprising:

a gate disposed on a substrate;

a channel below the gate;

diffusion regions adjacent to the gate separated by the channel; and

silicide contacts on the diffusion regions, the silicide contacts being displaced from the channel by a distance G.