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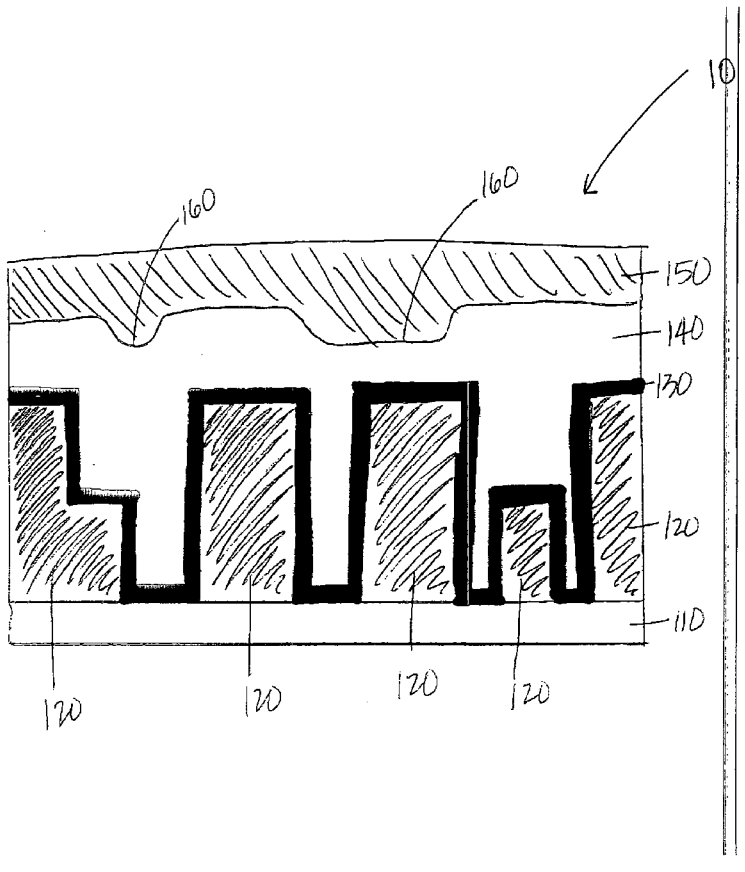
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(54) Title: PLANARIZERS FOR SPIN ETCH PLANARIZATION OF ELECTRONIC COMPONENTS AND METHODS OF USE THEREOF



(57) Abstract: An electronic component contemplated comprises a substrate layer (110), a dielectric layer (120) coupled to the substrate layer (110), a barrier layer (130) coupled to the dielectric layer (120), a conductive layer (140) coupled to the barrier layer (130), and a protective layer (150) coupled to the conductive layer (140). A method of making the electronic component comprises the steps of providing a substrate (110) coupling a dielectric layer (120) to the substrate (110), coupling a barrier layer (130) to the dielectric layer (120), coupling a conductive layer (140) to the barrier layer (130), and coupling a protective layer (150) to the conductive layer (140). A method of planarizing a conductive surface of the electronic component comprises the steps of introducing or coupling a protective layer (150) onto a conductive layer (140), dispersing the protective layer (150) across the conductive layer (140), curing the protective layer (150), introducing an etching solution onto the conductive layer (140), and etching the conductive surface to substantial planarity.

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