Formation Of Raised Source/Drain Structures In NFET With Embedded SiGe in PFET

Abstract

A structure and method for forming raised source/drain structures in a NFET device and embedded SiGe source/drains in a PFET device. We provide a NFET gate structure over a NFET region in a substrate and PFET gate structure over a PFET region. We form recesses in the PFET region in the substrate adjacent to the PFET second spacers. We form a PFET embedded source/drain stressor in the recesses. We form a NFET S/D epitaxial Si layer over the NFET SDE regions and a PFET S/D epitaxial Si layer over PFET embedded source/drain stressor. The epitaxial Si layer over PFET embedded source/drain stressor is consumed in a subsequent salicide step to form a stable and low resistivity silicide over the PFET embedded source/drain stressor.

Figure 10