# A METHOD OF MAKING DIRECT CONTACT ON GATE BY USING DIELECTRIC STOP LAYER

## BACKGROUND OF THE INVENTION

### (1) FIELD OF THE INVENTION

The present invention relates generally to a method of forming a semiconductor device, and more particularly to form low resistance gate contacts in a MOSTET device.

### (2) DESCTIPTION OF THE PRIOR ART

There has been increasing interest in the possible use of CMOS (complimentary metal-oxide-silicon) circuits for RF applications at > 900 MHz, such as mobile tele-communication devices. The reasons for this are: low fabrication cost of CMOS devices compared to the currently used bipolar and GaAs integrated circuits (IC), easy integration of analog and digital components, and fundamental advantages if attainable dynamic range when a frequency mixer is required in specific applications. Furthermore, the cut-off frequency of small geometry MOSFET has become comparable to that of advanced bipolar transistors. In addition, minimum noise figure (NFmin) has also improved in the submicron devices. For these reasons, CMOS devices will be increasingly used in RF front-end IC's.

In the case of high-frequency analog MOSFET's, while high trans-conductance is impor-

tant for high cut-off frequency and low noise characteristic, low gate resistance is essential for reducing thermal noise. In advanced device designs enabled by advances in process technologies, minimum feature sizes are continually decreasing. As a result, channel lengths in FET devices and thereby gate electrode widths have significantly decreased. One major problem associated with narrow gate electrode is its high electrical sheet resistance which impairs the device performance. Several methods have been proposed and used in prior art for reducing gate resistance. One method is to divide the gate electrode into several gate fingers, with each finger having provided with a contact hole, thereby increasing the total gate contact area. Another method is to use metal silicide contacts such as titanium, tungsten, or cobalt silicides or metal gates. The present invention proposes an alternate method of reducing gate contact resistance by directly contacting the gate poly-silicon with the contact metal.

U.S. Patent No. 5,731,239 describes a method for making low sheet resistance sub quarter micrometer gate electrode in FET devices. The method involves first patterning the gate from a doped poly-silicon layer. After forming the sidewall spacers and source/drain contact regions with Ti contacts, the insulating layer is chemically mechanically polished to the silicon nitride on the gate electrode layer. A pre-amorphizing implantation is done and a titanium silicide is selectively formed on the gate electrodes resulting in small grain sizes and reduced sheet resistance. Alternatively, cobalt silicide can also be formed on gate electrode to reduce the gate resistance.

U.S. Patent No. 6,010,945 describes a method to form a "mushroom shaped" gate structure that increases the top gate silicide contact area and improves the salicidation process.

The upper gate extensions increase the top gate surface area so that silicide gate contacts will have low resistivity.

U.S. Patent No. 6,271,087 B1 describes a method for forming self-aligned contacts and local interconnects. Multi-layer structures are formed on a semiconductor substrate; sidewall spacers are formed around the multi-layer structures; source and drain regions are formed; a stop layer is deposited over the substrate followed by the deposition of a dielectric layer over said stop layer. A first photo-resist contact mask is used to etch core contact and peripheral local interconnect openings. After stripping the first mask, a second contact mask is formed and the multi-layer structures are etched to form local interconnect openings. After removing the second mask, a conductive film is deposited over the dielectric layer and in the core and peripheral openings, followed by chemical mechanical polishing to remove the conductive film everywhere except in the core contact and local interconnect openings.

U.S. Patent No. 6,281,059 B1 describes a method of forming ESD protective transistor. This is done by ion implantation into the drain contact hole of the ESD protective transistor, wherein the contact hole is fabricated simultaneously with gate contact holes of the fundamental transistor and the ESD protective transistor. Both of the transistors have a respective metal silicide layer to cap the poly-silicon layer to prevent penetration of $p^+$ ions into poly-silicon while implanting into the contact holes.

## SUMMARY OF THE INVENTION

Accordingly, the main object of this invention is to describe a method of forming a MOSFET device with low resistance gate on a semiconductor substrate.

It is yet another object to describe a method to form low resistance gate contacts in a MOSFET device on a semiconductor substrate.

Another objective of the invention is to describe a MOSTET device with low resistance gate.

In accordance with these objectives, a CMOS RF device and a method to fabricate said device with low gate contact resistance are described. Conventional MOS transistor is first formed with isolation regions, gate structure, sidewall spacers, and implanted source/drain regions. An oxide layer like TEOS is deposited, planarized with chemical mechanical polishing (CMP) to expose the gate. Silicon nitride is then deposited and planarized with CMP, and then etched except around the gates using a gate poly-silicon oversize mask. Inter-level dielectric mask is then deposited; contact holes etched; and contact metal deposited to form the transistor. The resulting device structure achieves significantly reduced gate resistance.

## BRIEF DESCRIPTION OF THE DRAWINGS

The objects, advantages, and details of fabricating a semiconductor device according to

this invention will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings.

Figure 1 is a cross-section of a MOSFET device showing isolation trenches, gate structure, sidewall passivation, and lightly and heavily doped source/drain regions.

Figure 2 is a cross-section of the MOSFET device after depositing a dielectric layer, planarization, and HF dip.

Figure 3 is a cross-section of the MOSFET device after depositing a nitride layer and planarization.

Figure 4 is a cross-section of the MOSFET device after forming oversize mask over gate poly-silicon.

Figure 5 is a cross-section of the MOSFET device after etching the nitride and mask removal.

Figure 6 is a cross-section of the MOSFET device showing inter-level dielectric layer with contact holes etched and contact metal deposited.

## DETAILED DESCRIPTION OF THE INVENTION

The invention process begins with forming a dielectric layer over a MOSFET device known in prior art. Said MOSFET device **10**, with its components – filled isolation trenches **12**, gate structure **14** with gate poly-silicon **15**, sidewall passivation **16**, source/drain regions **18** with lightly doped **20** and heavily doped **22** regions shown in Figure 1. For simplicity, only n-channel part of the CMOS device formed in a p-type silicon substrate **24** is shown. Said structure could be formed in a p-tub formed in n-type silicon substrate or an MOS device.

A dielectric layer **26**, with a thickness of approximately between about 2000 °A and 5000 °A, comprising silicon dioxide, nitridized silicon dioxide, silicon oxy-fluoride (SiOF or FSG), tetra-ethyl-ortho-silicate (TEOS) is deposited using low pressure (LP) or plasma-enhanced (PE) chemical vapor deposition (CVD) methods known in prior art. Since the film is conformally deposited, the film covers the gate structures completely. The overburden is then planarized using a method comprising plasma etch back and/or chemical maechanical polishing. Planarization is done so as to expose the gate structures. The planarized wafer is subjected to a brief dilute HF dip so as to recess the oxide layer slightly below the gate structure, as shown in Figure 2. Amount of step below the gate level is approximately between 500 A and 1000 A, depending upon the thickness of gate poly-silicon used.

A silicon nitride layer **28**, with a thickness of approximately between about 1000 °A and 2000 °A, is deposited conformally and planarized with CMP or etch back methods, to expose the gate structure as shown in Figure 3. Although the preferred film is silicon nitride, other films

comprising oxygen doped silicon nitride, silicon oxy-nitride can alternatively be used.

An oversize photo-resist mask **30**, as shown in Figure 4, is formed over the structure of Fig. 3, such that only the nitride around the gate structure is preserved.

Nitride film **28** is etched selectively such that etching stops on the under-lying oxide film, using a plasma etching process known in prior art. The selective etching process uses a mixture of halogen containing gases (e.g. F, Cl, or Br) at low ion bombardment energy typically less than about 100 eV. The resulting structure after removing said resist mask is shown in Figure 5.

Figure 6 shows the completed device after the inter-level dielectric film **30** is deposited; contact holes **32** are etched; and contact metal **34** deposited using processes known in prior art. Said inter-level dielectric film, with thickness approximately between 8, 000 °A and 15,000 °A, comprises TEOS, borosilicate glass (BSG) and/or phosphorous silicate glass (PSG), deposited using LPCVD or PECVD method known in prior art. Un-etched nitride film surrounding the gate area acts as etch-stop during etching contact hole over the gate structure, preserving the sidewall spacers **16**.

The advantages of this invention over prior art are:

a) low resistance poly-silicon gate in a MOSFET structure,

b) improved high frequency noise performance in an RF CMOS device,

c) significant increase in maximum oscillation frequency and unit power gain frequency,

d) reduced RC gate delay

What is claimed is:

1. A method of forming a gate contact in a MOSFET device, the steps comprising:

forming a first dielectric layer on a substrate, having oxide-filled isolation trenches, gate structure, sidewall passivation around gate, source and drain with lightly and heavily doped regions;

planarizing said first dielectric layer and recessing said first dielectric layer below the level of said gate structure;

forming a second dielectric etch stop layer over said first dielectric layer;

planarizing said second dielectric layer in level with the gate structure;

pattern said second dielectric layer, using oversize gate mask to leave said second dielectric layer around said gate structure; and

forming electrical gate contact steps comprising: forming an inter-level dielectric layer over partially formed MOSFET device; patterning contact holes to source drain regions, patterning contact hole to gate stopping on said second dielectric layer; forming planarized metal patterns in and over said contact holes.

2. The method of forming a gate contact in a MOSFET device according to claim **1** wherein, said first dielectric layer comprises silicon dioxide, nitridized silicon dioxide, silicon oxy-fluoride, and/or tetraethylorthosilicate.

3. The method of forming a gate contact in a MOSFET device according to claim **2** wherein said first dielectric layer thickness is approximately between about 1000 °A and 3000 °A

after planarization.

4. The method of forming a gate contact in a MOSFET device according to claim **1** wherein, said first dielectric layer is planarized with steps comprising plasma etch back and/or chemical mechanical polishing.

5. The method of forming a gate contact in a MOSFET device according to claim **1** wherein, said first dielectric layer is recessed approximately between about 500 °A and 1000 °A.

6. The method of forming a gate contact in a MOSFET device according to claim **1** wherein, said second dielectric etch-stop layer comprises silicon nitride, oxygen doped silicon nitride, and/or silicon oxy-nitride.

7. The method of forming a gate contact in a MOSFET device according to claim **6** wherein, said second dielectric etch-stop layer thickness is approximately between about 500 °A and 1000 °A after planarization process.

8. The method of forming a gate contact in a MOSFET device according to claim **1** wherein, said second dielectric etch stop layer is planarized with steps comprising plasma etch back and/or chemical mechanical polishing.

9. The method of forming a gate contact in a MOSFET device according to claim **1** wherein, said inter-level dielectric layer comprises tetraethylorthosilicate, borosilicate glass and/

or phosphorous silicate glass.

10. The method of forming a gate contact in a MOSFET device according to claim 9 wherein, said inter-level dielectric layer thickness is approximately between about 8,000 °A and 15,000 °A.

11. A method of forming a poly-silicon gate contact in a MOSFET device, the steps comprising:

forming a silicon dioxide layer on a silicon substrate having oxide-filled isolation trenches, gate structure, sidewall passivation around gate, source and drain with lightly and heavily doped regions;

planarizing said silicon dioxide layer and recessing said silicon dioxide layer below the level of said poly-silicon gate structure;

forming a silicon nitride etch stop layer over said silicon dioxide layer;

planarizing said silicon nitride etch stop layer in level with the gate structure;

pattern said silicon nitride etch stop layer, using oversize poly-silicon gate mask to leave said silicon nitride layer around said poly-silicon gate structure; and

forming electrical poly-silicon gate contact steps comprising: forming an inter-level dielectric layer over partially formed MOSFET device; patterning contact holes to source drain regions, patterning contact hole to poly-silicon gate stopping on said silicon nitride etch stop layer; forming planarized metal patterns in and over said contact holes.

12. The method of forming a poly-silicon gate contact in a MOSFET device according to

claim **11** wherein, said post-planarized silicon dioxide layer thickness is approximately between about 1000 °A and 3000 °A.

13. The method of forming a poly-silicon gate contact in a MOSFET device according to claim **11** wherein, said silicon dioxide layer is planarized with steps comprising plasma etch back and/or chemical mechanical polishing.

14. The method of forming a poly-silicon gate contact in a MOSFET device according to claim **11** wherein, said silicon dioxide layer is recessed approximately between about 500 °A and 1000 °A.

15. The method of forming a poly-silicon gate contact in a MOSFET device according to claim **11** wherein, said silicon nitride layer thickness is approximately between about 500 °A and 1000 °A after planarization process.

16. The method of forming a poly-silicon gate contact in a MOSFET device according to claim **11** wherein, said silicon nitride layer is planarized with steps comprising plasma etch back and/or chemical mechanical polishing.

17. A MOSFET device structure comprising:

a semiconductor substrate having device elements comprising oxide-filled isolation trenches, gate structure, sidewall passivation around gate, source and drain with lightly and heavily doped regions;

first dielectric layer over said semiconductor substrate;

second dielectric etch stop layer over said first dielectric layer and around said gate structure;

inter-level dielectric layer over said MOSFET device structure; and

metal line, forming an electrical contacting with said gate.

18. A MOSFET device structure according to claim **17** wherein, said first dielectric layer comprises silicon dioxide, nitridized silicon dioxide, silicon oxy-fluoride, and/or tetraethyl-ortho-silicate.

19. The MOSFET device structure according to claim **17** wherein, said first dielectric layer thickness is approximately between about 1000 °A and 3000 °A.

20. The MOSFET device structure according to claim **17** wherein, said second dielectric etch-stop layer comprises silicon nitride, oxygen doped silicon nitride, and/or silicon oxy-nitride.

21. The MOSFET device structure according to claim **17** wherein, said second dielectric etch-stop layer thickness is approximately between about 500 °A and 1000 °A after planarization process.

22. The MOSFET device structure according to claim **17** wherein, said inter-level dielectric layer thickness is approximately between about 8,000 °A and 15,000 °A.