Claims:

What is claimed is:

1. A method of configuring a processor, the method comprising: receiving a program configured to run as software;

determining a first portion of the program to run in hardware, and a second portion of the program to run as software;

determining, based on the first portion, a plurality of interconnected reprogrammable operator blocks and dedicated data pathways interconnecting the plurality of operator blocks to form a hardware dataflow graph, wherein the dedicated data pathways comprise at least one feedback pathway coupling an output of a subsequent operator block to an input of a prior operator block; wherein the plurality of interconnected reprogrammable operator blocks comprise one or more transformation functions that take input data from a prior data bus, performs one or more transformations on the input data, and outputs transformed input data via an output data bus;

configuring the plurality of interconnected reprogrammable operator blocks to execute on one or more reprogrammable processors;

executing the second portion via one or more front-end processors;

sending first data from the one or more front-end processors to the one or more reprogrammable processors;

executing the first portion via the one or more reprogrammable processors by streaming data directly between the plurality of operator blocks via the dedicated data pathways without intermediate storage in a shared memory;

sending second data from the one or more reprogrammable processors to the one or more front-end processors; and

determining, based on the first data and second data, result data.

2. The method of claim 1, wherein determining a first portion further

comprises determining, based on computational complexity, the first portion of the program to run in hardware.

3. The method of claim 1, wherein the result data is a result of execution of the program.

4. The method of claim 1, wherein the second data is derived from the first data based on the one or more transformations.

5. The method of claim 1,wherein the result data is derived from the second data, and the second data is derived from the first data.

6. The method of claim 1, wherein the one or more reprogrammable processors is a field programmable gate array.

7. The method of claim 1, wherein sending the first data from the one or more front-end processors to the one or more reprogrammable processors further comprises sending the first data, via an expansion bus, from the one or more front-end processors to the one or more reprogrammable processors.

8. The method of claim 1, wherein receiving a program configured to run as software further comprises compiling the program into executable software code, a hardware configuration, and communication code for transferring data between the executable software code and the hardware configuration.

9. A conveyor belt processor, comprising:

an input data bus;

a plurality of interconnected reprogrammable operator blocks;

a plurality of dedicated data pathways interconnecting the plurality of reprogrammable operator blocks to form a hardware dataflow network configured to

process a stream of data without intermediate storage of the streamed data in an external shared memory, wherein the dedicated data pathways comprise at least one feedback pathway coupling an output of a subsequent operator block to an input of a prior operator block;

wherein the plurality of interconnected reprogrammable operator blocks comprise:

an input data bus, of a first reprogrammable operator block, coupled to an output data bus, of a second reprogrammable operator block, or the input data bus;

an output data bus, of a first reprogrammable operator block, coupled to an input data bus, of a third reprogrammable operator block, or an output data bus; and

one or more transformation functions that take input data from a prior data bus, performs one or more transformations on the input data, and outputs transformed input data via an output data bus; and the output data bus.

10. The conveyor belt processor of claim 9, wherein a bus width of the plurality of interconnected reprogrammable operator blocks are not the same.

11. The conveyor belt processor of claim 9, wherein an output of a subsequent block is an input of a previous block.

12. The conveyor belt processor of claim 9, wherein the second reprogrammable operator block and the third reprogrammable operator block are the same.

13. The conveyor belt processor of claim 9, wherein the third reprogrammable operator block are prior to the first reprogrammable operator block in execution order.

14. The conveyor belt processor of claim 9, further comprising a programming interface configured to receive instructions for creating the plurality of interconnected reprogrammable operator blocks.

15. A system for processing data, comprising:

a plurality of processors, each processor comprising:

an input data bus;

a plurality of interconnected reprogrammable operator blocks;

a plurality of dedicated data pathways interconnecting the plurality of reprogrammable operator blocks to form a hardware dataflow network configured to process a stream of data without intermediate storage of the streamed data in an external shared memory, wherein the dedicated data pathways comprise at least one feedback pathway coupling an output of a subsequent operator block to an input of a prior operator block;

wherein the plurality of interconnected reprogrammable operator blocks comprise:

an input data bus, of a first reprogrammable operator block,

an input data bus, of a first reprogrammable operator block, coupled to an output data bus, of a second reprogrammable operator block, or the input data bus;

an output data bus, of a first reprogrammable operator block, coupled to an input data bus, of a third reprogrammable operator block, or an output data bus; and

one or more transformation functions that take input data from a prior data bus, performs one or more transformations on the input data, and outputs transformed input data via an output data bus; and

the output data bus; and

a management function, wherein the management function

is configured to assign data to each processor.

16. The system of claim 15, wherein the management function is further configured to reconfigure the plurality of interconnected reprogrammable operator blocks.

17. The system of claim 15, wherein the management function comprises memory storing instructions to create the plurality of interconnected reprogrammable operator blocks of the plurality of processors.

18. The system of claim 15, further comprising at least one front-end processor with an architecture different than the plurality of processors.

19. The system of claim 18, wherein the at least one front-end processor comprises a general-purpose processor.

20. The system of claim 15, wherein the management function comprises: a secure interface configured to receive configuration changes; and an insecure interface configured to assign data to one or more processors of the plurality of processors.