

PROBE CARD AND METHOD FOR FABRICATING THE SAME

[0001] This application claims the benefit of Korean Application No. 10-2007-0046099, filed on May 11, 2007, which is hereby incorporated by reference.

[0002] This application claims the benefit of Korean Application No. 10-2007-0088270, filed on August 31, 2007, which is hereby incorporated by reference.

BACKGROUND

FIELD

[0003] The present disclosure relates a probe card and a method for fabricating the same, and more specifically to a probe card and a method for fabricating the same capable of minimizing process defect and improving thermal deformation, flatness, and alignment precision by fabricating probe modules in a chip unit size or comparable size and mounting them on a large area space transformer.

Discussion of the Related Art

[0004] Generally, a process for manufacturing a semiconductor is largely divided into a front-end process and a back-end process. The front-end process, which is a fabrication process, is a process for forming an integrated circuit pattern on a wafer. The back-end process, which is an assembly process, is a process for

forming an integrated circuit package by dividing the wafer into a plurality of chips, connecting a conductive lead or ball to each chip so as to provide electrical path to external devices and then molding the chips with epoxy, etc.

[0005] Prior to performing the assembly process, an electrical die sorting (EDS) process for testing the electrical characteristics of each chip is carried out. Defective chips are discriminated during the EDS process. Of the defective chips, reparable chips are repaired and irreparable chips are removed. As a result, it is possible to save time and cost in the following assembly process.

[0006] Such EDS process is performed in a probe station. The probe station usually consists of a probe chuck on which the wafer to be tested is seated and a test head having a probe card. A plurality of probes are provided on the probe card, wherein the probes electrically contact pads provided on the respective chips on the wafer so that they can check whether the corresponding chips are defective.

[0007] As the semiconductor technology develops, more chips are formed on a single wafer in order to reduce the manufacturing cost and improve the productivity. Recently, with the realization of a 300 mm wafer process, the increase in the number of chips per wafer is accelerated. Therefore, the development of the large area probe card becomes important in the wafer test field.

[0008] The conventional probe card for testing the large area wafer can be categorized into the substrate type and the block type from the vantage point of the

space transformer. The substrate type, which is a type providing a plurality of probes 102 on a space transformer 101, for example, a ceramic substrate, with a size corresponding to the wafer to be tested (FIG. 1), has advantages in facilitating the subsequent assembly of the space transformer and stably maintaining the probe alignment. However, unlike a general ceramic substrate, the ceramic substrate for the space transformer, which is a substrate having metal lines for providing electrical connection between the probe and the circuit board, is difficult to fabricate. Therefore, the fabricating cost is high. The problem of the ceramic substrate for the space transformer becomes more serious as the area of the substrate increases. At present, the production of a ceramic substrate for the space transformer corresponding to a 300 mm wafer has not been made yet.

[0009] Meanwhile, the block type is a type fabricating the large area probe card by dividing the area to be tested into multiple blocks 202, mounting the plurality of probes 203 on the respective blocks 202 and then precisely aligning the respective blocks 202 on a block fixing frame 201, as shown in FIG. 2. Considering the fabricating process, the block type has an advantage that it is possible to replace only the corresponding block when a problem occurs during the fabricating process or during the use. However, as the area to be tested increases, the number of blocks and the length of block to be precisely aligned are increased, too. Therefore,

it has the problems that much time is spent to precisely align the blocks in addition to the fact that the alignment of the blocks may deteriorate during the test.

SUMMARY

[0010] It is an object of the present invention to provide a probe card and a method for fabricating the same capable of minimizing process defect and improving thermal deformation, flatness, and alignment precision by fabricating probe modules in a chip unit size or comparable size and mounting them on a large area space transformer having vertical conductive medium.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The accompanying drawings, which are included to provide a further understanding of the implementations and are incorporated in and constitute a part of this disclosure, illustrate implementations and together with the description serve to explain the implementations. In the drawings;

[0012] FIG. 1 is a plan view of a probe card according to a prior art.

[0013] FIG. 2 is a plan view of a probe card according to another prior art.

[0014] FIG. 3 is a plan view of a probe card according to one implementation of the present invention.

[0015] FIG. 4 is an enlarged plan view of portion A of FIG. 3.

- [0016] FIG. 5 is a cross-sectional view taken along line B-B' of FIG. 4.
- [0017] FIG. 6 is a perspective view of FIG. 4.
- [0018] FIG. 7 is a divided perspective view of FIG. 6.
- [0019] FIG. 8 is an enlarged view of C portion of FIG. 6.
- [0020] FIG. 9 is a plan view of a side-positioned printed circuit board.
- [0021] FIG. 10 is a plan view of a lower-surface printed circuit board according to one implementation of the present invention.
- [0022] FIG. 11 is a flow chart for explaining a method for fabricating a probe card according to one implementation of the present invention.
- [0023] FIGS. 12, 13a to 13c, and 14a to 14c are process reference views for explaining a method for fabricating a probe card according to one implementation of the present invention.

DETAILED DESCRIPTION

[0024] Reference will now be made in detail to the implementations, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[0025] Hereinafter, a probe card and a method for fabricating the same according to one general implementation will be described in detail with reference to

accompanying drawings. FIG. 3 is a plan view of a probe card according to one implementation of the present invention. FIG. 4 is an enlarged plan view of portion A of FIG. 3. FIG. 5 is a cross-sectional view taken along line B-B' of FIG. 4. FIG. 6 is a perspective view of FIG. 4. FIG. 7 is a divided perspective view of FIG. 6. FIG. 8 is an enlarged view of C portion of FIG. 6. FIG. 9 is a plan view of a side-positioned printed circuit board. And, FIG. 10 is a plan view of a lower-surface printed circuit board according to one general implementation. In the figures, like reference numbers refer to like elements for convenience of explanation.

[0026] The probe card will be described according to one implementation of the present invention, with reference to FIGS. 3 to 10.

[0027] As shown in FIG. 5, the probe card 300 according to one implementation of the present invention has a form wherein a circuit board 360 and a space transformer 310 are sequentially stacked. Unit probe modules 320 contacting semiconductor chips (not shown) to be tested are provided on the space transformer 310. Electrical signals to and from the semiconductor chips through the contact of the unit probe modules 320 are transferred to the circuit board 360. Interposers 350 are further provided between the circuit board 360 and the space transformer 310 and a stiffener plate 370 is further provided on the rear surface of the circuit board 360. The detailed description thereof will be described below.

[0028] The probe card constituted by the combination of the circuit board 360 and the space transformer 310 according to the present invention provides the following advantages. Firstly, the space transformer 310 has an area corresponding to the area of the wafer to be tested, making it possible to facilitate the subsequent assembly; secondly, the unit probe module 320 provided on the space transformer 310 has a size corresponding to the size of the semiconductor chip or has a size corresponding to 20 to 1000 % of the size of the semiconductor chip; and thirdly, a plurality of vertical conductive media 330 are provided in the space transformer 310 and each of the vertical conductive medium 330 mediate the electrical connection between the unit probe module 310 and the circuit board 360.

[0029] Specifically, the space transformer 310 of the probe card according to one implementation of the present invention has a size corresponding to the area of the semiconductor wafer to be tested, as shown in FIG. 3. A plurality of unit probe modules 320 are arranged with intervals on the space transformer 310. Herein, the plurality of unit probe modules 320 may be repeatedly arranged to be spaced with predetermined intervals.

[0030] At the positions spaced from each of the unit probe modules 320, vertical apertures 311 are created at predetermined intervals, as shown in FIG. 7. The vertical apertures 311 penetrate the space transformer 310 up and down vertically or slantly and the vertical conductive medium 330 is mounted in the vertical

apertures 311, as shown in FIGS. 6 and 7. The number of the unit probe modules 320 provided between the vertical conductive medium 330 may be one or more. In other words, one or a plurality of unit probe modules 320 may be commonly connected to a particular vertical conductive medium 330.

[0031] The vertical apertures 311 may be provided at a position spaced from at least one side surface of the four side surfaces of the unit probe module 320, that is, the up, down, left and right surfaces thereof. In other words, the vertical aperture 311 may be formed at one side or two sides of the unit probe module 320 or formed at positions spaced from three side surfaces or four side surfaces. For convenience of explanation, the implementation of the present invention will be described below based on the fact that the vertical apertures are formed at two sides of the unit probe module 320.

[0032] Meanwhile, the space transformer 310 may be formed using any one of stainless steel, aluminum, invar, kovar, nobinite, SKD11, alumina, glass, and machinable ceramic. In the case where the space transformer 310 is formed of a metallic material, the vertical aperture 311 may be formed by drill machining or wire discharge machining, etc. In the case where the space transformer 310 is formed of a ceramic material, the vertical aperture 311 may be formed by drill machining, laser machining, or micro sandblast machining, etc.

[0033] Preferably, the unit probe module 320 provided on the space transformer 310 has a size corresponding to the size of the semiconductor chip or a size corresponding to 20 to 1000 % of the semiconductor chip. If the size of the unit probe module 320 becomes larger, the fabricating cost for the unit probe module increases and its yield decreases, but the assembly of the probe card becomes easier. If the size of the unit probe module 320 becomes smaller, the fabricating cost for the unit probe module decreases and its yield increases; but the assembly of the probe card becomes complicated. The present invention fabricates the unit probe module 320 so as to have a size corresponding to the size of the semiconductor chip or a size corresponding to 20 to 1000 % of the semiconductor chip, in consideration of the foregoing advantages and disadvantages regarding the size of the unit probe module 320.

[0034] The unit probe module 320 is constituted by an insulating probe body 321 and micro cantilevers 322 provided on the probe body 321, as shown in FIGS. 5 and 6. The micro cantilever 322 is constituted by a pillar 322a, a beam 322b, and a tip 322c and plays a role of contacting the tip 321c to a pad of the semiconductor chip to be tested. In addition to the micro cantilevers 322, metal lines 323 and pads 324 for transferring an electrical signal generated by the contact of the micro cantilevers 322 and the semiconductor chip to the circuit board 360 are provided on the upper surface of the probe body 321.

[0035] As described above, the electrical signal to and from the semiconductor chip are transferred through the circuit board 360. At this time, vertical conductive medium 330 plays the role of a primary medium of electrical transfer between the unit probe module 320 and the circuit board 360. The electrical signals transferred to the vertical conductive medium 330 are ultimately transferred to the circuit board 360 via the lower-surface conductive medium 340 and the interposer 350 inserted between the lower surface of the space transformer 310 and the circuit board 360. The description of the lower-surface conductive medium 340 will be given below.

[0036] The constitution and role of the vertical conductive medium 330 will be described in detail as follows. First, the vertical conductive medium 330 may be implemented by a printed circuit board as one implementation. Hereinafter, the vertical conductive medium 330 is referred to as a side-positioned printed circuit board 330 for convenience of explanation.

[0037] The side-positioned printed circuit board 330 has a conductive pattern 332 formed therein, wherein both ends of the conductive pattern 332 are exposed to the outside, as shown in FIG. 9. Bonding pads 333 are provided on both ends of the conductive pattern 332 to facilitate wire bonding with the pad 324 of the unit probe module 320 or with a bonding pad 341 of the lower-surface printed circuit board 340.

[0038] The side-positioned printed circuit board 330 can be fabricated by means of a general method for fabricating a printed circuit board. The fabricating method is already known and, thus, only the structure of the side-surface printed circuit board will be described in order to help the understanding of the present invention. As shown in FIG. 8, the side-positioned printed circuit board 330 has a structure of a multi-layer printed circuit board which is sequential stacking of a plurality of insulating substrates 331, wherein the conductive patterns 332 are provided on the respective insulating substrates 331. As such, there is an interface between the insulating substrates 331 by having a structure wherein the plurality of insulating substrates 331 are stacked, however, the interface does not exist in the multi-layer printed circuit board ultimately fabricated since heat and pressure are applied in the subsequent processes. In FIG. 8, a portion indicated by a dotted line indicates the interface between the insulating substrates 331; however, it does not actually exist and is indicated for the convenience of understanding in order to indicate that it consists of the plurality of insulating substrates 331.

[0039] Although both ends of the conductive pattern 332 of the side-positioned printed circuit board 330 are indicated as provided with the bonding pads 333; in the case where a cross sectional area of the conductive pattern 332 is sufficient for the wire bonding, the bonding pads 333 may be not created. In this case, both ends of the conductive pattern 332 play the role of the bonding pads 333.

On the other hand, in the case where the bonding pads 333 are required at both ends of the conductive patterns 332, a conductive material is deposited on both ends of the conductive pattern 332 through processes such as metal plating, thereby making it possible to form the bonding pads 333. In this case, if the thickness of the deposited conductive material is larger than a certain thickness, the surface of the bonding pad 333 does not have a flat shape but has a convex shape, and in such case, the surface of the bonding pad 333 can be flattened by means of a grinding process. For reference, it is preferable that the area of the bonding pad 333 has an area sufficient for performing one or plurality of wire bondings.

[0040] The reason why the side-positioned printed circuit board 330 comprises the plurality of insulating substrates 331 is to form more bonding pads 333 on the side-positioned printed circuit board 330. For example, in the case where the side-positioned printed circuit board 330 comprises a single or two insulating substrates 331, the number of the bonding pads 333 provided on the corresponding side-surface printed circuit board is limited considering the minimum distance between the bonding pads 333 because the bonding pads 333 are created only in one line. On the other hand, in the case where the side-positioned printed circuit board 330 comprises 3 to 20 insulating substrates 331, the distance between the bonding pads 333 is assured because the bonding pad is arrayed in multiple rows on the side-positioned printed circuit board 330 since the bonding pads 333 are created

at the interfaces of the insulating substrates 331. As a result, relatively more bonding pads 333 can be formed as compared to the case of the side-positioned printed circuit board 330 comprising a single or two insulating substrates 331. The increase in the number of the bonding pads 333 means that they can be connected to more micro cantilevers 322. Consequently, this serves as an advantage in employing a probe card with a large number of probes. For reference, in order to form more bonding pads 333, it is preferable that the conductive patterns 332 provided at the interfaces of the insulating substrates 331 are not provided at positions corresponding to the conductive patterns 332 provided at the interfaces adjacent thereto, but are arranged in a zigzag direction. Also, in addition to the side-positioned printed circuit board 330 comprising 3 to 20 insulating substrates 331, the side-positioned printed circuit board 330 can comprise of the insulating substrates 331 in a single layer or a double layer.

[0041] The bonding pad 333 at one surface of the side-positioned printed circuit board 330 is electrically connected to the pad 324 of the unit probe module 320 through wire bonding. The bonding pads 333 provided at the opposite surface of the side-positioned printed circuit board 330 are wire-bonded to the lower-surface conductive medium 340 provided at the lower surface of the space transformer 310.

[0042] Capacitors 381 can be installed on the bonding pads 333 of the side-positioned printed circuit board 330, as shown in FIG. 4. Here, it is preferable that the capacitor 381 is attached on the bonding pad 333 of the upper surface of the side-positioned printed circuit board 330 positioned adjacent to the micro cantilevers 322 of the unit probe module 320, in consideration of maximizing the noise attenuating effect of the capacitor or capacitors in the electrical signal transferred to the circuit board 360 from the unit probe module 320. When the capacitor is mounted on the bonding pad 333, the corresponding bonding pad need not be wire-bonded to the pad of the unit probe module.

[0043] Also, the capacitor 381 may be provided on the side surface of the side-positioned printed circuit board 330 as shown in FIG.5. In this case, a capacitor groove part 382 may be provided in the space transformer 310 at a position corresponding to the capacitor 381. The capacitor groove part 382 provides space in which the capacitor 381 is positioned, when the space transformer 310 is combined with the side-positioned printed circuit board 330.

[0044] Up to now, the constitution and role of the vertical conductive medium 330, i.e., the side-positioned printed circuit board 330 was described. Meanwhile, as described above, the lower-surface conductive medium 340 is provided at the lower surface of the space transformer 310, wherein the lower-surface conductive medium 340 may be realized by a printed circuit board as in the vertical conductive

medium 330. For the convenience of explanation, the lower-surface conductive medium 340 is referred to as the lower-surface printed circuit board 340 in the following description.

[0045] The lower-surface printed circuit board 340 is provided on the lower surface of the space transformer 310 as shown in FIG. 5, and the plurality of bonding pads 341 wire-bonded to the bonding pads 333 of the side-positioned printed circuit board 330 and a plurality of lands 343 contacting and connected to the interposers 350 are provided on the lower-surface printed circuit board 340 310, as shown in FIG. 10. The bonding pads 341 and the lands 343 are electrically connected to each other by means of a conductive material 342.

[0046] Up to now, the vertical conductive medium 330 and the lower-surface conductive medium 340 according to the present invention were described. The electrical connection between the unit probe module 320 and the circuit board 360 can be assured stably without needing to extend the micro cantilever 322 or a needle, using the vertical and lower-surface conductive media. Also, signal integrity between the tester and the wafer to be tested can be increased using the impedance-matched printed circuit board as an implementation of the vertical conductive medium 330 and the lower-surface conductive medium 340.

[0047] The interposer 350, the circuit board 360, and the stiffener plate 370 are provided on the rear surface of space transformer 310, as described above.

The interposer 350 plays a role of mediating the electrical connection between the lower-surface conductive medium 340 and the circuit board 360, and the circuit board 360 plays a role of transferring the electrical signal from the tester located outside to the unit probe module 320 or the signal generated by the semiconductor chip from the unit probe module 320 to the tester. Herein, the interposer 350 may be formed of a pogo pin or a pressure conductive rubber (PCR).

[0048] Meanwhile, the stiffener plate 370 is provided on the rear surface of the circuit board 360 to play a role of physically coupling and supporting the space transformer 310, the interposer 350, and the circuit board 360. The stiffener plate may be formed in a stacked structure and may be made of one of stainless steel, aluminum, invar, kovar, nobinite, and SKD11 and a combination thereof.

[0049] Also, each of the stiffener plate 370, the circuit board 360, the interposer 350, and the space transformer 310 is provided with a plurality of apertures 371. The apertures 371 provided in each of the stiffener plate 370, the circuit board 360, the interposer 350, and the space transformer 310 are provided at positions corresponding to each other. The apertures 371 completely penetrate through the stiffener plate 370, the circuit board 360 and the interposer 350, and partly penetrate through the space transformer 310. Preferably, screw threads are formed in the apertures 371 formed in the space transformer 310 and the stiffener

plate 370 so that the space transformer 310 and the stiffener plate 370 are coupled with the pulling screws 373 or the pushing screws 372.

[0050] The pulling screws 373 or the pushing screws 372 are provided in the respective apertures 371, wherein the pulling screws 373 and the pushing screws 372 may be alternately provided in the apertures 371 and the pulling screws 373 and the pushing screws 372 may be selectively provided. When the pulling screws 373 and the pushing screws 372 are provided in the plurality of apertures 371, the pulling screws 373 or the pushing screws 372 are selectively operated so that they can push or pull the space transformer 310 up or down. With this, the deformation of the space transformer 310 is prevented so that the flatness of the space transformer 310 can be maintained constantly.

[0051] The above description of the constitution of the probe card according to one implementation of the present invention is limited to the constitution that the size of the space transformer corresponds to the size of the semiconductor wafer to be tested. However, the probe card having the space transformer smaller than the size of the semiconductor wafer to be tested may have the same constitution as the implementation of the present invention and this belongs to the scope of the present invention. Also, the above description is limited to the constitution that the unit probe modules 320 provided on the space transformer are repeatedly arranged.

However, it is apparent to those skilled in the art that the unit probe modules can be freely provided at desired positions.

[0052] Up to now, the constitution of the probe card according to one implementation of the present invention was described. Hereinafter, a method for fabricating a probe card according to one implementation of the present invention will be described. FIG. 11 is a flow chart for explaining a method for fabricating a probe card according to one implementation of the present invention. FIGS. 12, 13a to 13c, and 14a to 14c are process reference views for explaining a method for fabricating a probe card according to one implementation of the present invention.

[0053] According to one implementation of the present invention, a method for fabricating a probe card comprising the steps of forming a vertical aperture penetrating through a space transformer and positioning an vertical conductive medium in the formed vertical aperture, attaching a plurality of unit probe modules to be seated on positions spaced from the vertical conductive medium inserted in the space transformer, and electrically connecting the respective unit probe modules to the vertical conductive medium provided in the space transformer.

[0054] First, the unit probe module is fabricated as shown in FIG. 11 (S101). To this end, a substrate 501 and a silicon wafer 601 on which a plurality of unit probe module regions 502 are defined are prepared as shown in FIG. 12. As used herein, the unit probe module region 502 refers to a region in which one unit probe module

is formed. Each unit probe module region 502 is divided by means of a scribe line in consideration of a subsequent unit probe module cutting process. Herein, as the substrate 501 a glass substrate or a ceramic substrate may be used and the size of the substrate 501 is preferably the same as the size of the silicon wafer 601. Also, it is preferable that the silicon wafer 601 has a $\langle 110 \rangle$ crystal direction.

[0055] Next, a silicon oxide film or a silicon nitride film is formed on the silicon wafer 601 using any one of a thermal chemical vapor deposition (thermal CVD) method, a physical vapor deposition (PVD) method, and a plasma-enhanced chemical vapor deposition (PECVD) method, as shown in FIG. 13a. Then, the silicon oxide film or the silicon nitride film is selectively patterned through a photolithography process and an etching process to form an etch mask 602 defining micro cantilever forming regions.

[0056] In the state where the surface of the silicon wafer 601 corresponding to the micro cantilever forming region is exposed by the etch mask 602, the exposed silicon wafer 601, that is, the silicon wafer 601 in the micro cantilever forming region, is vertically etched at a depth of 5 to 500 μm through an anisotropic wet etching using KOH solution. With this, the micro cantilever in a pillar shape (322a) is formed and a space D in which the micro cantilever can be elastically deformed is assured.

[0057] Although not shown in the drawings, a conductive material is deposited on the substrate 501 and inverted patterns of the metal lines and pads are formed.

[0058] Next, the etched surface of the silicon wafer 601 contacts the substrate 501 as shown in FIG. 13b and a fusion bonding of the silicon wafer 601 to the glass substrate is then performed by applying a pressure between 1 to 5 atmospheric pressures at a temperature of 300 to 600 °C. In addition to the fusion bonding, an anodic bonding of the silicon wafer 601 to the substrate 501 may be employed by applying a voltage of 100 to 2000 V and a current of 1 to 100 mA at a temperature of 200 to 500 °C in the state where the glass substrate contacts the silicon wafer 601.

[0059] Thereafter, a photoresist pattern (not shown) defining the beam and tip of the micro cantilever is formed on the silicon wafer 601 through the photolithography process and the exposed silicon wafer 601 is etched using the photoresist pattern as the etch mask to form the beam 322b and tip 322c of the micro cantilever 322, as shown in FIG. 13c. At this time, it is preferable that the silicon wafer 601 is etched by the anisotropic wet etching using KOH. In order to attain a preferred shape of the beam 322b and tip 322c of the micro cantilever 322, the photolithography process and the etching process can be performed several times. Meanwhile, the upper surface of the silicon wafer 601, that is, the surface of the silicon wafer 601 not contacting the substrate, may be machined into a proper

thickness through a grinding process or a chemical mechanical planarization (CMP) process before the beam 322b and tip 322c of the micro cantilever are formed through the photolithography process and the etching process.

[0060] After the pillar 322a, the beam 322b, and the tip 332c of the micro cantilever 322 are completed through the above processes, although not shown in the drawings, the conductive material is deposited on the substrate and a lift-off process is performed so that the inverted pattern of the metal lines and pads formed on the substrate before performing the bond process of the substrate to the silicon wafer is removed and the desired metal lines and pads are formed, thereby completing the manufacturing of the unit probe module 320. Herein, the substrate is the probe body (reference number 321 of FIG. 6) of the unit probe module 320.

[0061] Meanwhile, it is preferable that the unit probe module 320 formed corresponds to the size of the semiconductor chip or has the size corresponding to 20 to 1000 % of the semiconductor chip.

[0062] When the plurality of unit probe modules 320 are formed on the substrate 501, the substrate 501 is cut along the scribe line 503 to obtain the plurality of unit probe modules 320 with the same size. Then, a defect inspection on the respective unit probe modules 320 is performed to select the unit probe modules 320 with good quality.

[0063] Then, the space transformer 310 having an area corresponding to the wafer to be tested is prepared (S102). The space transformer 310 is provided with the vertical apertures 311 penetrating through the space transformer 310 and the vertical conductive medium 330 is inserted into the vertical apertures 311, as shown in FIG. 14a. For reference, vertical conductive medium 330 inserted in the vertical apertures 311 may be fixed in position by epoxy, etc. Also, the lower surface of the space transformer 310 is provided with the lower-surface conductive medium 340.

[0064] After the space transformer 310 is prepared, the unit probe modules 320 are transferred and mounted on the space transformer 310 using a transfer apparatus, for example, a vacuum chuck (S103). At this time, when transferring and mounting the unit probe module 320, the lower surface of body of the unit probe module 320 contacts the upper surface of the space transformer 310. When transferring the unit probe module 320, the transfer means picks up the upper surface of the body where the micro cantilever 322 are not formed, strictly speaking, the predetermined portion of upper surface of the body where the ~~microprobe~~ micro cantilevers 322 are not formed and transfers it. Also, the transfer means may pick up the side surface of the body and transfer it. When attaching the unit probe module 320 on the space transformer 310, the unit probe module 320 has to be accurately placed at a predetermined position on the upper surface of the space transformer 310 and the heights of the arranged unit probe modules 320 should be constant.

[0065] First, in order to accurately place the unit probe module at the predetermined position on the upper surface of the space transformer and in order to prevent misalignment, alignment marks may be formed on each of the upper surfaces of body of the unit probe modules 320 and the upper surface (or lower surfaces) of the space transformer 310 or the tip 321c of the micro cantilever 322 provided on the unit probe module 320 may be utilized as the alignment mark.

[0066] Subsequently, in order to make the heights of the unit probe modules 320 arranged on the space transformer 310 constant, the heights of the unit probe modules 320 can be maintained constant by interposing epoxy between the space transformer 310 and the unit probe modules 320 and controlling the thickness of the corresponding epoxy (see t1 and t2 of FIG. 5a). With this, the heights of the micro cantilevers 322 provided on the unit probe modules 320 are also maintained constant. The reason of controlling the heights of the unit probe modules 320 by controlling the thickness of epoxy is that the large area space transformer 310 does not have uniform flatness.

[0067] After the respective unit probe modules 320 are attached on the space transformer 310, the electrical connection from the unit probe modules 320 through the space transformer 310 is performed. In detail, the pads of the unit probe modules 320, are connected with the one side of the bonding pads 333 of the vertical conductive medium 330, and the opposite side the bonding pads 333 of the

vertical conductive medium 330 are connected to the bonding pads 333 of the lower-surface conductive medium 340 by wire bonding(S103) as shown in FIG. 14b.

[0068] After the electrical connection between the respective unit probe modules 320 and the space transformer 310 is completed, the interposer 350, the circuit board 360, and the stiffener plate 370 are sequentially stacked on the rear surface of the space transformer 310 and are coupled to each other, as shown in FIG. 14c (S104). Herein, the interposer 350, which plays a role of electrically connecting the space transformer 310 and the circuit board 360, is preferably formed of a pogo pin or a pressure conductive rubber (PCR). The stiffener plate 370, which plays a role of physically coupling and supporting the probe card comprising the space transformer 310, the interposer 350, and the circuit board 360, may be formed of stainless steel, etc.

[0069] After the interposer 350, the circuit board 360, and the stiffener plate 370 are coupled on the rear surface of the space transformer 310, the process of providing the pushing screw 372 and the pulling screw 373 is performed (S105). At this time, each of the stiffener plate 370, the circuit board 360, the interposer 350, and the space transformer 310 is provided with the plurality of apertures 371 and the apertures formed in each of the stiffener plate 370, the circuit board 360, the interposer 350, and the space transformer 310 are positioned to correspond to each other. Herein, the aperture 371 completely penetrates through the stiffener plate

370, the circuit board 360, and the interposer 350 and partly penetrates through the space transformer 310. Also, the screw thread is formed in the aperture 371 of the space transformer 310 so that the space transformer is coupled with the pulling screw 373 or the pushing screw 372. The respective apertures 371 may be formed at the positions that correspond to the portions where the unit probe modules 320 are attached or at the positions that do not correspond to the portions where the unit probe modules 320 are attached.

[0070] Then, the pushing screws 372 and the pulling screws 373 are provided in the respective apertures 371. The pushing screws 372 and the pulling screws 373 may be alternately provided in the apertures 371 or the pushing screws 372 and the pulling screws 373 may be selectively provided depending on the apertures 371.

[0071] As the pushing screws 372 and the pulling screws 373 are provided as such, the pushing screws 372 and the pulling screws 373 are selectively operated so that they can push or pull the space transformer 310 up or down. With this, the deformation of the space transformer 310 is prevented and in the case where the micro cantilever 322 of the particular unit probe module 320 is provided at higher position or lower position than the other micro cantilever 322, the position of the micro cantilever 322 of the corresponding unit probe module 320 can be corrected accurately.

[0072] According to one general implementation, a probe card and a method for fabricating the same according to the present invention provide the following advantageous effects.

[0073] The space transformer has an area corresponding to the area of the wafer to be tested, making it possible to facilitate the subsequent assembly of the space transformer, and the probe module provided on the space transformer has a size corresponding to the size of a semiconductor chip or has a size corresponding to 20 to 1000 % of the size of the semiconductor chip, making it possible to improve the yield of the probe card.

[0074] Also, the side on which the micro cantilevers are not provided is safely seated on the space transformer when transferring the unit probe module, making it possible to improve alignment precision. Further, the particular portions of the space transformer can be selectively pulled or pushed by means of pushing screws and pulling screws provided in a rear surface of a stiffener plate, making it possible to assure a uniform flatness.

[0075] Exemplary implementations of the present invention have been disclosed herein, and although specific terms are employed, they are used and are to be interpreted in a generic and descriptive sense only and not for purpose of limitation. Accordingly, it will be understood by those of ordinary skill in the art that

various changes in form and details may be made without departing from the spirit and scope of the present invention as set forth in the following claims.

WHAT IS CLAIMED IS:

1. A probe card for testing semiconductor chips on a semiconductor wafer comprising:

a circuit board receiving electrical signals from outside;

a plurality of unit probe modules contacting the semiconductor chips on the wafer to transfer the electrical signals, wherein the unit probe module has a plurality of micro cantilevers;

a space transformer having the plurality of unit probe modules seated on the upper portion thereof and electrically connected to the circuit board, wherein the respective probe modules are arranged with intervals from each other on the space transformer and the space transformer has vertical apertures penetrating through it up and down ; and

at least one vertical conductive medium electrically connecting the respective unit probe modules and the circuit board, wherein the vertical conductive medium is inserted in the vertical apertures provided in the space transformer and the respective unit probe modules are arranged at positions spaced from the vertical conductive medium,

wherein each of the vertical conductive medium transfer the electrical signals of the plurality of micro cantilevers to the circuit board through one vertical aperture, and each of the vertical conductive medium includes a plurality of conductive patterns.

2. The probe card according to claim 1, wherein the unit probe module has a size corresponding to the size of the semiconductor chip.

3. The probe card according to claim 1, wherein the unit probe module has a size corresponding to 20 to 1000 % of the size of the semiconductor chip.

4. The probe card according to claim 1, wherein the vertical conductive medium comprises a printed circuit board which has a plurality of insulating substrates and a plurality of conductive patterns on the interfaces of the insulating substrates.

5. The probe card according to claim 4, wherein both ends of the conductive patterns are exposed to outside, bonding pads are provided on both ends of the exposed conductive patterns, the bonding pad provided at one side of the conductive pattern is exposed to the upper surface of the space transformer, and the bonding pad provided at the other side of the conductive pattern is exposed at the lower surface of the space transformer.

6. The probe card according to claim 1, further comprising a capacitor provided on the vertical conductive medium.

7. The probe card according to claim 5, further comprising a capacitor provided on the bonding pad of the vertical conductive medium.

8. The probe card according to claim 6, wherein the space transformer at a position corresponding to the capacitor is provided with a capacitor groove part and the capacitor groove part provides a space in which the capacitor is positioned, when the space transformer and the vertical conductive medium are coupled.

9. The probe card according to claim 5, wherein the bonding pad exposed to the upper surface of the space transformer is wire-bonded to the unit probe module.

10. The probe card according to claim 1, wherein the unit probe module comprises:

a probe body seated on the upper surface of the space transformer;

micro cantilevers provided on the upper surface of the probe body;

metal lines provided on the upper surface of the probe body electrically connected to the micro cantilevers; and

pads provided at one end of the metal lines.

11. The probe card according to claim 10, wherein a lower surface of body of the unit probe module is fixed on the upper surface of the space transformer by using epoxy as a medium.

12. The probe card according to claim 11, wherein the heights of the respective unit probe modules seated and fixed on the space transformer are identical with each other by means of a control of the thickness of epoxy.

13. The probe card according to claim 1, further comprising a lower-surface conductive medium electrically connected to each of the vertical conductive medium and the circuit board on a lower surface of the space transformer.

14. The probe card according to claim 13, wherein the lower-surface conductive medium further comprising lands, metal lines, and bonding pads,

wherein the bonding pads of the lower-surface conductive medium are wire-bonded to the vertical conductive medium.

15. The probe card according to claim 1, further comprising an interposer between the space transformer and the circuit board and a stiffener plate on a rear surface of the circuit board.

16. The probe card according to claim 15, further comprising a plurality of apertures completely penetrating through the stiffener plate, the circuit board, and the interposer and partly penetrating through the space transformer, the apertures formed in each of the space transformer, the interposer, the circuit board, and the stiffener plate being positioned to correspond to each other.

17. The probe card according to claim 16, further comprising pulling screws and pushing screws provided in each of the plurality of apertures, the pushing screws or the pulling screws being selectively operated so that they can push or pull the space transformer up or down.

18. The probe card according to claim 13, wherein the vertical conductive medium and the lower-surface conductive medium comprise an impedance-matched circuit board.

19. A method for fabricating a probe card comprising the steps of:
forming vertical apertures penetrating through a space transformer up and down at one side of the space transformer and inserting a vertical conductive medium in the formed vertical apertures;

generating a plurality of unit probe modules having a plurality of micro cantilevers, and arranging the unit probe modules with intervals each other on the

space transformer; and

electrically connecting the respective unit probe modules to a circuit board through the vertical conductive medium provided in the space transformer,

wherein each of the vertical conductive medium transfer the electrical signals of the plurality of micro cantilevers to the circuit board through one vertical aperture, and each of the vertical conductive medium includes a plurality of conductive patterns.

20. The method according to claim 19, wherein the step of generating the unit probe modules is prepared through the steps of:

selectively etching portions corresponding to a micro cantilever forming regions of a silicon wafer;

bonding an etched surface of the silicon wafer to a substrate;

forming micro cantilevers by selectively patterning and etching the silicon wafer bonded to the substrate;

forming metal lines and pads on the substrate; and

forming a plurality of unit probe modules by cutting the substrate along scribe lines defined on the substrate.

21. The method according to claim 20, wherein the substrate is formed of any one of glass material or ceramic material and the bonding of the silicon wafer to the substrate is performed by means of any one of a fusion bonding method or an

anodic bonding method.

22. The method according to claim 19, wherein the space transformer is formed of any one of stainless steel, aluminum, invar, kovar, nobinite, SKD11, alumina, glass, and machinable ceramic.

23. The method according to claim 19, wherein the step of seating each of the unit probe modules on the space transformer comprises transferring and seating the unit probe modules on the space transformer using a transfer apparatus and transferring the unit probe modules by picking up the upper surface or the side surface thereof.

24. The method according to claim 19, wherein the vertical conductive medium comprises a plurality of insulating substrates and a plurality of conductive patterns on the interfaces of the insulating substrates, both ends of the conductive patterns are exposed to outside, and bonding pads are provided on both ends of the exposed conductive patterns, and the bonding pads are formed through the steps of depositing conductive materials on the both ends of the conductive patterns and flattening them by grinding the stacked conductive materials.

25. The method according to claim 19, further comprising the steps of:

sequentially stacking and coupling an interposer, a circuit board, and a stiffener plate on a rear surface of the space transformer;

mounting pushing screws pushing the space transformer up or pulling screws pulling the space transformer down in the apertures formed in each of the space transformer, the interposer, the circuit board, and the stiffener plate being positioned to correspond to each other; and

making the heights of the plurality of unit probe modules constant by selectively controlling the pushing screws and the pulling screws.

ABSTRACT OF THE DISCLOSURE

The present disclosure relates to a probe card for testing semiconductor chips on a semiconductor wafer comprising: a circuit board receiving electrical signals from outside; a plurality of unit probe modules contacting the semiconductor chips on the wafer to transfer the electrical signals; a space transformer having the plurality of probe modules seated on the upper portion thereof and electrically connected to the circuit board, wherein the respective probe modules are arranged at intervals from each other on the space transformer and the space transformer has vertical apertures penetrating through it up and down; and at least one vertical conductive medium electrically connecting the respective unit probe modules and the circuit board, wherein the vertical conductive medium is arranged in the vertical apertures provided in the space transformer and the respective unit probe modules are arranged at positions spaced from the vertical conductive medium.

Fig. 3