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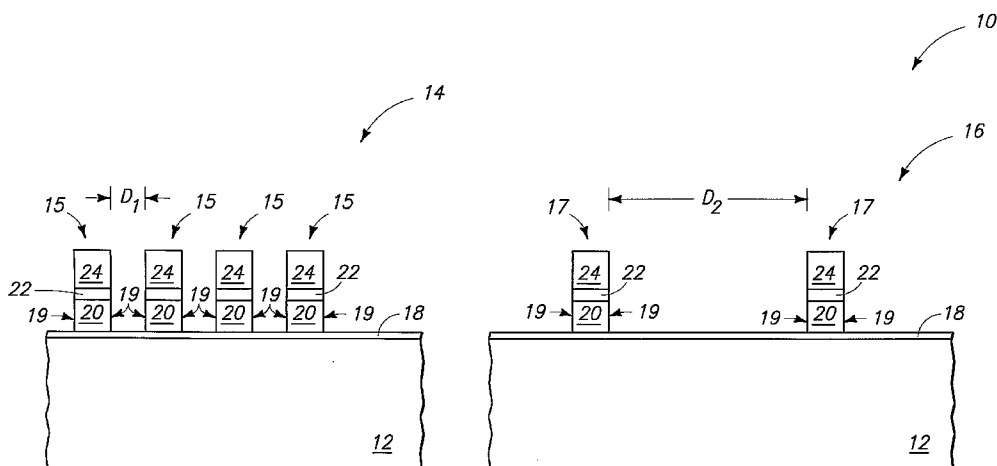
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(54) Title: METHODS OF FORMING MEMORY CIRCUITRY WITH DIFFERENT INSULATIVE SIDEWALL SPACERS



(57) Abstract: The invention includes methods of forming memory circuitry. In one implementation, a substrate (12) is provided which has a memory array circuitry area (14) and a peripheral circuitry area (16). The memory array circuitry area comprises transistor gate lines (15) having a first minimum line spacing (D_1). The peripheral circuitry area comprises transistor gate lines (17) having a second minimum line spacing (D_2) which is greater than the first minimum line spacing. Anisotropically etched insulative sidewall spacer (34) are formed over opposing sidewalls of individual of said transistor gate lines within the peripheral circuitry area prior to forming anisotropically etched insulative sidewall spacers (40) over opposing sidewalls of individual of said transistor gate lines within the memory array area. Other aspects and implementations are contemplated.

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