



VARIABLE GAIN LOW NOISE AMPLIFIER



Field of the Invention

This invention relates generally to the control of the gain of amplifiers or other high
5 frequency blocks such as filter attenuators etc. by switching the load impedance. The
invention in particular relates to controlling the gain of a Low Noise Amplifier (LNA).

Background of the Invention

The problem of gain control versus the noise figure (NF) of low noise amplifiers as
10 frequencies go steadily higher in the Giga Hertz range is a continuing challenge to all
workers in this field. We now describe a circuit of the related art by referring to Fig. 1.
Fig. 1 is taken from US 6,046,640 (Brunner), discussed below, and is referred there to as
Fig. 6. The circuit is a switched-gain cascode amplifier, including an input stage 26, a
loading network 24, first and a second cascode transistors Q22, Q23, and a bias signal
15 generator 22. The input stage 26 receives a bias signal V_{BIAS} and the input signal V_{IN} .
The loading network 24 is coupled to a power supply voltage V_{CC} and provides an output
signal V_{OUT} to a load. The input to the base of the first cascode transistor is a gain
control signal V_G . The input to the base of the second cascode transistor is a base control
signal V_{BC} . As mentioned the load is connected to the loading network 24 which
20 attenuates the output signal by a different amount depending on which input terminal the
signal is switched to.

Listed below are related patents and a publication which bear on this problem:

US 6,466,095 B1 (Susuki) dated Oct 15, 2002, Power Amplifier:-- relates to gain
25 variation and power amplification, whereas our invention, described below, is for a low
noise amplifier (LNA). Unlike the LNA, the Power Amplifier (PA) is a large signal
block, i.e., it deals with higher signal power. The main performance criterion for a PA is
efficiency while for the LNA the main performance criterion is the Noise Figure (NF). In
addition, the circuit of the PA itself is different from the LNA. The PA gain control
30 scheme is also entirely different and can not be applied to the LNA.

US 6,392,492 B1 (Yuan) dated May 21, 2002, High Linearity Cascode Low Noise Amplifier, and EP 0 977 352 A2 (Fong), Noise Figure and Linearity Improvement Technique using Shunt Feedback:-- both patents are for LNAs and teach techniques to improve the Noise Figure and linearity of the LNA in its normal (High Gain) mode of operation, whereas our invention proposes a gain control circuit for the LNA. The proposed Variable Gain LNA achieves the best Noise Figure in the High Gain mode and best linearity (surely better than the achievable linearity of the quoted patents) in the Low Gain mode. In addition, the reduced gain in the Low Gain mode greatly reduces the linearity requirements of the following blocks like Mixers, Filters etc, resulting in a power-efficient overall receiver. Reduced gain also reduces the dynamic range of the AGC circuit, which helps to improve the Signal to Noise Ratio (SNR).

US 6,046,640 (Brunner) dated Apr 04, 2000, Switched-Gain Cascode Amplifier Using Loading Network for Gain Control:-- this patent also is about Variable Gain LNAs. This circuit bypasses both AC and DC signals to ground in the Low Gain mode, whereas our proposed circuit bypasses only the AC signal to ground thereby not wasting the DC power. The main advantage of doing so in our scheme is that the Noise Figure and Linearity in the Low Gain mode is improved substantially. Also the input impedance is unaffected and the gain flatness is improved during gain variation. Another advantage is that one can get any amount of gain control with this circuit. Based on the requirement, the circuit can be optimized for the gain variation or the linearity or both in the Low Gain mode.

Related Publication: Gain Controllable Very Low Voltage (≤ 1 V) 8-9 GHz Integrated CMOS LNA's, T.K.K. Tsang and M.N. El-Gamal,," *IEEE RFIC Symposium 2002*. The scheme proposed in this publication controls the gate bias of the PMOS transistor in the folded cascode topology and does not sacrifice the NF in Low Gain mode. A parallel tank circuit is used from VDD to the amplifier which needs lots of care to achieve in a commercially packaged LNA. The gain control scheme which we propose not only achieves a better NF but also a superior third order intercept point (IIP3) in the Low Gain mode.

Summary Of The Invention

It is an object of at least one embodiment of the present invention to provide a circuit and a method where the load of the cascode amplifier is varied by connecting another (secondary) load in parallel with the original load through a switch which also acts as a
5 voltage controlled resistor.

It is another object of the present invention to provide a number of such switchable loads which are connected across the load to obtain programmability of the gain.

10 It is yet another object of the present invention to vary the load impedance as a function of a control voltage.

It is still another object of the present invention to improve the noise figure and to reduce the linearity requirements in low gain mode.

15 It is a further object of the present invention to use the bias current effectively in the low gain mode.

These and many other objects have been achieved by connecting a secondary load through
20 a MOSFET switch. During the High Gain Mode the MOSFET switch is OFF and the secondary load is electrically isolated from the main load, whereas in the Low Gain Mode the switch is turned ON and the secondary load appears across the primary load, thereby reducing the effective load impedance. The secondary load is AC coupled such that the DC bias current does not pass through the secondary load and hence the Noise Figure
25 (NF) and linearity (IIP3) performance are better in the Low Gain Mode.

These and many other objects and advantages of the present invention will be readily apparent to one skilled in the art to which the invention pertains from a perusal of the claims, the appended drawings, and the following detailed description of the preferred
30 embodiments.

Brief Description Of The Drawings

FIG. 1 is a circuit diagram of a switched-gain amplifier of the related art;

FIG. 2 is a circuit diagram illustrating the principle of the present invention;

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FIG. 3 is circuit diagram of one preferred embodiment of the circuit diagram of FIG. 2;

FIG. 4 is circuit diagram of another preferred embodiment of the circuit diagram of FIG. 2 present invention; and

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FIG. 5 is a block diagram of the method for implementing the circuit diagram of FIG. 2.

Use of same reference numbers in different figures indicates similar or like elements.

15 Detailed Description Of The Preferred Embodiment

Referring now to Figure 2 we describe the general principle of the invention. The Variable Gain low noise amplifier (LNA) 10 comprises a cascode amplifier stage 12 and a gain control circuit 14. The cascode amplifier stage comprises in series between the positive and negative terminal of a power supply, respectively Vdd and ground (GND) by way of illustration, a primary load L_L , transistors M2 and M1, inductor L_s and a current source I_D , which has capacitor C_s shunted across it. Input $R_{f\text{ in}}$ is coupled via inductor L_g and capacitor C_g to the gate of transistor M1. The gate of transistor M2 is coupled to Vdd. The junction J between transistor M2 and load L is coupled via capacitor C_o to the output node P of the LNA. Coupled between output node P and the negative terminal of the power supply (ground) is gain control circuit 14. Gain control circuit 14 typically comprises, in series between output node P and ground, a capacitor C_x , transistor M3, and a secondary load L_x . The gate of transistor M3 is coupled to a control voltage V_c . The gate bias voltage is the gain control voltage V_c and is varied from 0 to Vdd. Not shown is the primary load of the next stage coupled to output node P.

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When $V_c=0$ V, M3 is OFF and the gain control circuitry offers a high impedance at P

with respect to ground. Hence, the output of the LNA is delivered to the next stage and the whole LNA operates in High Gain mode. When $V_c = V_{dd}$, M3 will be in the ON state and offers a low resistance between its drain and source. Now, the secondary load appears effectively across the load of the LNA, thereby reducing the overall load impedance and hence results in reduced gain of the LNA. In other words, part of the output of the first stage is shunted to ground and therefore the overall gain is reduced.

The advantage of this scheme is that the drain current of M1 and M2 (and thus the gate overdrive) remains the same, even in the Low Gain mode and hence the Noise Figure (NF) and third order intercept point (IIP3) performance of the first stage is not sacrificed. In fact, there is a slight improvement in IIP3 of the first stage due to the reduced gain.

In order to maintain the gain flatness, the impedance Z_{O1} at output node P with respect to ground must remain in the same quadrant (in the real and imaginary plane) in the desired frequency band when M3 is ON as well as OFF. When M3 is OFF, this impedance is due only to the primary load L_L . In the absence of the secondary load, Z_{O1} would not be in the same plane due to the presence of C_{gs} and C_{sb} of M3, when M3 is ON. Hence the secondary load L_x is adjusted to keep Z_{O1} in the same plane.

When V_c takes on values between 0 and 1.8V, M3 acts as a voltage controlled resistor. Therefore the load impedance is varied as a function of V_c and thus the gain can be varied continuously by varying the control voltage V_c . The size of M3 determines the amount of gain control that can be achieved.

Figure 3 shows a Variable Gain LNA according to a first embodiment of the invention. Figure 3 is similar to Figure 2, except that a) a decoupling capacitor C_D is coupled between V_{dd} and ground, b) loads L_L and L_x are shown as inductors, c) resistive means R_b is coupled between the gate of M3 and V_c , and d) capacitor C_b is coupled between the gate of M3 and ground.

The LNA is matched to the input impedance through L_g , L_s and the gate-to-source capacitance C_{gs} (not shown) of M1 for the desired frequency band of operation. Capacitor C_s is used to provide RF ground to L_s . Transistors M1 (Common Source) and M2 (Common Gate) form the cascode amplifier. C_d is the decoupling capacitor.

5 Inductive Load L_L is used rather than a resistive load as the inductive load offers lower NF and better IIP3. The overlap transistor gate-to-drain capacitance C_{gd} (not shown) of M2 and the load inductance L_L determine the output impedance Z_{O1} . Usually the input impedance of the following stage is optimized for gain and gain flatness with respect to this Z_{O1} . The network consisting of C_x , M3, L_x , R_b and C_b is the gain control circuitry.

10 C_x blocks the DC current from entering the gain control circuit since we want to bypass only the AC signal to ground through M3 and L_x . M3 acts as a voltage controlled resistor controlled by V_c .

When M3 is OFF, Z_{O1} is inductive because of L_x . In the absence of the secondary load,

15 when M3 is ON, Z_{O1} becomes capacitive due to the presence of C_{gs} and C_{sb} (not shown) of M3. The secondary load inductor L_x ensures that Z_{O1} is inductive even when M3 is ON. Since Z_{O1} remains inductive for all values of V_c the gain flatness is not affected. The low pass network consisting of R_b and C_b at the gate of M3 is to isolate the RF from DC. By adding a resistive means (not shown) in series with L_x , one can trade off gain

20 and IIP3. In fact, L_x can be replaced by any RLC network based on the requirements of IIP3 and gain step. Since the drain current of M1 and M2 does not pass through M3 for all values of V_c , the NF and IIP3 are even better when M3 is ON (Low Gain Mode).

In a second preferred embodiment of the present invention the primary and secondary

25 loads L_L and L_x are RLC networks consisting of series and parallel combinations of all the three elements or two or one of the RLC elements. In fact, the secondary load L_x is added to get the gain flatness and in its simplest form can be replaced by a short.

In a third preferred embodiment of the present invention the switching means shown as

30 NMOSFETs can be PMOSFETs or can be implemented in BJT or BiCMOS technology as well.

In a fourth preferred embodiment of the present invention this technique of bypassing the signal through a voltage-controlled resistive means can be used for any CMOS, BJT or BiCMOS circuit like a filter, Mixer, Power Amplifier etc and is not limited to a LNA.

5 In a fifth preferred embodiment of the present invention a number of such gain control circuits are combined into a gain control block 16 and connected as shown in Figure 4 for gain programmability. Figure 4 is similar to Figure 2 as far as the cascode amplifier stage 12 is concerned but has gain control block 16 coupled to the output node P. In addition, capacitor C_{out} is coupled between output node P and the primary load (not shown) of the
 10 next stage. Gain control block 16 comprises an analog-to-digital converter (ADC) and decoder 18, which is driven by analog control signals. Coupled between output node P and the ADC&Decoder 18 are a plurality of control circuits ranging from 1,2, to n, comprising switching means S1, S2, to Sn and corresponding secondary loads SL1, SL2 to SLn. Where switching means 'n' in series with secondary load 'n' are coupled between
 15 output node P and ground. ADC&Decoder 18 has 'n' outputs, where outputs 1, 2, to n go to the gate of switching means 1, 2, to n, respectively. It is thus possible to activate any one, a combination or all (there are n^2 combinations) of the secondary loads. Decoders of this type are well known to those skilled in the art and need not to be explained further. This allows complete programmability of the secondary load.

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Referring now to Figure 5, we describe the method of varying the gain of a low noise amplifier:

Block 1 provides a cascode amplifier stage driving a primary load;

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Block 2 couples a secondary load across the primary load at the output of the cascode amplifier stage;

Block 3 couples a switching means between the secondary load and the output of the cascode amplifier stage;

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Block 4 applies a control voltage to the switching means to vary the impedance of

the switching means;

Block 5 switches the switching means into the OFF state, thereby switching the low noise amplifier into a high gain mode;

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Block 6 switches the switching means into the ON state, thereby switching the low noise amplifier into a low gain mode, and

Block 7 couples a plurality of secondary loads across the primary load.

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While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

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What is claimed is:

1. A low noise amplifier comprising:
a cascode amplifier stage with an input and an output, said amplifier stage delivering an amplified high frequency input signal to a primary load at said output,
5 where the load of said cascode amplifier stage is varied by coupling a secondary load in parallel with said primary load; and

a gain control circuit coupled to said output of said cascode amplifier stage, said gain control circuit for providing said secondary load, where said secondary load is
10 coupled via switching means to said output of said cascode amplifier stage, where said secondary load is varied by controlling the conductance of said switching means.
2. The low noise amplifier of claim 1, wherein said cascode amplifier stage is in a high gain mode when said switching means is not conducting.
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3. The low noise amplifier of claim 1, wherein said secondary load is electrically isolated from said primary load when said switching means is not conducting.
4. The low noise amplifier of claim 1, wherein said cascode amplifier stage is in a
20 low gain mode when said switching means is conducting.
5. The low noise amplifier of claim 1, wherein said secondary load is coupled across said primary load when said switching means is conducting, thereby reducing the effective load seen by said cascode amplifier stage.
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6. The low noise amplifier of claim 1, wherein said secondary load is AC coupled using capacitive means such that a DC bias current cannot pass through said secondary load.
- 30 7. The low noise amplifier of claim 1, wherein said switching means acts as a voltage controlled resistive means.

8. The low noise amplifier of claim 7, wherein said voltage controlled resistive means is varied as the control voltage is varied at the control gate of said switching means.
- 5 9. The low noise amplifier of claim 1, wherein a plurality of said switching means is arranged in a series/parallel circuit.
10. The low noise amplifier of claim 9, wherein said switching means is a NMOS transistor.
- 10 11. The low noise amplifier of claim 9, wherein said switching means is a PMOS transistor.
12. The low noise amplifier of claim 9, wherein said switching means is a BJT
15 transistor.
13. The low noise amplifier of claim 1, wherein a plurality of said secondary loads is arranged in a series/parallel circuit.
- 20 14. The low noise amplifier of claim 13, wherein said secondary load is a resistive means.
15. The low noise amplifier of claim 13, wherein said secondary load is an inductive means.
- 25 16. The low noise amplifier of claim 13, wherein said secondary load is a capacitive means.
17. A variable gain low noise amplifier comprising:
30 a cascode amplifier stage with an input and an output, said amplifier stage delivering an amplified high frequency input signal to a primary load at said output,

where the load of said cascode amplifier stage is varied by coupling a secondary load, through a load switching means, in parallel with said primary load; and

a gain control circuit coupled to said cascode amplifier stage and a power supply having positive and negative terminals, the gain control circuit electrically extending between said output of said cascode amplifier and the negative terminal of the power supply, where said variable gain low noise amplifier is in a low gain mode when said secondary load is switched in through said load switching means, and where said variable gain low noise amplifier is in a high gain mode when said secondary load is switched out.

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18. The variable gain low noise amplifier of claim 17, wherein said cascode amplifier stage further comprises:

a first gain stage means coupled to a second gain stage means, where the control gate of said first gain stage means is coupled, via a first capacitive means in series with a first inductive means, to said input of said cascode amplifier stage; where the source of said first gain stage means is coupled via a second inductive means in series with a current source to the negative terminal of said power supply, where the drain of said second gain stage means is coupled via a third inductive means to the positive terminal of said power supply, and where the junction of said drain of said second gain stage means and said third inductive means is coupled to said output of said cascode amplifier stage.

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19. The variable gain low noise amplifier of claim 17, wherein said gain control circuit further comprises:

a first capacitive means, said load switching means, and said secondary load all in series and coupled between said output of said cascode amplifier stage and the negative terminal of said power supply, where the control gate of said load switching means is coupled via resistive means to a control input providing a control voltage.

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20. The variable gain low noise amplifier of claim 19, wherein said load switching means acts as a voltage controlled resistive means which is varied as said control voltage is varied at the control gate of said load switching means.

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21. The variable gain low noise amplifier of claim 17, wherein the control gate of said load switching means is coupled via a second capacitive means to the negative terminal of said power supply.
- 5 22. The variable gain low noise amplifier of claim 17, wherein said load switching means of said gain control circuit is conducting when said secondary load is switched in.
23. The variable gain low noise amplifier of claim 17, wherein said load switching means of said gain control circuit is not conducting when said secondary load is switched
10 out.
24. The variable gain low noise amplifier of claim 17, wherein a plurality of said switching means is arranged in a series/parallel circuit.
- 15 25. The variable gain low noise amplifier of claim 24, wherein said load switching means is a NMOS transistor.
26. The variable gain low noise amplifier of claim 24, wherein said load switching means is a PMOS transistor.
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27. The variable gain low noise amplifier of claim 24, wherein said load switching means is a BJT transistor.
28. The variable gain low noise amplifier of claim 17, wherein a plurality of said
25 secondary loads is arranged in a series/parallel circuit.
29. The variable gain low noise amplifier of claim 28, wherein said secondary load is a resistive means.
- 30 30. The variable gain low noise amplifier of claim 28, wherein said secondary load is an inductive means.

31. The variable gain low noise amplifier of claim 28, wherein said secondary load is a capacitive means.

32. A low noise amplifier comprising:

5 a cascode amplifier stage with an input and an output, said amplifier stage delivering an amplified high frequency input signal to a primary load at said output, where the load of said cascode amplifier stage is varied by coupling a secondary load in parallel with said primary load; and

10 a programmable gain control coupled to said output of said cascode amplifier stage to provide said secondary load, said programmable gain controller comprising:

a plurality of load elements;

a plurality of switching means electrically coupled to the plurality of load elements for one of coupling and decoupling each of the plurality of load elements to said output of said cascode amplifier stage; and

15 a decoding means in electrical communication with the load switching means,

whereby the decoding means receives and decodes a control signal to therefrom select at least one of the plurality of loads corresponding thereto for coupling to said output of said cascode amplifier to thereby vary the gain of said cascode amplifier stage.

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33. The low noise amplifier of claim 32, wherein said cascode amplifier stage further comprises:

a first gain stage means coupled to a second gain stage means, where the control gate of said first gain stage means is coupled, via a first capacitive means in series with a first inductive means, to said input of said cascode amplifier stage; where the source of said first gain stage means is coupled via a second inductive means in series with a current source to the negative terminal of said power supply, where the drain of said second gain stage means is coupled via a third inductive means to the positive terminal of said power supply, and where the junction of said drain of said second gain stage means and said third inductive means is coupled to said output of said cascode amplifier stage.

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34. The low noise amplifier of claim 32, wherein said programmable gain control further comprises:

an analog-to-digital converter and decoder with a number of outputs equal to the plurality of said load elements, where each of said load elements comprises said load
5 switching means in series with an impedance and coupled between said output of said cascode amplifier stage and the negative terminal of a power supply with a positive and a negative terminal, where the control gate of each of said load switching means is coupled to one of said outputs of said analog-to-digital converter and decoder.

10 35. The low noise amplifier of claim 32, wherein said secondary load is varied as the control voltage is varied at the control gate of said load switching means.

36. The low noise amplifier of claim 32, wherein a plurality of said switching means is arranged in a series/parallel circuit.

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37. The low noise amplifier of claim 36, wherein said load switching means is a NMOS transistor.

38. The low noise amplifier of claim 36, wherein said load switching means is a
20 PMOS transistor.

39. The low noise amplifier of claim 36, wherein said load switching means is a BJT transistor.

25 40. The low noise amplifier of claim 32, wherein said secondary load is a resistive means.

41. The low noise amplifier of claim 32, wherein said secondary load is an inductive means.

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42. The low noise amplifier of claim 32, wherein said secondary load is a capacitive means.

43. A gain control circuit comprising:

5 a capacitive means, a load switching means, and a load, all in series, and coupled between the output of said gain control circuit and a reference potential, where the input of said gain control circuit is coupled to the control gate of said load switching means, where a control voltage, applied to said input, controls the impedance of said gain control circuit, such that when said load switching means is switched off to create a high
10 resistance between the terminals of said switching means, a high impedance is provided by said gain control circuit between said output and said reference potential, and when said load switching means is switched on to create a low resistance between the terminals of said switching means, a low impedance is provided by said gain control circuit between said output and said reference potential.

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44. The gain control circuit of claim 43, wherein a capacitive means is coupled between said output and said load switching means to provide AC coupling for said load.

45. The gain control circuit of claim 43, wherein said control voltage when varied,
20 varies the gain of a filter circuit when coupled to said output of said gain control circuit.

46. The gain control circuit of claim 43, wherein said control voltage when varied, varies the gain of a mixer circuit when coupled to said output of said gain control circuit.

25 47. The gain control circuit of claim 43, wherein said control voltage when varied, varies the gain of an amplifier circuit when coupled to said output of said gain control circuit.

48. A method of varying the gain of a low noise amplifier, comprising the steps of:
30 a) providing a cascode amplifier stage driving a primary load;

- b) coupling a secondary load across said primary load at the output of said cascode amplifier stage;
- c) coupling a switching means between said secondary load and the output of said cascode amplifier stage;
- 5 d) applying a control voltage to said switching means to vary the impedance of said switching means;
- e) switching said switching means into the off state, thereby switching said low noise amplifier into a high gain mode;
- f) switching said switching means into the on state, thereby switching said low
10 noise amplifier into a low gain mode, and
- g) coupling a plurality of said secondary loads across said primary load.

49. The method of claim 48, whereby the gain of said low noise amplifier can be varied continuously by varying said control voltage.

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50. The method of claim 48, where controlling said secondary loads through a decoder, provides programmability of the gain of said low noise amplifier.