Description

The present invention relates to an input protecting circuit in use with a MOS semiconductor device for protecting a gate insulating film of a transistor contained in an input stage from a high voltage noise.

One of the major problems in the IC device, which frequently arises after a manufactured IC chip is packaged, is a breakdown due to ESD (Electric Static Discharge). This is a gate breakdown phenomenon caused through a occurence that when a charged object such as a human body or mechanical object makes contact with an external pin or pins of the packed IC, charges flow from the object to the inside of the IC package, and consequently a high voltage is applied to the gate of the MOS transistor in the input stage of the IC semiconductor circuit, and possibly damages the gate of the transistor. To protect the gate from excessive stress, some measure must be taken to clamp the voltage applied to the gate.

A typical measure thus far taken is to place protecting element 62 of a diode or a bipolar transistor, for example, near and in connection with input pad 61 connected to an external pin (not shown) of an IC package, as shown in Fig. 1. Provision of protecting element 62 clamps an excessively high or surge voltage applied to input pad 61, and inhibits the surge voltage from traveling and reaching MOS transistor 63 in the input stage. Thus, the protecting element is located near the input pad. The reason for this is that the protecting element may operate as a latch-up generating source, for example, to adversely influence the internal circuit, and hence the protecting element must be located apart from the internal circuit to such an extent that it has little adverse effect on the internal circuit.

For the thick gate oxide film of the MOS transistor 63, the above protecting circuit satisfactorily functions. In a recent trend of thinner oxide films, the conventional protecting circuit is frequently nonfunctional. This will be described in detail by using a specific example. In the circuit of Fig. 1, let us consider a case that protecting element 62 is an aluminum field transistor (equivalent to a bipolar transistor) of which the channel width is 500 μm, and the interval between the source and drain diffusion regions, 2.4 μm, and the gate oxide film of MOS transistor 63 in the input stage is 25nm (250 Å) thick. In this case, a breakdown voltage at the pn junction of this transistor is approximately 15 V. If it is clamped at approximately 15 V, an electric field applied to the gate of the MOS transistor in the input stage is 6 MV/cm at most. There is no danger that such an electric field will break down the gate.

The EIAJ Standard for the ESD evaluation method has gradually been replaced by the MIL Standard. The evaluation conditions (100 pF, 1.5 kilo ohms) under the MIL Standard was applied for evaluating the conventional protecting circuit. In the evaluation, when a voltage of approximately ±1400 V was applied to input pad 51, gate breakdown was observed. When the applied voltage is positive in polarity, the electric field applied to the gate is 6 MV/cm. When it is negative, the applied electric field is much smaller than the former and gate breakdown cannot occur. Nevertheless, gate breakdown was actually observed for both the positive and negative voltages applied. No one has exactly explicated the cause of this phenomenon. We reason that the inductance component involved in the wire probably makes a great contribution to the gate breakdown. This will be described below. Normally, aluminum wire of several mm in length exists ranging from the protecting element placed near the input pad inside the IC to the internal circuit. The wire has inductance L of approximately several tens nH.

It is assumed now that an ESD stress is applied to an external pin (not shown), and a high voltage noise as shown in Fig. 2(A) is applied to the input pad. Under this condition, a potential near the wire connecting to protecting element 62 is clamped at the breakdown voltage Vbk of protecting element 62, as shown in Fig. 2(B). When the potential stepwise or abruptly changes in this way, the inductance L acts so that the potential of the wire near the gate of MOS transistor 63 oscillates as shown in Fig. 2(C). During the oscillation, the potential applied to the gate instantaneously exceeding the clamped voltage by the protecting element repeatedly appears. The excess potentials repeatedly cause stress in the gate oxide film, finally resulting in gate breakdown.

Document EP-A-0 280 236 is an earlier European application forming part of the state of the art as defined in Article 54(3) EPC and discloses an insulated gate semicustom integrated circuit which comprises an input protecting circuit in use with a MOS semiconductor device. In this integrated circuit, a first MOS transistor is provided in an input stage of the MOS semiconductor device, and a wire connects an input pad to the gate of the first MOS transistor.

A first protecting element consisting of two diodes connected in series is provided near the input pad, one end of the first protecting element being connected to the interconnecting wire, the other end being connected to a ground potential or a power source potential. A second protecting element consisting of two further MOS transistors is provided near the gate of the first MOS transistor, one end of said second protecting element being

connected to the interconnecting wire and the other end being connected to the ground potential or the power source potential.

Further prior art document Patent Abstracts of Japan 9 (298), E-361, describes an input circuit gate array in which a P channel MOS transistor and an N channel MOS transistor form a CMOS inverter. A first diode presents protecting action to a negative-directional static input voltage, and a second diode presents it to a positive static input voltage. Parasitic diodes between the substrate regions and the drains of the N-channel MOS transistor and the P-channel MOS transistor in the cell unused for input-output of the group of input-output cells are additionally connected as third and fourth protection diodes. The electrostatic strength of the protection diode can be improved without influences on the number of input-output cell or on the size of chips.

Prior art document Patent Abstracts of Japan 2 (104), (E-53) (5437) discloses an insulating gate type field effect transistor with a protective device corresponding to the first part of Claim 1. In this known circuit arrangement, a second MIS FET is placed at a location very close to a gate terminal of a first MIS FET between this gate terminal and a stray capacitance.

Finally, prior art document Patent Abstracts of Japan 2 (112), (E-57) (6074) describes a semiconductor device in which a gate protecting circuit includes two diodes which are connected between gate electrodes of MOS transistors and source electrodes thereof. Further, a thin film resistor for reducing current is provided near an input pad, and both ends of this thin film resistor are connected to an input wire.

It is an object of the present invention to provide an input protecting circuit in use with a MOS semiconductor device which has a satisfactorily high ESD breakdown voltage, and is available for present and coming MOS semiconductor devices whose gate oxide films are thin.

To achieve this object the present invention provides an input protecting circuit as specified in claim 1.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a circuit diagram showing a part of a conventional MOS semiconductor device with an input protecting circuit, which illustrates the interrelation of the protecting circuit and the semiconductor circuit;

Fig. 2 is a set of waveforms showing voltages in the circuit of Fig. 1;

Fig. 3 is a circuit diagram showing a first embodiment of an input protecting circuit according to the present invention;

Fig. 4 is a sectional view showing a first protecting element in the first embodiment;

Fig. 5 is a sectional view showing a second protecting element in the first embodiment;

Fig. 6 is a sectional view showing a first protecting element in the first embodiment;

Fig. 7 is a sectional view showing a first protecting element in the first embodiment;

Figs. 8 to 11 are circuit diagrams showing arrangements of 2nd to 5th embodiments of an input protecting circuit according to the present invention;

Fig. 12 is a sectional view showing an element used in each of the embodiments of Figs. 10 and 11;

Fig. 13 a plan view showing a pattern of a CMOS IC into which an input protecting circuit according to the present invention is applied;

Fig. 14 is a graph comparatively showing element destruction rates of the input protecting circuits of the above embodiments and of prior art; and

Figs. 15 to 16 are circuit diagrams showing arrangements of 6th and 7th embodiments of an input protecting circuit according to the present invention.

The present invention will be described in detail by using some specific embodiment with reference to the accompanying drawings.

Fig. 3 is a circuit diagram schematically showing an arrangement of a first embodiment of an input protecting circuit according to the present invention. In the figure, input pad 11, connected to an input pin (not shown) is connected to the gate of MOS transistor 13 in the input stage of a MOS semiconductor device, through interconnection wire 12 made of aluminum. A point of wire 12 close to input pad 11 is connected to the collector of npn bipolar transistor 14 serving as a first protecting element. The emitter of this transistor 14 is connected to ground potential Vss. Another point of wire 12 close to the gate of MOS transistor 13 is connected to the cathode of pn junction diode 15 serving as a second protecting element. The anode of this diode 15 is connected to ground potential Vss. Interconnection wire 12 contains inductance L, which is equivalently expressed in the illustration.

In the circuit thus arranged, if a stress due to the ESD is applied to the input pin of the IC coupled with input pad 11, most of the energy injected into input pad 11 flows toward each potential via bipolar transistor 14. This operation is similar to that of the conventional circuit shown in Fig. 1. As already referred to, it would be surmised that the breakdown of the gate insulating film in a conventional circuit is due to the inductance L of the interconnection wire. In other words, an ex-

tremely high potential stress, though the energy of it is small, applied to the gate oxide film of the MOS transistor in the input stage, results in dreakdown of the gate oxide film.

To cope with this, in the present embodiment, pn junction diode 15 serving as another protecting element is additionally provided near the gate of MOS transistor 13. This diode clamps the excess voltage applied to the gate of MOS transistor 13. As a result, the gate oxide film of the MOS transistor will never be breakdown even though it is very thin. The ESD breakdown voltage is thus improved.

Most of the energy injected into the input pad 11 is first shunted through transistor 14, and then the remaining energy, which is small but large in potential, reaches diode 15 through interconnection wire 12. Therefore, diode 15 as the second protecting element, which has a smaller chip area, can satisfactorily deal with such remaining energy. Further, there is no occurrence of latch-up in the internal circuit, even the provision of this diode 15.

Fig. 4 is a sectional view showing a part of the structure of a bipolar transistor 14, which is used in the embodiment as mentioned above. An IC chip uses p-type silicon substrate 21. A pair of n^+ type diffusion regions 23 and 24 are formed in the surface region of the substrate 21, with field oxide film 22 interposed therebetween. Diffusion region 23 is connected to wire 25, which is made of aluminum and connected to interconnection wire 12. This wire 25 extends over field oxide film 22. Another diffusion region 24 is connected to ground potential Vss by means of a wire (not shown). The element thus arranged is generally called an aluminum field transistor, and operates as a bipolar transistor in which n^+ diffusion regions 23 and 24 respectively are used for the collector and emitter, and p type substrate 21 for the base.

Fig. 5 is a sectional view showing in detail the structure of a pn junction diode 15, which is used as the second protecting element in the embodiment as mentioned above. Also in this structure, an IC chip uses p-type silicon substrate 21. An n^+ type diffusion region 26 is formed in the surface region of the substrate 21, which is enclosed by field oxide film 22. This diffusion region 26 is connected to wire 27, which is made of aluminum and connected to interconnection wire 12. The pn junction diode 15 is constructed such that n^+ type diffusion region 26 is used for the cathode, and p-type substrate 21 for the anode.

Figs. 6 and 7 are sectional views each showing a part of the structure of an element, which may be used for the first protecting element, and is used in the embodiment as mentioned above. In the instance of Fig. 6, a pair of n^+ type diffusion regions 28 and 29 are formed in the surface region of the substrate 21, with field oxide film 22 interposed therebetween. Diffusion region 28 is connected to interconnection wire 12. Another diffusion region 29 is connected to ground potential Vss. The element thus arranged operates as an npn bipolar transistor in which n^+ diffusion regions 28 and 29 respectively are used for the collector and emitter, and p type substrate 21 for the base.

In the element shown in Fig. 7, a pair of n^+ type diffusion regions 30 and 31 are formed in the surface region of the substrate 21, with gate electrode 32 bridging the surface region between those diffusion regions. Diffusion region 30 is connected to interconnection wire 12. Another diffusion region 31 and gate electrode 32 are connected to ground potential Vss. The element thus arranged operates as a npn bipolar transistor in which n^+ diffusion regions 30 and 31 are respectively used for the collector and emitter, and p type substrate 21 for the base.

Fig. 8 is a circuit diagram showing an arrangement of a second embodiment of an input protecting circuit according to the present invention. In the first embodiment, bipolar transistor 14 is used as the first protecting element which is located near the input pad 11 of interconnection wire 12. In this embodiment, the first protecting element is a pair of diodes, one is pn junction diode 16 inserted between wire 12 and positive power source potential Vcc, to clamp an incoming positive high voltage, and the other is a pn junction diode 17 inserted between wire 12 and ground potential Vss, to clamp an incoming negative high voltage. The second protecting element may be the same pn junction diode as that in the embodiment of Fig. 3.

Fig. 9 is a circuit diagram showing an arrangement of a third embodiment of an input protecting circuit according to the present invention. In this embodiment, the protecting element is a pair of transistors, one is npn transistor 14, and the other is pnp transistor 18 as an aluminum field transistor, of which the collector is connected to wire 12, and the emitter to positive power source potential Vcc. Also in this embodiment, the second protecting element may be the same pn junction diode as that in the embodiment of Fig. 3.

In the embodiment of Fig. 9, when a positive voltage due to ESD is applied to input pad 11, it is shunted through the collector-base path of transistor 18 or through the bipolar action of transistor 14. When the applied voltage is negative, it is shunted through the collector-base path of transistor 14 or through the bipolar action of transistor 18.

Fig. 10 is a circuit diagram showing an arrangement of a 4th embodiment of an input protecting circuit according to the present invention. While in each of the embodiments as mentioned above, pn junction diode 15 is used for the second protecting element connected to the point of wire

12 near the gate of MOS transistor 13, MOS transistor 19, whose drain and source are both connected to wire 12, is used for the second protecting element in this case. The gate of transistor 19 is connected to ground potential Vss. In the circuit of Fig. 10, the first protecting element may be the bipolar transistor as in the embodiment of Fig. 3.

In the case that the pn junction diode is used for the second protecting element, the clamp voltage is the breakdown voltage of the pn junction. In the case of the MOS transistor being used for the second protecting element, the clamp voltage is the surface breakdown voltage. The surface breakdown voltage of the MOS transistor is lower than the breakdown voltage of the pn junction. Therefore, when MOS transistor 19 is used for the second protecting element, voltage stress applied to the gate oxide film of MOS transistor 13 in the input stage is reduced.

Fig. 11 is a circuit diagram showing an arrangement of a 5th embodiment of an input protecting circuit according to the present invention. In the 5th embodiment, MOS transistor 19 is used for the second protecting element, as in the embodiment of Fig. 10. A difference between the 5th embodiment and the 4th embodiment of Fig. 10, is that the gate of MOS transistor 19 is connected to power source potential Vcc. With this connection, when a voltage stress is applied, the gate of this transistor 19 is equivalently grounded. The resultant surface breakdown voltage is lower than that in a normal operation mode. Thus, various types of elements may be used for the second protecting element.

Fig. 12 is a sectional view showing a structure of MOS transistor 19, which may be used in the embodiments of Figs. 10 and 11. As shown, a pair of n^+ diffusion regions 33 and 34, which is to serve as the source and drain, are formed in the surface region of p type substrate 21 as enclosed by field oxide film 22. These diffusion regions are connected together and to interconnection wire 12. Gate electrode 35 bridges the surface region of substrate 21 between n^+ diffusion regions 33 and 34. This gate electrode 35 is coupled with ground potential Vss or power source potential Vcc.

Fig. 13 is a plan view showing a partial pattern of a CMOS-IC in which the input protecting circuit shown in Fig. 3, in which only one input pad and its related circuit are illustrated in detail. Like reference symbols are used for designating like portions in Fig. 3, for simplicity. Input pad 11 made of aluminum is connected to interconnection wire 25 of bipolar transistor 14 as the first protecting element, via interconnection wire 41, which is made of aluminum and a part of wire 12. Bipolar transistor 14 is an aluminum field transistor having a sectional structure as shown in Fig. 4. Wire 25 is connected through a plurality of contact holes 42 respectively to a plurality of n^+ diffusion regions 23. A plurality of n^+ diffusion regions 24 are connected through a plurality of contact holes 43 to interconnection wire 44, which is made of aluminum and connected to ground potential Vss. Wire 25 is connected to interconnection wire 46 of the internal circuit, which is made of aluminum, by way of jumper wire 45 as a polysilicon layer, which allows wire 22 to pass above wire 44. This wire 46 is also contained in wire 12.

In n-type well region 47, circuit block 49 is formed while being enclosed by n^+ type guard ring region 48. In this circuit block 49, P-channel MOS transistor 50 is formed serving as the MOS transistor in the input stage. Reference numeral 51 designates a polysilicon wire to be the gate of the transistor 50, and 52 and 53, p^+ diffusion regions as the source and drain. Interconnection wire 46 is connected to polysilicon wire 51.

Reference numeral 54 designates a circuit block enclosed by p^+ type guard ring region 55. N channel MOS transistor 56 as the input stage MOS transistor is formed within this circuit block 54. Reference numeral 57 designates a polysilicon wire to be the gate of the transistor 56, and 58 and 59, p^+ diffusion regions as the source and drain. Interconnection wire 46 is connected to polysilicon wire 57. Within the circuit block 54, wire 46 is connected to n^+ diffusion region 60 to be the cathode of pn junction diode 15 as the second protecting element. Diode 15 is enclosed by guard ring region 55 in the circuit block 54 containing the input stage MOS transistor 56.

A chip area of the diffusion region 60 serving as the cathode of pn junction diode 15, may be very small, 10 μm, for example. Therefore, if this diode 15 is formed near MOS transistor 56, it causes little causes latch-up phenomenon in the internal circuit.

Fig. 14 shows a graph comparatively showing destruction rates (%) of the elements when a high voltage is applied to the input pad in each of the above-mentioned embodiments, and in the conventional input protecting circuit. In the graph, curve "a" shows a variation of destruction rate of the conventional protecting circuit shown in Fig. 1, which is constructed as follows: a polysilicon resistor of 200-ohm and 20 μm in width is inserted in the interconnection wire, the inductance L of the wire is 20 nH, the protecting element is an aluminum field transistor of which the channel width is 500 μm and the interval between the diffusion regions is 24 μm. Destruction rate variation curve "b" is obtained when the protecting element 52 in the conventional protecting circuit is an aluminum field transistor of which the channel width is 500 μm, and the interval between the diffusion regions

is 2.4 μm. In this case, the portion that is is destroyed is the gate oxide film of the MOS transistor in the input stage. The breakdown voltage is ±1400 V, and low next to curve "a". Destruction rate variation curve "c" is obtained when the protecting element 52 in the conventional protecting circuit uses an aluminum field transistor of which the channel width is 300 μm, and the interval between the diffusion regions is 2.4 μm, and another aluminum field transistor of which the channel width is 100 μm, and the interval between the diffusion regions is 2.4 μm, and a further diffusion resistor laid between these transistors. Also in this case, the portion that is destroyed is the gate oxide film of the MOS transistor in the input stage. The breakdown voltage is ±2000 V, and low next to curve "b".

Curve "c" shows a destruction rate variation of an input protecting circuit according to the present invention in which the second protecting element is the MOS transistor 19 shown in Fig. 11. The channel width and the distance between the diffusion regions of the bipolar transistor 14 as the first protecting element are respectively 500 μm and 2.4 μm, the same as those in the cases of curves "a" and "b". It was confirmed that the breakdown voltage is ±3000 V or more. Thus, the ESD breakdown voltage is remarkably improved.

Fig. 15 is a circuit diagram showing a 6th embodiment of an input protecting circuit according to the present invention. In the present embodiment, resistor R of 200-ohm or more, for example, is inserted between bipolar transistor 14 as the first protecting element and pn junction diode 15 as the second protecting element. This resistor R and a parasitic capacitor C in the vicinity of the gate of the MOS transistor 13 in the input stage, cooperate to form a CR filter. This filter functions to absorb the potential oscillation in wire 12.

Fig. 16 is a circuit diagram showing a 7th embodiment of an input protecting circuit according to the present invention. In this embodiment, resistor R of 200-ohm or more, for example, is inserted between input pad 11 and bipolar transistor 14 as the first protecting element. The resistor R and a parasitic capacitor C in the vicinity of the gate of the MOS transistor 13 in the input stage, also cooperate to form a CR filter. This filter functions to absorb the potential oscillation in wire 12.

As described above, in the input protecting circuit according to the present invention, the protecting element is additionally provided near the gate of the input stage MOS transistor. This feature attains ±300 V or more of the ESD breakdown voltage. This figure is much higher than that of the conventional protecting circuit.

Further, the effect by the present invention may be obtained even if the chip area required for the protecting element near the gate of the input stage MOS transistor is very small. Therefore, there is no degradation of the latch-up performance.

Claims

1. An input protecting circuit for protecting the gate of a MOS semiconductor device against over voltages comprising:

   an input pad (11);

   a MOS transistor (13, 50, 56) provided in the input stage of the MOS semiconductor device;

   a wire (12, 41, 25, 45, 46) for interconnecting said input pad (11) to the gate of said MOS transistor (13, 50, 56) in said input stage;

   a first protecting element (14, 16, 17, 18) for clamping an excess voltage applied to said input pad (11) provided near said input pad (11), one end of said first protecting element (14, 16, 17, 18) being connected to said interconnecting wire (12, 41, 25, 45, 46), and another end of said first protecting element (14, 16, 17, 18) being connected to a ground potential or a power source potential; and

   a second protecting element (15, 19) for clamping an excess voltage at the gate of said MOS transistor (13) provided near the gate of said MOS transistor (13, 50, 58), one end of said second protecting element (15, 19) being connected to said interconnecting wire (12, 41, 25, 45, 46), and another end of said second protecting element (15, 19) being connected to the ground potential or the power source potential;

   characterized in that said second protecting element is formed in a circuit block (54) which is enclosed by a guard ring region (55) and contains said MOS transistor (56) of the input stage formed therein.

2. An input protecting circuit according to claim 1, characterized in that said first protecting element is one bipolar transistor (14).

3. An input protecting circuit according to claim 1, characterized in that said first protecting element includes a pair of diodes (16, 17).

4. An input protecting circuit according to claim 1, characterized in that said first protecting element includes a pair of bipolar transistors (14, 18).

5. An input protecting circuit according to claim 1, characterized in that said second protecting element includes a diode (15).

is 2.4 μm. In this case, the portion that is is destroyed is the gate oxide film of the MOS transistor in the input stage. The breakdown voltage is ±1400 V, and low next to curve "a". Destruction ate variation curve "c" is obtained when the protecting element 52 in the conventional protecting circuit uses an aluminum field transistor of which the channel width is 300 μm, and the interval between the diffusion regions is 2.4 μm, and another aluminum field transistor of which the channel width is 100 μm, and the interval between the diffusion regions is 2.4 μm, and a further diffusion resistor laid between these transistors. Also in this case, the portion that is destroyed is the gate oxide film of the MOS transistor in the input stage. The breakdown voltage is ±2000 V, and low next to curve "b".

Curve "c" shows a destruction rate variation of an input protecting circuit according to the present invention in which the second protecting element is the MOS transistor 19 shown in Fig. 11. The channel width and the distance between the diffusion regions of the bipolar transistor 14 as the first protecting element are respectively 500 μm and 2.4 μm, the same as those in the cases of curves "a" and "b". It was confirmed that the breakdown voltage is ±3000 V or more. Thus, the ESD breakdown voltage is remarkably improved.

Fig. 15 is a circuit diagram showing a 6th embodiment of an input protecting circuit according to the present invention. In the present embodiment, resistor R of 200-ohm or more, for example, is inserted between bipolar transistor 14 as the first protecting element and pn junction diode 15 as the second protecting element. This resistor R and a parasitic capacitor C in the vicinity of the gate of the MOS transistor 13 in the input stage, cooperate to form a CR filter. This filter functions to absorb the potential oscillation in wire 12.

Fig. 16 is a circuit diagram showing a 7th embodiment of an input protecting circuit according to the present invention. In this embodiment, resistor R of 200-ohm or more, for example, is inserted between input pad 11 and bipolar transistor 14 as the first protecting element. The resistor R and a parasitic capacitor C in the vicinity of the gate of the MOS transistor 13 in the input stage, also cooperate to form a CR filter. This filter functions to absorb the potential oscillation in wire 12.

As described above, in the input protecting circuit according to the present invention, the protecting element is additionally provided near the gate of the input stage MOS transistor. This feature attains ±300 V or more of the ESD breakdown voltage. This figure is much higher than that of the conventional protecting circuit.

Further, the effect by the present invention may be obtained even if the chip area required for the protecting element near the gate of the input stage MOS transistor is very small. Therefore, there is no degradation of the latch-up performance.

Claims

1. An input protecting circuit for protecting the gate of a MOS semiconductor device against over voltages comprising:

   an input pad (11);

   a MOS transistor (13, 50, 56) provided in the input stage of the MOS semiconductor device;

   a wire (12, 41, 25, 45, 46) for interconnecting said input pad (11) to the gate of said MOS transistor (13, 50, 56) in said input stage;

   a first protecting element (14, 16, 17, 18) for clamping an excess voltage applied to said input pad (11) provided near said input pad (11), one end of said first protecting element (14, 16, 17, 18) being connected to said interconnecting wire (12, 41, 25, 45, 46), and another end of said first protecting element (14, 16, 17, 18) being connected to a ground potential or a power source potential; and

   a second protecting element (15, 19) for clamping an excess voltage at the gate of said MOS transistor (13) provided near the gate of said MOS transistor (13, 50, 58), one end of said second protecting element (15, 19) being connected to said interconnecting wire (12, 41, 25, 45, 46), and another end of said second protecting element (15, 19) being connected to the ground potential or the power source potential;

   characterized in that said second protecting element is formed in a circuit block (54) which is enclosed by a guard ring region (55) and contains said MOS transistor (56) of the input stage formed therein.

2. An input protecting circuit according to claim 1, characterized in that said first protecting element is one bipolar transistor (14).

3. An input protecting circuit according to claim 1, characterized in that said first protecting element includes a pair of diodes (16, 17).

4. An input protecting circuit according to claim 1, characterized in that said first protecting element includes a pair of bipolar transistors (14, 18).

5. An input protecting circuit according to claim 1, characterized in that said second protecting element includes a diode (15).

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6. An input protecting circuit according to claim 1, characterized in that said second protecting element includes a MOS transistor (19) of which the source and drain are connected to said wire (12).

7. An input protecting circuit according to claim 6, characterized in that the gate of said MOS transistor (19) is grounded.

8. An input protecting circuit according to claim 6, characterized in that the gate of said MOS transistor (19) is connected to a power source potential.

9. An input protecting circuit according to claim 1, characterized in that a resistor (R) is inserted in series with said wire (12).

Patentansprüche

1. Eingangsschutzschaltung zum Schutz des Gate bzw. der Steuerelektrode einer MOS-Halbleitervorrichtung gegen Überspannungen, die folgendes umfaßt:
ein Eingangskissen (11);
einen in der Eingangsstufe der MOS-Halbleitervorrichtung vorgesehenen MOS-Transistor (13, 50, 56);
einen Draht (12, 41, 25, 45, 46) zur Verbindung des Eingangskissens (11) mit dem Gate des MOS-Transistors (13, 50, 56) in der Eingangsstufe;
ein erstes Schutzelement (14, 16, 17, 18) zum Festhalten einer an das Eingangskissen (11) angelegten Überspannung, welches in der Nähe des Eingangskissens (11) so angeordnet ist, daß ein Ende des ersten Schutzelements (14, 16, 17, 18) an den Verbindungsdraht (12, 41, 25, 45, 46) und ein anderes Ende des ersten Schutzelements (14, 16, 17, 18) an ein Massepotential oder ein Spannungsquellenpotential angeschlossen ist; und
ein zweites Schutzelement (15, 19) zum Festhalten einer an das Gate des MOS-Transistors (13) angelegten Überspannung, welches in der Nähe des MOS-Transistors (13, 50, 58) so angeordnet ist, daß ein Ende des zweiten Schutzelements (15, 19) an den Verbindungsdraht (12, 41, 25, 45, 46) und ein anderes Ende des zweiten Schutzelements (15, 19) an das Massepotential oder das Spannungsquellenpotential angeschlossen ist;
dadurch gekennzeichnet, daß
das zweite Schutzelement in einem Schaltungsblock (54) angeordnet ist, welcher von einer Schutzringzone umgeben ist und den darin ausgebildeten MOS-Transistor (56) der Eingangsstufe enthält.

2. Eingangsschutzschaltung gemäß Anspruch 1, dadurch gekennzeichnet, daß das erste Schutzelement ein bipolarer Transistor (14) ist.

3. Eingangsschutzschaltung gemäß Anspruch 1, dadurch gekennzeichnet, daß das erste Schutzelement ein Diodenpaar (16, 17) umfaßt.

4. Eingangsschutzschaltung gemäß Anspruch 1, dadurch gekennzeichnet, daß das erste Schutzelement ein Paar bipolarer Transistoren (14, 18) umfaßt.

5. Eingangsschutzschaltung gemäß Anspruch 1, dadurch gekennzeichnet, daß das zweite Schutzelement eine Diode (15) enthält.

6. Eingangsschutzschaltung gemäß Anspruch 1, dadurch gekennzeichnet, daß das zweite Schutzelement einen MOS-Transistor (19) enthält, dessen Source und Drain mit dem Draht (12) verbunden sind.

7. Eingangsschutzschaltung gemäß Anspruch 6, dadurch gekennzeichnet, daß das Gate des MOS-Transistors (19) geerdet ist.

8. Eingangsschutzschaltung gemäß Anspruch 6, dadurch gekennzeichnet, daß das Gate des MOS-Transistors (19) an ein Spannungsquellenpotential angeschlossen ist.

9. Eingangsschutzschaltung gemäß Anspruch 1, dadurch gekennzeichnet, daß ein Widerstand (R) in Reihe in den Draht (12) eingeschaltet ist.

Revendications

1. Circuit de protection d'entrée pour protéger la grille d'un dispositif semi-conducteur MOS contre des surtensions comprenant :
une plage d'entrée (11);
un transistor MOS (13, 50, 56) placé dans l'étage d'entrée du dispositif semi-conducteur MOS;
un fil (12, 41, 25, 45, 46) pour interconnecter ladite plage d'entrée (11) à la grille dudit transistor MOS (13, 50, 56) dudit étage d'entrée;
un premier élément de protection (14, 16, 17, 18) pour bloquer une tension en excès appliquée à ladite plage d'entrée (11), placée près de ladite plage d'entrée (11), une extrémité dudit premier élément de protection (14, 16, 17, 18) étant reliée audit fil d'interconnexion (12, 41, 25, 45, 46), et une autre extrémité

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dudit premier élément de protection (14, 16, 17, 18) étant reliée à un potentiel de la masse ou à un potentiel d'alimentation; et

un second élément de protection (15, 19) pour bloquer une tension en excès sur la grille dudit transistor MOS (13) placé près de la grille dudit transistor MOS (13, 50, 58), une extrémité dudit second élément de protection (15, 19) étant reliée audit fil d'interconnexion (12, 41, 25, 45, 46), et l'autre extrémité dudit second élément de protection (15, 19) étant reliée au potentiel de la masse ou au potentiel d'alimentation;

caractérisé en ce que ledit second élément de protection est formé dans un bloc circuit (54) qui est enfermé dans une zone ayant un anneau de garde (55) et qui contient ledit transistor MOS (56) de l'étage d'entrée formé dans celui-ci.

2. Circuit de protection d'entrée selon la revendication 1, caractérisé en ce que ledit premier élément de protection est un transistor bipolaire (14).

3. Circuit de protection d'entrée selon la revendication 1, caractérisé en ce que ledit premier élément de protection comprend une paire de diodes (16, 17).

4. Circuit de protection d'entrée selon la revendication 1, caractérisé en ce que ledit premier élément de protection comprend une paire de transistors bipolaires (14, 18).

5. Circuit de protection d'entrée selon la revendication 1, caractérisé en ce que ledit second élément de protection comprend une diode (15).

6. Circuit de protection d'entrée selon la revendication 1, caractérisé en ce que ledit second élément de protection comprend un transistor MOS (19) dont la source et le drain sont reliés audit fil (12).

7. Circuit de protection d'entrée selon la revendication 6, caractérisé en ce que la grille dudit transistor MOS (19) est reliée à la masse.

8. Circuit de protection d'entrée selon la revendication 6, caractérisé en ce que la grille dudit transistor MOS (19) est reliée à un potentiel d'alimentation.

9. Circuit de protection d'entrée selon la revendication 1, caractérisé en ce qu'une résistance (R) est insérée en série avec ledit fil (12).

* C L M S *