CIRCUIT DELAY SELF-MEASUREMENT METHOD, DEVICE AND SYSTEM

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a national phase application of International Application No. PCT/CN2017/100212 filed on September 1, 2017, which claims priority to Chinese patent applications Serial No. 201610977256.7 filed on November 7, 2016 and Serial No. 201610978228.7 filed on November 7, 2016, the entire content of which is incorporated herein by reference.

FIELD

The present disclosure relates to the field of circuit delay detection, and more particularly, to a circuit delay self-measurement method, device and system.

BACKGROUND

At present, the near field communication method is widely adopted in various fields (e.g. payment), and the communication between device A and device B that uses the near field communication method (e.g. RFID, NFC, infrared or Bluetooth) may have safety hazards. For example, as illustrated in Fig 1, if the data channel established by device A and device B is intervened by a third party, the data during the entire communication process arrives at the other device through a third party without the knowledge of both rightful parties, eventually resulting in data leakage.

At present, the following method can be used to determine if the communication data between device A and device B is hijacked. After device A sends a command signal to device B, device A waits to receive a response signal from device B, the waiting time period refers to a difference between the time point when device A sends the command signal and the time point when the response signal from device B is received, and the communication data between device A and device B is considered not to be hijacked by the third party as long as the waiting time period is within a preset time period.

However, the response signal received by device A from device B is an analog signal, that is, the analog signal obtained by device A is a modulated response signal based on the response data. After receiving the response signal, device A, as illustrated in Fig. 2, first demodulates the signal obtained by the receiving circuit and generates the response data, but the low-pass filter in the receiving circuit for removing high-frequency signal components causes circuit delay, which is un-ignorable for the waiting time period. Since the response data obtained by device A is processed by the main control chip in device A, device A can obtain an accurate time point when the response data is received by the main control chip. In view of the circuit delay in the receiving