ABSTRACT

A semiconductor device includes an active pattern provided on a substrate, a source/drain pattern provided on the active pattern, a channel pattern configured to be connected to the source/drain pattern, a gate electrode configured to be extended in a first direction and to cross the channel pattern, and a first spacer provided on a side surface of the gate electrode. The first spacer includes a fence portion provided on a side surface of the active pattern and below the source/drain pattern. The source/drain pattern includes a body portion and a neck portion between the body portion and the active pattern. The body portion includes a crystalline surface configured to be slantingly extended from the neck portion. The crystalline surface is configured to be spaced apart from an uppermost portion of the fence portion.

FIG. 6A