Description

This invention relates generally to circuits for processing video signals in digital format, and particularly to a digital signal correlation indicator. The invention may be applied to a system which utilizes such a correlation indicator to effect reduction of picture disturbances of the so-called "hanging dot" type that may be associated with employment of a comb filter for separation of the luminance and chrominance components of composite video signals in a color television receiver.

The success of the separation function performed by typical forms of comb filters in color television receivers is dependent upon the existence of redundancy of picture information in adjacent regions of successive scan lines. For picture areas where a transition in the direction of field scanning (hereinafter referred to as a vertical transition) occurs, the difference in picture information in adjacent regions of sucessive scan lines can result in imperfect performance of the separation function, with one consequence being the appearance of a chrominance component in the luminance signal output of the comb filter. If not removed, the interloping chrominance component will be reproduced as "hanging dots", i.e., as an undesirable array of dots extending across the region of the vertical transition in the displayed picture.

U.S. Patent No. US-A-4,241,363 illustrates one prior art approach to the detection of "hanging dot" occurrences, wherein the indication of such an occurrence is developed by a signal multiplier responsive to chrominance signal and high frequency luminance signal outputs of comb filter apparatus.

As recognized in cofiled EP-A-201,227, the signal multiplier apparatus of the aforesaid patent serves as a correlation indicator, relying upon a recognition of correlation between signal components in the respective outputs of the comb filter apparatus to identify "hanging dot" occurrences. For certain types of vertical transitions, such as transitions between colored and uncolored areas, the disclosed apparatus of said patent can provide a reliable identification of "hanging dot" occurrences.

However, as additionally recognized in the aforesaid copending patent application, the disclosed apparatus of the aforesaid patent fails in its role of identification of "hanging dot" occurrences in instances of certain vertical transitions between areas of different colors. For example, for certain transitions of this type, the interloping chrominance component appearing in the high frequency luminance signal output of the comb filter apparatus bears a substantially quadrature phase relationship to the chrominance component appearing in the chrominance signal output of the comb filter apparatus. In such an instance, the signal multiplier of the aforesaid patent fails to develop an indication of a "hanging dot" occurrence, and, as a result, an undesired dot array will be subject to display in the vertical transition region.

Pursuant to the principles of the invention disclosed in the aforesaid copending patent application, the identification of "hanging dot" occurrences is desirably carried out by apparatus employing a pair of correlation indicators: (a) one correlation indicator being responsive to inputs comprising chrominance signal and high frequency luminance outputs derived without difference in delay from the comb filter apparatus, and (b) another correlation indicator being responsive to inputs comprising chrominance signal and high frequency luminance outputs derived with a relative delay difference from the comb filter apparatus, the delay difference substantially corresponding to one-quarter of the length of a period at the nominal subcarrier frequency associated with the chrominance component. Through reliance upon the development of an output by either (or both) of the correlation indicator pair to identify "hanging dot" occurrences, a more reliable "hanging dot" identifier is obtained, which avoids the quadrature relationship failure of the prior art apparatus described above. During periods of "hanging dot" identification, the luminance signal output of the comb filter is subjected to appropriate modification (e.g., high frequency component deletion) to preclude "hanging dot" display.

In the aforesaid copending patent application, each correlation indicator is illustrated as comprising a signal multiplier, a low pass filter and a voltage comparator. The signal multiplier functions to multiply the high frequency components of the respective comb filter outputs. The products of multiplication developed by the signal multiplier are filtered by the low pass filter to develop a filtered multiplier output signal, which is subject to comparison with a threshold voltage in the voltage comparator. A hanging dot occurrence indication is provided at the output terminal of the voltage comparator whenever the level of the filtered multiplier output signal exceeds the threshold voltage.

The above-described form of correlation indicator, employing a signal multiplier, is readily implemented in receivers of the analog signal processing type. Such form of correlation indicator may also be implemented in receivers of the digital signal processing type, using well known techniques for digital signal multiplication and filtering.

The present invention is concerned with novel structures for implementing the function of a correlation indicator in a digital signal processing system. A hanging dot reduction system embodying the principles of the invention of the aforesaid

copending patent application may be realized with use of the present invention with significant savings in expense and complexity relative to that required if conventional digital signal multipliers were to be employed therein.

The present invention provides a digital correlation indicator, in a color television receiver employing a system for processing composite color television signals appearing in a digital format, said composite color television signals being inclusive of a luminance signal component and a chrominance signal component comprising sidebands developed by the modulation of a color subcarrier of a frequency f_{sc}; said system including comb filter apparatus for developing a first comb filtered signal representing composite signals subjected to a first comb filter characteristic exhibiting a first plurality of response peaks and producing a first digital signal of "m" bits representative of a first bipolar signal component comprising high frequency components of said first comb filtered signal, and a second comb filtered signal representing composite signals subjected to a second comb filter characteristic exhibiting a second plurality of response peaks interleaved with the response peaks of said first plurality, and providing a second digital signal of "m" bits representative of a second bipolar component signal comprising high frequency components of said second comb filtered signal; said digital correlation indicator being characterized by: first logic circuit means responsive to only the "k" mot significant bits of said first digital signal, where "k" is less than "m", for outputting a "l" whenever said first digital signal is representative of an excursion of said first bipolar signal component, in either a positive or a negative direction, which equals or exceeds a threshold determined by the "k'th" most significant bit of said first digital signal; second logic circuit means responsive to only the "j" most significant bits of said second digital signal, where "j" is less than or equal to "m", for outputting a "l" whenever said second digital signal is representative of an excursion of said second bipolar signal component, in either a positive or a negative direction, which equals or exceeds a threshold determined by the "j'th" most significant bit of said second digital signal; an "and" gate having two inputs, one responsive to the output of said first logic circuit means and the other responsive to the output of said second logic circuit means and correlation indication signal developing means responsive to the output of said "and" gate, comprising means for recognizing the existence of a predetermined sequence of logic levels in a train of output pulses developed by said "and" gate.

Pursuant to the present invention, an indicator of correlation between respective digital signals, of "m" bits each, representative of first and second bipolar signal components comprises: first logic circuit means, responsive to only the "k" most significant bits of said first digital signal, where "k" is less than "m"; second logic circuit means, responsive to only the "j" most signficant bits of said second digital signal, where "j" is less than or equal to "m"; an "and" gate having two inputs, one responsive to the output of said first logic circuit means and the other responsive to the output of said second logic circuit means; and correlation indication signal developing means responsive to the output of said "and" gate.

In an embodiment of the invention the first logic circuit means functions to output a "l" whenever the first digital signal is representative of an excursion of the first bipolar signal component, in either a positive or negative direction, which equals or exceeds a threshold determined by the "k'th" most significant bit of said first digital signal. In the embodiment, the second logic circuit means functions to output a "l" whenever the second digital signal is representative of an excursion of the second bipolar signal component, in either a positive or negative direction, which equals or exceeds a threshold determined by the "j'th" most significant bit of said second digital signal. Illustratively, the first logic circuit means comprises a first absolute value circuit for developing a sign-independent version of said first digital signal, a first "or" gate having "k" inputs, and means for applying each of the "k" most significant bits of the output of said first absolute value circuit to a respectively different one of the inputs of said first "or" gate; while the second logic circuit means comprises a second absolute value circuit for developing a sign-independent version of said second digital signal, a second "or" gate having "j" inputs, and means for applying each of the "j" most significant bits of the output of said second absolute value circuit to a respectively different one of the inputs of said second "or" gate.

In accordance with an illustrative embodiment of the present invention, the correlation indication signal developing means of the above-described digital correlation indicator comprises: signal delay means having a plurality of successive signal takeoff points, with the amount of delay between successive ones of said takeoff points being the same, and with the input of said delay means being responsive to the output of the aforesaid "and" gate; a plurality of signal paths, each connected to a respectively different one of said signal takeoff points; a second"and" gate having a plurality of inputs equal in number to said plurality of signal paths, with each of said signal paths terminating at a respectively different one of said plurality of inputs of said second "and" gate; and a control signal former responsive to the output of said sec-

ond "and" circuit.

Illustratively, the control signal former of the aforementioned combination comprises: a succession of two-input "or" gates and a plurality of delay devices (each imparting the same amount of delay), (a) with one input of each "or" gate of said succession rendered responsive to the output of the aforementioned second "and" gate, (b) with the output of each of said succession of "or" gates, with the exception of the last of said succession, being coupled via a respective one of said plurality of delay devices to the other input of the next succeeding one of said succession of "or" gates; and (c) with the control signal appearing at the output of the last of said succession of "or" gates.

In a hanging dot reduction system employing the above-described correlation indication structure according to the invention, the first bipolar signal component, represented by said first digital signal, comprises high frequency components of a first comb filtered signal representing composite video signals subjected to a first comb filter characteristic exhibiting a plurality of response peaks at even multiples of half the line frequency of said composite signals; while the second bipolar signal component, represented by said second digital signal, comprises high frequency components of a second comb filtered signal representing composite video signals subjected to a second comb filter characteristic exhibiting a plurality of response peaks at odd multiples of half said line frequency. Means are provided for subjecting said first comb filtered signal to high frequency component removal in response to development of said control signal. Desirably, the hanging dot reduction system may additionally include: a third "and" gate having two inputs; a pair of additional signal paths respectively linking the outputs of said first and second "or" gates with the respective inputs of said third "and" gate, with said additional signal paths exhibiting a difference in delay corresponding to 90° at the color subcarrier frequency (f_{sc}) of the chrominance component of the composite video signals; and an additional "or" gate for delivering signals to the input of the aforementioned delay means, said additional "or" gate having a first input coupled to the output of the first-named "and" gate, and a second input coupled to the output of said third "and" gate.

In an illustrative implementation of the above-described hanging dot reduction system in a receiver employing a 4 f_{sc} clocking rate for its digital signal processing circuits, each of the aforementioned plurality of delay devices imparts a delay equal to a period at 4 f_{sc}, while the amount of delay between successive ones of said signal takeoff points corresponds to twice a period at 4 f_{sc}. Desirably, the other input of the first of said succession of two-input "or" gates is effectively inactive, while the sum of the delays imparted by said plurality of delay devices exceeds the amount of delay between the first and last of said plurality of successive signal takeoff points.

In the accompanying drawing, the sole figure illustrates a portion of a color television receiver incorporating a hanging dot reduction system utilizing digital signal correlation indication pursuant to an illustrative embodiment of the present invention.

In the illustrated color TV receiver apparatus, composite video signals, inclusive of a luminance component, and of a chrominance component comprising sidebands developed by the modulation of a color subcarrier f_{sc}, appear (in an 8-bit digital format) at a composite video signal input terminal CV and are supplied to the input of a 1-H delay line 11. The digital signal processing circuits (including the aforesaid delay line 11) of the illustrated color TV receiver are subject to clocking at a $4f_{sc}$ rate, with the clocking signals derived from a source (not illustrated) desirably synchronized by the color burst component of the received signals in a conventional manner. The delayed signal output of delay line 11 is additively combined with signals derived directly from terminal CV in signal combiner 13, and also is subtractively combined with signals derived directly from terminal CV in signal combiner 15.

The combination of delay line 11 and the subtractive signal combiner 15 forms a first comb filter having a frequency response characteristic exhibiting a succession of response peaks at odd multiples of half the line frequency of the composite signals (interspersed with response minima at even multiples of half the line frequency). High frequency components of the output of the first comb filter, falling within the band of frequencies occupied by the chrominance component, are selectively passed by a bandpass filter 17 coupled to the output of signal combiner 15 to form a combed chrominance signal suitable for delivery to the receiver's chrominance channel.

The combination of delay line 11 and the additive signal combiner 13 forms a second comb filter having a frequency response characteristic exhibiting a succession of response peaks at even multiples of half the line frequency (interspersed with response minima at odd multiples of half the line frequency). The output of signal combiner 13 consitutes a combed luminance signal, substantially freed of chrominance component accompaniment, but also undesirably stripped of low frequency components representative of vertical detail. Restoration of vertical detail information to the combed luminance signal is effected by an additional signal combiner 21, which additively combines the output of signal combiner 13 with the

output of a vertical detail filter 19. Vertical detail filter 19 is responsive to the output of the first comb filter, accepting the output of signal combiner 15 and selectively passing low frequency components thereof falling within a frequency band below that occupied by the chrominance component.

The output of signal combiner 21 is normally employed as the signal input to the receiver's luminance channel. For this purpose, the output of signal combiner 21 is coupled via a signal delay device 23 (with a compensating function to be subsequently explained) to a first signal input terminal (0) of a multiplexer 25. In a first of the two operating states of multiplexer 25, which state exists when a "zero" appears at the multiplexer control terminal CO, the signal delivered to this first signal input terminal appears at the output of multiplexer 25 for delivery to the luminance channel. In the second of the operating states of multiplexer 25, which exists when a "one" appears at control terminal CO, the signal appearing at a second signal input terminal (1) of multiplexer 25 is instead delivered to the luminance channel.

In the second operating state of multiplexer 25, the signal delivered to the receiver's luminance channel corresponds to the output of signal combiner 21, subject, however, to removal of its high frequency components. For production of such a reduced-bandwidth signal, the illustrated apparatus includes a subtractive signal combiner 31, responsive to the output of signal combiner 21 (supplied therefrom via delay device 23) and to the output of a bandpass filter 27 (supplied therefrom via an additional delay device 29). Bandpass filter 27 is responsive to the output of signal combiner 21, and illustratively has a passband substantially identical with that of bandpass filter 17. The delay imparted to signals by delay device 23 exceeds the delay imparted by delay device 29 by an amount comparable to the signal delay introduced by bandpass filter 27, so as to align the timing of the high frequency components of the signal inputs to combiner 31 in a manner ensuring high frequency component cancellation therein.

Control of the switching of multiplexer 25 between its respective operating states is effected by a multiplexer control signal delivered to the control terminal CO by apparatus now to be described.

The illustrated control apparatus includes a first "or" gate 33 for deriving a one-bit stream of information concerning the high frequency components of the combed luminance signal passed by bandpass filter 27, and a second "or" gate 35 for deriving a one-bit stream of information concerning the combed chrominance component passed by bandpass filter 17. An absolute value circuit 28 operates upon the output of bandpass filter 27 to derive a signal representative of the absolute value (i.e., with sign independence) of the combed luminance high frequency components for application to "or" gate 33, while an absolute value circuit 18 operates upon the output of bandpass filter 17 to derive a signal representative of the absolute value (i.e., with sign independence) of the combed chrominance components for application to "or" gate 35. In a system where the outputs of the respective absolute value circuits comprise signals having "m" bits, "or" gate 33 desirably has "k" inputs, where "k" is less than "m", and "or" gate 35 desirably has "j" inputs, where "j" is less than, or equal to, "m". A plurality of signal paths of a number equal to the number of inputs for "or" gate 33 supply each of the "k" most signficant bits of the output of absolute value circuit 28 to a respectively different one of the inputs of "or" gate 33, while a plurality of signal paths of a number equal to the number of inputs for "or" gate 35 supply each of the "j" most significant bits of the output of absolute value circuit 18 to a respectively different one of the inputs of "or" gate 35.

In the system illustrated in the drawing, where m=7, an illustrative choice of 6 for both "j" and "k" is shown. Pursuant to this illustrative choice, "or" gate 33 will output a "1" whenever the output of absolute value circuit 28 reaches or exceeds a threshold level represented by the sixth most significant bit; in instances of lower signal levels, or signal absence, the presence of "0" at all of the inputs will result in a "0" output for "or" gate 33. Similarly, "or" gate 35 will output a "1" only when the output of absolute value circuit 18 reaches or exceeds the same threshold level.

The illustrated control apparatus additionally includes a pair of two-input "and" gates 37 and 39. The outputs of gates 33 and 35 are supplied directly to the inputs of "and" gate 37. While "and" gate 39 is also responsive to the outputs of gates 33 and 35, the signal delivery paths therebetween exhibit a difference in delay due to the interposition of a delay device 38 in the path from gate 35 to an input of "and" gate 39. Delay device 38 imparts a delay corresponding to 90° at the color subcarrier frequency f_{sc} (i.e., corresponding to a period at the clocking frequency of $4f_{sc}$). The respective outputs of "and" gates 37 and 39 are delivered to the inputs of a two-input "or" gate 40. Gate 40 develops an output of "1" when: (1) gate 37 outputs a "1" in response to coincident development of "1" outputs by "or" gates 33 and 35, and/or (2) gate 39 outputs a "1" in response to coincidence between the delayed appearance of a "1" at the output of delay device 38, and development of a "1" output by "or" gate 33.

The output of "or" gate 40 is applied to a sequence recognizing apparatus 50, comprising delay means formed by a plurality of similar delay

devices (51,52,53,54,55,56) in cascade (each imparting a delay corresponding to twice a period at the clocking frequency of 4 f_{sc}), and a seven-input "and" gate 58. Respective signal paths link each input of gate 58 to a different one of seven signal takeoff points associated with the delay means, with the first of the signal takeoff points located at the input of the first delay device 51 (to which the output of "or" gate 40 is applied), and with the remainder located at the respective outputs of the successive delay devices (51,52,53,54,55 and 56). Gate 58 outputs a "1" (at terminal CI) as an indication of an occurrence of hanging dots only upon the simultaneous appearance of a "1" at each of the seven successive signal takeoff points.

Control signal forming apparatus 60, responsive to the signal appearing at terminal CI comprises a plurality of like signal delay devices ("n" in number: D-1,D2,D-3...D-n), each imparting a delay corresponding to a period at the clocking frequency of 4 f_{sc}, and a succession of two-input "or" gates ("n + 1" in number: O-1,O-2,O-3....O-n, O-n + 1). The signal appearing at terminal CI is supplied to one input of each of the succession of "or" gates (O-1,O-2, etc.). The output of each of the succession of "or" gates (O-1,O-2, etc.), with the exception of the last (O-n + 1) of said succession, is coupled via a respective one of said plurality of delay devices (D-1, D-2, etc.) to the other input of the next succeeding one of said succession. The other input of the first (O-1) of said succession of "or" gates is maintained at a "0" level. The output of the last (O-n + 1) of said succession of "or" gates is delivered to terminal CO as the multiplexer control signal. Illustratively, the number "n" is selected so that the sum of the delays provided by the plurality of delay devices (D-1,D-2,D-3....D-n) of control signal former 60 exceeds the delay provided between the first and last signal takeoff points of the sequence recognition apparatus 50, so as to provide a desirable control signal stretching effect when hanging dot occurrences are recognized.

The magnitude of the delay imparted by the previously mentioned delay device 23 is selected to substantially match the delay associated with control signal development so as to ensure appropriate timing of the switching of operating states of multiplexer 25 relative to the timing of the hanging dot appearances in the signals being delivered to multiplexer 25. Where the aforementioned control signal stretching is employed, the delay amount for delay device 23 desirably is particularly selected to symmetrize the stretching obtained.

It may be observed that "or" gates 33,35 and "and" gate 37 cooperate with the sequence recognition apparatus 50 to form a first correlation indicator for signals derived (without difference in delay) from the respective absolute value circuits 28 and 18, while "or" gates 33,35, delay device 38, and "and" gate 39 cooperate with the sequence recognition apparatus 50 to form a second correlation indicator for signals derived (with a difference in delay) from the respective absolute value circuits 28 and 18. Switching of multiplexer 25 to an operating state resulting in high frequency component suppression for the signals delivered to the receiver's luminance channel occurs in response to an indication of correlation by either (or both) of the aforementioned correlation indicators.

To aid in an understanding of the operation of the illustrated system, several different examples of vertical transitions introducing a hanging dot problem will be considered below. For convenience of explanation, it will be assumed that the nature of control of the 4 f_{sc} clocking signal source (not illustrated) for the digital signal processing circuits of the illustrated receiver is such that the successively clocked samples of the composite video signals appearing at terminal CV coincide with +I, +Q,-I,-Q phases of the chrominance component.

Example 1: The vertical transition is such that a chrominance component appears with appreciable magnitude in the outputs of both bandpass filters (27,17) at the same I phase. A 1-0-1-0, etc. sequence appears at the output of "and" gate 37, while "and" gate 39 outputs a 0-0-0-0, etc. sequence. The delivery of seven successive alternate samples at the "1" level to apparatus 50 from gate 37 will trigger a correlation indication by apparatus 50, and switching of multiplexer 25 to a dot-removing mode of operation will ensue. Due to the above-discussed stretching action, the duration of the dot-removing mode can exceed the period of sequence existence to a suitable degree ensuring dot removal during transient edge periods.

Example 2: The vertical transition is such that a chrominance component appears with appreciable magnitude in the outputs of both bandpass filters (27,17), but at the I phase in the output of bandpass filter 27 and at a phase in quadrature therewith (i.e., at the Q phase) in the output of bandpass filter 17. In this instance, the output of "and" gate 37 (exhibiting a 0-0-0-0 sequence) will not trigger a correlation indication. However, a 1-0-1-0, etc. sequence appears at the output of "and" gate 39 to enable a correlation indication and appropriate swtiching of multiplexer 25.

Example 3: The vertical transition is such that a chrominance component appears with appreciable magnitude in the outputs of both bandpass filters (27,17), but at the I phase in the output of bandpass filter 27 and at a phase shifted 45° therefrom in the output of bandpass filter 17. In this instance, both of the "and" gates 37 and 39 output a 1-1-1-1,

etc. sequence, whereby both enable a correlation indication and appropriate switching of multiplexer 25.

The illustrative requirement for existence of a sequence of seven alternate samples at the "1" level to confirm existence of an interloping chrominance component in the combed luminance signal is consistent with the minimum duration of a chrominance component dictated by the limited bandwidth thereof, and enhances protection aginst misinterpreting the signal produced at a sharp luminance edge as a hanging dot occurrence requiring elimination.

The number of bits subject to elimination at the inputs of "or" gate 33 constitutes a threshold selection facility, with the number choice related to the hanging dot level viewed as tolerable and not requiring elimination. A different threshold choice may be associated with the bit elimination at the inputs of "or" gate 35, if desired.

In the illustrated arrangement, use of the absolute value circuit 28, for example, permits the associated "or" gate 33 to perform the same threshold test for both the positive and negative swings of the high frequency components passed by bandpass filter 27. It will be appreciated that other implementations, wherein the positive and negative swings of the bandpass filter output are subject to scrutiny in separate, parallel channels, are also feasible. It should also be noted that each of the signal combiners (13,15,21,31) of the illustrated arrangement desirably incorporates a divide-by-two operation at its output for conventional dynamic range maintenance purposes.

Claims

1. A digital correlation indicator, in a color television receiver employing a system for processing composite color television signals appearing in a digital format, said composite color television signals being inclusive of a luminance signal component and a chrominance signal component comprising sidebands developed by the modulation of a color subcarrier of a frequency f_{sc}; said system including comb filter apparatus (11,13,15,17,19,21,27) for developing a first comb filtered signal representing composite signals subjected to a first comb filter characteristic exhibiting a first plurality of response peaks and producing a first digital signal of "m" bits representative of a first bipolar signal component comprising high frequency components of said first comb filtered signal, and a second comb filtered signal representing composite signals subjected to a second comb filter characteristic exhibiting a second plurality of response peaks interleaved with the response peaks of said first plurality, and providing second digital signal of "m" bits representative of a second bipolar component signal comprising high frequency components of said second comb filtered signal; said digital correlation indicator being characterized by:

first logic circuit means (28,33) responsive to only the "k" most significant bits of said first digital signal, where "k" is less than "m", for outputting a "1" whenever said first digital signal is representative of an excursion of said first bipolar signal component, in either a positive or a negative direction, which equals or exceeds a threshold determined by the "k'th" most significant bit of said first digital signal;

second logic circuit means (18,35) responsive to only the "j" most significant bits of said second digital signal, where "j" is less than or equal to "m", for outputting a "1" whenever said second digital signal is representative of an excursion of said second bipolar signal component, in either a positive or a negative direction, which equals or exceeds a threshold determined by the "j'th" most significant bit of said second digital signal;

an "and" gate (37) having two inputs, one responsive to the output of said first logic circuit means and the other responsive to the output of said second logic circuit means and

correlation indication signal developing means (50,60) responsive to the output of said "and" gate, comprising means (50) for recognizing the existence of a predetermined sequence of logic levels in a train of output pulses developed by said "and" gate.

2. Apparatus in accordance with claim 1 wherein the sequence existence recognizing means includes:

signal delay means (51,56) having a plurality of successive signal takeoff points; the amount of delay between successive ones of said takeoff points being the same; the input of said delay means being responsive to the output of said "and" gate (37);

a plurality of signal paths, each connected to a respectively different one of said signal takeoff points;

a second "and" gate (58) having a plurality of inputs equal in number to said plurality of signal paths, each of said signal paths terminating at a respectively different one of said plurality of inputs of said second "input" gate; and

wherein said correlation indication signal developing means also includes a control signal former (60) responsive to the output of said second "and" gate.

etc. sequence, whereby both enable a correlation indication and appropriate switching of multiplexer 25.

The illustrative requirement for existence of a sequence of seven alternate samples at the "1" level to confirm existence of an interloping chrominance component in the combed luminance signal is consistent with the minimum duration of a chrominance component dictated by the limited bandwidth thereof, and enhances protection aginst misinterpreting the signal produced at a sharp luminance edge as a hanging dot occurrence requiring elimination.

The number of bits subject to elimination at the inputs of "or" gate 33 constitutes a threshold selection facility, with the number choice related to the hanging dot level viewed as tolerable and not requiring elimination. A different threshold choice may be associated with the bit elimination at the inputs of "or" gate 35, if desired.

In the illustrated arrangement, use of the absolute value circuit 28, for example, permits the associated "or" gate 33 to perform the same threshold test for both the positive and negative swings of the high frequency components passed by bandpass filter 27. It will be appreciated that other implementations, wherein the positive and negative swings of the bandpass filter output are subject to scrutiny in separate, parallel channels, are also feasible. It should also be noted that each of the signal combiners (13,15,21,31) of the illustrated arrangement desirably incorporates a divide-by-two operation at its output for conventional dynamic range maintenance purposes.

Claims

1. A digital correlation indicator, in a color television receiver employing a system for processing composite color television signals appearing in a digital format, said composite color television signals being inclusive of a luminance signal component and a chrominance signal component comprising sidebands developed by the modulation of a color subcarrier of a frequency f_{sc}; said system including comb filter apparatus (11,13,15,17,19,21,27) for developing a first comb filtered signal representing composite signals subjected to a first comb filter characteristic exhibiting a first plurality of response peaks and producing a first digital signal of "m" bits representative of a first bipolar signal component comprising high frequency components of said first comb filtered signal, and a second comb filtered signal representing composite signals subjected to a second comb filter characteristic exhibiting a second plurality of response peaks interleaved with the response peaks of said first plurality, and providing second digital signal of "m" bits representative of a second bipolar component signal comprising high frequency components of said second comb filtered signal; said digital correlation indicator being characterized by:

first logic circuit means (28,33) responsive to only the "k" most significant bits of said first digital signal, where "k" is less than "m", for outputting a "1" whenever said first digital signal is representative of an excursion of said first bipolar signal component, in either a positive or a negative direction, which equals or exceeds a threshold determined by the "k'th" most significant bit of said first digital signal;

second logic circuit means (18,35) responsive to only the "j" most significant bits of said second digital signal, where "j" is less than or equal to "m", for outputting a "1" whenever said second digital signal is representative of an excursion of said second bipolar signal component, in either a positive or a negative direction, which equals or exceeds a threshold determined by the "j'th" most significant bit of said second digital signal;

an "and" gate (37) having two inputs, one responsive to the output of said first logic circuit means and the other responsive to the output of said second logic circuit means and

correlation indication signal developing means (50,60) responsive to the output of said "and" gate, comprising means (50) for recognizing the existence of a predetermined sequence of logic levels in a train of output pulses developed by said "and" gate.

2. Apparatus in accordance with claim 1 wherein the sequence existence recognizing means includes:

signal delay means (51,56) having a plurality of successive signal takeoff points; the amount of delay between successive ones of said takeoff points being the same; the input of said delay means being responsive to the output of said "and" gate (37);

a plurality of signal paths, each connected to a respectively different one of said signal takeoff points;

a second "and" gate (58) having a plurality of inputs equal in number to said plurality of signal paths, each of said signal paths terminating at a respectively different one of said plurality of inputs of said second "input" gate; and

wherein said correlation indication signal developing means also includes a control signal former (60) responsive to the output of said second "and" gate.

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3. Apparatus in accordance with claim 2 wherein said control signal former includes a succession of two-input "or" gates (0-1 to 0-n) and a plurality of delay devices (D-1 to D-n) with one input of each "or" gate of said succession rendered responsive to the output of said second "and" gate (58), with the output of each of said succession of "or" gates, with the exception of the last of said succession, being coupled via a respective one of said plurality of delay devices to the other input of the next succeeding one of said succession of "or" gates, and with said control signal appearing at the output of the last of said succession of "or" gates

wherein each of said delay devices imparts the same amount of delay.

4. Apparatus in accordance with claim 3 wherein the other input of the first of said succession of two-input "or" gates is effectively inactive.

5. Apparatus in accordance with claim 3 or 4 wherein the sum of the delays imparted by said plurality of delay devices exceeds the amount of delay between the first and last of said plurality of successive signal takeoff points.

6. Apparatus in accordance with claim 2,3,4 or 5 including a third "and" gate (39) having two inputs, a pair of additional signal paths respectively linking the outputs of said first (28,33) and second (18,35) logic circuit means with the respective inputs of said third "and" gate, said additional signal paths exhibiting a difference in signal delay (38) corresponding to a period at $4f_{sc}$; the input of said of delay means (51-56) being additionally responsive to the output of said third "and" gate.

7. Apparatus in accordance with claim 6 wherein the input of said delay means (51-56) receives signals from the output of an additional "or" gate (40), said additional "or" gate having a first input coupled to the output of said first-named "and" gate, and a second input coupled to the output of said third "and" gate.

8. Apparatus in accordance with claim 3 also including means (27,29,31,25) for subjecting said first comb filtered signal to high frequency component removal in response to development of said control signal.

9. Apparatus in accordance with claim 3 wherein said signal processing system is subject to clocking at a $4f_{sc}$ rate, wherein each of said delay devices imparts a delay equal to a period at $4f_{sc}$, and wherein the amount of delay between successive ones of said signal takeoff points corresponds to twice a period at $4f_{sc}$.

Patentansprüche

1. Digital-Korrelationsindikator in einem Farb-Fernsehempfänger, der ein System einsetzt zum Verarbeiten zusammengesetzter Farb-Fernsehsignale, die in einem Digitalformat auftreten, wobei die zusammengesetzten Farb-Fernsehsignale eine Luminanz-Signalkomponente und eine Chrominanz-Signalkomponente aufweisen, die Seitenbänder hat, welche durch Modulation eines Farb-Zwischenträgers mit einer Frequenz f_{SC} gebildet werden;
   - welches System eine Kammfilter-Einrichtung (11, 13, 15, 17, 19, 21, 27) beinhaltet zum Bilden eines ersten kammgefilterten Signales, welches zusammengesetzte Signale repräsentiert, die einer ersten Kammfilter-Charakteristik unterworfen worden sind, welche eine Mehrzahl von Antwortspitzen (response peaks) aufweist und wobei ein erstes Digitalsignal mit "m" Bits erzeugbar ist, welches repräsentativ für eine erste Bipolar-Signalkomponente ist, die eine Hochfrequenz-Komponente des ersten kammgefilterten Signales aufweist, und zum Bilden eines zweiten kammgefilterten Signales, das repräsentativ für zusammengesetzte Signale ist, die einer zweiten Kammfilter-Charakteristik unterworfen worden sind, welche eine zweite Mehrzahl von Antwortspitzen aufweist, die mit den Antwortspitzen der ersten Mehrzahl verschachtelt sind und wobei ein zweites Digitalsignal mit "m" Bits gebildet wird, das repräsentativ für eine zweite Bipolar-Signalkomponente ist, die Hochfrequenz-Komponenten des zweiten kammgefilterten Signales aufweist;
   - wobei der Digital-Korrelationsindikator **gekennzeichnet** ist durch;
   - erste Logik-Schaltungsmittel (28, 33), die abhängig von nur den "k" hochwertigen (most significant) Bits des ersten Digitalsignals sind, wobei "k" geringer als "m" ist, zum Abgeben einer "1", wann immmer das erste Digitalsignal repräsentativ für eine Abweichung (excursion) der ersten Bipolar-Signalkomponente in entweder einer positiven oder negativen Richtung ist, welche gleich oder größer einem Schwellenwert ist, der durch das "k-te" hochwertige Bit (MSB) des ersten

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Digitalsignales bestimmt wird;

- zweite Logik-Schaltungsmittel (18, 35), welche abhängig von den nur "j" hochwertigen Bits des zweiten Digitalsignales sind, wobei "j" geringer oder gleich "m" ist, zum Abgeben einer "1", wann immer das zweite Digitalsignal repräsentativ für eine Abweichung (excursion) der zweiten Bipolar-Signalkomponente in entweder einer positiven oder negativen Richtung ist, welche gleich oder größer einem Schwellenwert ist, der von dem "j-ten" hochwertigen Bit des zweiten Digitalsignales bestimmt wird;
- ein "UND"-Gatter (37) mit zwei Eingängen, einer abhängig von dem Ausgangssignal der ersten Logik-Schaltungsmittel und der andere abhängig von dem Ausgangssignal der zweiten Logik-Schaltungsmittel;
- Korrelations-Indikationssignal-Bildungsmittel (50, 60), die abhängig von dem Ausgangssignal des "UND"-Gatters sind, welche Mittel (50) aufweisen zum Erkennen der Anwesenheit einer vorbestimmten Sequenz von Logikpegeln in einer Folge von Ausgangspulsen, die von dem "UND"-Gatter gebildet werden.

2. Einrichtung nach Anspruch 1, bei der die Sequenzexistenz-Erkennungsmittel aufweisen:
   - Signal-Verzögerungsmittel (51, 56) mit einer Mehrzahl von aufeinanderfolgenden Signal-Abnahmepunkten (signal takeoff points); wobei die Verzögerung (amount of delay) zwischen aufeinanderfolgenden der Abnahmepunkte gleich ist; wobei der Eingang der Verzögerungsmittel abhängig von dem Ausgangssignal des "UND"-Gatters (37) ist;
   - eine Mehrzahl von Signalpfaden, wovon jeder mit einem jeweils unterschiedlichen Punkt der Signal-Abnahmepunkte verbunden ist;
   - ein zweites "UND"-Gatter (58) mit einer Mehrzahl von Eingängen, die zahlenmäßig gleich sind der Mehrzahl von Signalpfaden, wovon jeder der Signalpfade an einem jeweils unterschiedlichen der Mehrzahl von Eingängen des zweiten "Eingangs"-Gatters endet;
   - wobei die Korrelations-Indikationssignal-Bildungsmittel auch ein Steuersignal-Former (60) beinhalten, welcher abhängig von dem Ausgangssignal des zweiten "UND"-Gatters ist.

3. Einrichtung nach Anspruch 2, bei welcher der Steuersignal-Former eine Folge von zwei-Eingangs-"ODER"-Gattern (0-1 bis 0-n) und eine Mehrzahl von Verzögerungseinrichtungen (D-1 bis D-n) beinhaltet, wobei ein Eingang jedes "ODER"-Gatters der Folge (succession) abhängig gemacht ist von dem Ausgangssignal (Ausgang) des zweiten "UND"-Gatters (58), wobei die Ausgange jedes der Folge von "ODER"-Gattern - mit Ausnahme des letzten dieser Folge - über eine jeweilige Verzögerungseinrichtung der Mehrzahl der Verzögerungseinrichtungen auf den anderen Eingang des nächstfolgenden der Folge von "ODER"-Gattern gekoppelt ist und wobei das Steuersignal am Ausgang des letzten der Folge von "ODER"-Gattern erscheint;
   - wobei jede der Verzögerungseinrichtungen dieselbe Verzögerungs(zeit) bewirkt.

4. Einrichtung nach Anspruch 3, bei welcher der andere Eingang des ersten der Folge von Zwei-Eingangs-"ODER"-Gattern wirksam inaktiv ist.

5. Einrichtung nach Anspruch 3 oder 4, bei der die Summe der Verzögerung, welche durch die Mehrzahl von Verzögerungseinrichtungen bewirkt wird, den Verzögerungsbetrag zwischen dem ersten und letzten der Mehrzahl von aufeinanderfolgenden Signal-Abnahmepunkte überschreitet.

6. Anordnung nach Anspruch 2, 3, 4 oder 5, beinhaltend ein drittes "UND"-Gatter (39) mit zwei Eingängen, einem Paar von zusätzlichen Signalpfaden, welche jeweils die Ausgänge der ersten (28, 33) und zweiten (18, 35) Logik-Schaltungsmittel verbinden, und zwar mit den jeweiligen Eingängen des dritten "UND"-Gatters, wobei die zusätzlichen Signalpfade einen Unterschied in der Signalverzögerung (38) aufweisen, welcher mit einer Periode von $4 \cdot f_{SC}$ korrespondiert; wobei der Eingang der Verzögerungsmittel (51-56) zusätzlich abhängig von dem Ausgangssignal des dritten "UND"-Gatters ist.

7. Einrichtung nach Anspruch 6, bei welcher der Eingang der Verzögerungsmittel (51-56) Signale von dem Ausgang eines zusätzlichen "ODER"-Gatters (40) erhält, wobei das zusätzliche "ODER"-Gatter einen ersten - mit dem Ausgang des zuerst genannten "UND"-Gatters gekoppelten - Eingang und einen zweiten - mit dem Ausgang des dritten "UND"-Gatters gekoppelten - Eingang aufweist.

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8. Einrichtung nach Anspruch 3, welche auch Mittel (27, 29, 31, 25) beinhaltet zum Aussetzen/Unterwerfen des kammgefilterten Signals einer Hochfrequenz-Komponenten-Beseitigung abhängig von der Bildung des Steuersignals.

9. Einrichtung nach Anspruch 3, bei welcher die Signal-Verarbeitungseinrichtung einer $4 \cdot f_{SC}$-Taktfrequenzrate ausgesetzt ist, wobei jede der Verzögerungseinrichtungen eine Verzögerung einbringt (bewirkt), die gleich einer Periode bei $4 \cdot f_{SC}$ ist und wobei der Betrag der Verzögerung zwischen aufeinanderfolgenden der Signal-Abnahmepunkte mit der doppelten Periode bei $4 \cdot f_{SC}$ korrespondiert.

Revendications

1. Indicateur de corrélation numérique, dans un récepteur de télévision couleur utilisant un système pour traiter les signaux de télévision couleur composites apparaissant selon un format numérique, lesdits signaux de télévision couleur composites étant constitués d'une composante de signaux de luminance et d'une composante de signaux de chrominance comprenant des bandes latérales développées par la modulation d'une sous-porteuse couleur de fréquence f_{sc}; ledit système incluant un dispositif de filtre à peigne (11, 13, 15, 17, 19, 21, 27) pour développer un premier signal filtré par filtre à peigne représentant les signaux composites soumis à une première caractéristique de filtre à peigne présentant une première pluralité de pics de réponse et produisant un premier signal numérique de "m" bits représentatifs d'une première composante de signaux bipolaires comprenant des composantes de haute fréquence dudit premier signal filtré par filtre à peigne et un second signal filtré par filtre à peigne représentant des signaux composites soumis à une seconde caractéristique de filtre à peigne présentant une seconde pluralité de pics de réponse intercalée avec les pics de réponse de ladite première pluralité et fournissant un second signal numérique de "m" bits représentatifs d'un second signal de composante bipolaire comprenant des composantes de haute fréquence dudit signal filtré par filtre à peigne ; ledit indicateur de corrélation numérique étant caractérisé par :

un premier moyen de circuit logique (28, 33) seulement sensible aux "k" bits les plus significatifs dudit premier signal numérique où "k" est inférieur à "m" pour délivrer un "1" chaque fois que ledit premier signal numérique est représentatif d'une excursion de ladite première composante de signal bipolaire, soit dans une direction positive soit dans une direction négative, qui égale ou dépasse un seuil déterminé par le "$k^{ème}$" bit le plus significatif dudit premier signal numérique ;

un second moyen de circuit logique (18,35) sensible seulement aux "j" bits les plus significatifs dudit second signal numérique où "j" est inférieur ou égal à "m" pour délivrer un "1" chaque fois que ledit second signal numérique est représentatif d'une excursion de ladite seconde composante de signal bipolaire, soit dans une direction positive soit dans une direction négative, qui égale ou dépasse un seuil déterminé par le "$j^{ème}$" bit le plus significatif dudit second signal numérique

une porte "et" (37) comportant deux entrées, l'une sensible à la sortie dudit premier moyen de circuit logique et l'autre sensible à la sortie dudit second moyen de circuit logique et

un signal d'indication de corrélation développant un moyen (50, 60) sensible à la sortie de la porte "et", comprenant un moyen (50) pour reconnaitre l'existence d'une séquence prédéterminée de niveaux logiques dans un train d'impulsions de sortie développé par ladite porte "et".

2. Dispositif selon la revendication 1 dans lequel le moyen de reconnaissance de l'existence de séquence inclut :

un moyen pour retarder un signal (51, 56) comportant une pluralité de points de prise de signaux successifs ; la quantité de retard entre points successifs desdits points de prise étant la même ; l'entrée dudit moyen de retard étant sensible à la sortie de ladite porte "et" (37) ;

une pluralité de trajets du signal, chacun étant connecté à l'un des points respectivement différent desdits points de prise de signaux ;

une seconde porte "et" (58) comportant une pluralité d'entrées égale en nombre à ladite pluralité de trajets du signal, chacun desdits trajets du signal se terminant à l'une des entrées respectivement différente de ladite pluralité d'entrées de ladite seconde porte "et"; et

dans lequel ledit moyen de développer un signal d'indication de corrélation inclut également un dispositif de formation de signal de commande (60) sensible à la sortie de ladite seconde porte "et".

3. Dispositif selon la revendication 2 dans lequel ledit dispositif de formation de signal de commande inclut une succession de portes "ou" à deux entrées (0-1 à 0-n) et une pluralité de

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dispositifs à retard (D-1 à D-n) avec une entrée de chaque porte "ou" de ladite succession rendue sensible à la sortie de ladite seconde porte "et" (58), avec la sortie de chacune de ladite succession de portes "ou", à l'exception de la dernière de ladite succession, étant couplée via un dispositif respectif de ladite pluralité de dispositifs à retard à l'autre entrée de la prochaine porte qui suit de ladite succession de portes "ou" et avec ledit signal de commande apparaissant à la sortie de la dernière porte de ladite succession de portes "ou"

dans lequel chacun desdits dispositifs à retard communique la même quantité de retard.

4. Dispositif selon la revendication 3 dans lequel l'autre entrée de la première porte de ladite succession de portes "ou" à deux entrées est effectivement inactive.

5. Dispositif selon la revendication 3 ou 4 dans lequel la somme des retards communiqués par ladite pluralité de dispositifs à retard dépasse la quantité de retard entre les premier et dernier points de ladite pluralité des points successifs de prise de signal.

6. Dispositif selon la revendication 2, 3, 4 ou 5 incluant une troisième porte "et" (39) ayant deux entrées , une paire de trajets du signal supplémetaires reliant respectivement les sorties desdits premier (28, 33) et second (18, 35) moyens de circuit logique aux entrées respectives de ladite troisième porte "et", lesdits trajets du signal supplémentaires présentant une différence en retard de signal (38) correspondant à une période à $4f_{sc}$; l'entrée dudit moyen de retard (51-56) étant sensible, de façon additionnelle, à la sortie de ladite troisième porte "et".

7. Dispositif selon la revendication 6 dans lequel l'entrée dudit moyen de retard (51-56) reçoit des signaux de la sortie d'une porte "ou" supplémentaire (40), ladite porte "ou" supplémentaire ayant une première entrée couplée à la sortie de ladite porte "et" première nommée et une seconde entrée couplée à la sortie de ladite troisième porte "et".

8. Dispositif selon la revendication 3 comprenant également un moyen (27, 29, 31, 25) pour soumettre ledit premier signal filtré par filtre à peigne pour élimination de la composante de haute fréquence en réponse au développement dudit signal de commande.

9. Dispositif selon la revendication 3 dans lequel ledit système de traitement de signal est soumis à une synchronisation à une fréquence de $4f_{sc}$, dans lequel chacun desdits dispositifs à retard communique un retard égal à une période à 4 f_{sc}, et dans lequel la quantité de retard entre points successifs desdits points de pise de signal correspond à deux fois une période à $4f_{sc}$.

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