FCBGA Package Structure

The present invention is a continue in part (CIP) application of a co-pending application number 10/835,571 filed on April, 30, 2004, and entitled "Structure of Package". The co-pending application is incorporated herein for reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a package structure, and more particularly to a FCBGA (Flip Chip Ball Grid Array) package structure, the package structure can avoid the open circuit caused by the solder ball cracking due to the temperature variation induces the reinforcing stress between the solder balls and a print circuit board.

2. Description of the Prior Art

The earlier lead frame package technology is already not suitable for the advanced semiconductor dies due to the density of the terminals thereof is too high. Hence, a new package technology of BGA (Ball Grid Array) has been developed to satisfy the packaging requirement for the advanced semiconductor dies. The BGA package

has an advantage of that the spherical terminals has a shorter pitch than that of the lead frame package, and the terminals of the BGA are unlikely to be damage and deform. In addition, the shorter signal transmitting distance benefits to raise the operating frequency to conform to the requirement of faster efficiency. Most of the package technologies divide dice on a wafer into respective dies and then to package and test the die respectively. Another package technology, called "Wafer Level Package (WLP)", can package the dies on a wafer before dividing the dice into respective individual die. The WLP technology has some advantages, such as a shorter producing cycle time, lower cost, and no need to under-fill or molding.

Besides, a partial package structure using in the present marketing is shown as Fig. 1. The package structure comprises an isolation layer 103 and a passivation layer 102 of an IC device 100. The material of the isolation layer 103 may be a dielectric layer with a thickness of 5 micron such as BCB, polyimides etc.. The material of the passivation layer 102 is polyimides or SiN. The redistribution layer(RDL)104 is combined with the isolation layer 103, Al pads 101 of the IC device. The material of the redistribution layer(RDL)104 may be Cu/Ni/Au alloy with a thickness of 15 micron. Moreover, an isolation layer 105 covers the redistribution layer (RDL) 104. And, the isolation layer 105 has a plurality of openings. Each of the openings has a solder ball 106 to electrically couple with a print circuit board or

external parts. The material of the isolation layer 105 may be a dielectric layer such as BCB, epoxy, or polyimides etc..

The aforementioned package structure generally needs an additional material to intensively fix the solder ball 106. It has a drawback mentioned as follow: the adhesion between the redistribution layer (RDL) 104 and the isolation layer 105 is too strong, which is drawback to the solder ball. When the solder ball 106 joints to the print circuit board, the stress may be induced by temperature influence at the joint part between the solder ball 106 and the redistribution layer (RDL) 104, it is indicated by the area 107, the solder ball 106 will be cracked owing to reinforcing stress raised by temperature variation, thereby causing open circuit between the solder ball and pad.

In view of the aforementioned, the present invention provides an improved package structure to overcome the above drawback.

SUMMARY OF THE INVENTION

It is an objective of the present invention to provide a flip chip ball grid array (BGA) package structure. The package structure of the present invention can avoid open circuit generated by solder ball cracking due to reinforcing stress.

The present invention provides a flip chip ball grid array (BGA) package structure. The structure comprises a flip chip solder bumping structure, having a plurality of chips and solder bumps. A substrate has a plurality of conductive lines electrically coupling with the plurality of solder bumps. A print circuit board has a plurality of solder balls electrically coupling with the plurality of conductive lines.

The flip chip may be an IC (Integrated Circuit).

The flip chip package structure has a die formed thereon, solder bumps, a patterned first elastic dielectric layer, a conductive layer and a second patterned elastic dielectric layer. The patterned first elastic dielectric layer is provided adjacent to a passivation layer of the IC (Integrated Circuit). The conductive layer is configured over the passivation layer and bonding pads of the IC to have a curved or winding or zigzag conductive layer pattern due to the topography of the patterned first elastic dielectric layer, wherein the zigzag conductive layer pattern is partially attached on the passivation layer and partially attached on the first elastic dielectric layer. The second elastic dielectric layer is formed over the conductive layer having a plurality of openings, and solder bumps can be formed in the openings to electrically couple to the plurality of conductive lines.

The conductive layer will not directly stretch the bonding pads of the chips when the solder bumps are placed on the substrate. The zigzag conductive layer creates buffer area, like a cushion to absorb the stress by poor adhesion between the curved or zigzag conductive layer pattern and the patterned first and patterned second elastic dielectric layer.

The curved or zigzag conductive layer pattern is starting from the bonding pad to solder pad under the solder bump.

The solder bump can be lifted without broken due to performance of the first and second elastic dielectric layer and poor adhesion between the conductive layer and the first and second elastic dielectric layer when the thermal extension of the substrate is higher than the flip chip.

A conductive bumping arrangement for a package comprises a plurality of bonding pads formed on a die and a plurality of bumpings formed over the die and connected to the plurality of bonding pads by conductive traces, wherein an included angle between a line segment from center of the die to center of the bumping and a radius orientation from the center of the bumping of the conductive traces departing from the bumping is greater than 45^0 (degrees) . The

conductive trace extends from a bonding pad to a pad under the bumping.

BRIEF DESCRIPTION OF THE DRAWINGS

The above objects, and other features and advantages of the present invention will become more apparent after reading the following detailed description when taken in conjunction with the drawings, in which:

Fig. 1 is a schematic diagram of a conventional package structure.

FIG. 2 is a schematic diagram of a package structure according to the present invention.

FIG. 3 is a top view of conductive layer pattern and solder bumps of one chip of the wafer level package structure according to the present invention.

Fig. 4 is a schematic diagram of a flip chip ball grid array (FCBGA) package structure according to the present invention.

Fig. 5 is a schematic diagram of a flip chip ball grid array (FCBGA) package structure according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The present invention provides a backend structure of packag, and the scope of the present invention is expressly not limited expect

as specified in the accompanying claims. The present invention discloses a structure of flip chip BGA package comprising: a patterned elastic dielectric layer covering a partial region of a underlying layer; and a conductive layer configured on the patterned elastic dielectric layer to have a zigzag pattern to absorb stress due to the topography of the patterned elastic dielectric layer. Wherein the material for the elastic dielectric layer comprises BCB, SINR (Siloxane polymer), epoxy, polyimides or resin. The material for the conductive layer is metal alloy.

As shown in FIG. 2, it is a schematic diagram of one package structure according to the present invention. The packaging is expressly not limited expect as specified in the accompanying claims of the present invention. The present invention comprises a patterned elastic dielectric layer 203 covering a partial region of passivation layer 202 of a device 200. The material of the elastic dielectric layer 203 may be dielectric, such as BCB, SINR (Siloxane polymer), epoxy, polyimides or resin etc.. The patterned elastic dielectric layer 203 has a plurality of openings to expose the underlying passivation layer 202. The material of the passivation layer 202 comprises polyimide or SiN. The area indicated by 207 will suffer the external force as shown in FIG. 2.

The redistribution layer (RDL) 204 on the patterned elastic

dielectric layer 203 is configured with a zigzag or winding conductive layer pattern owing to the pattern topography of the elastic dielectric layer. In one preferred embodiment, the material of the conductive layer includes Ti/Cu alloy or Cu/Ni/Au alloy with a thickness of 15 micron. The Ti/Cu alloy may be formed by sputtering technique, the Cu/Ni/Au alloy may be formed by electroplating. The material of the bonding pads 201 may be Al or Cu or the combination.

Furthermore, an elastic dielectric layer 205 is formed on the conductive layer 204 and the elastic dielectric layer 205 have a plurality of openings. Each of the openings has a contact metal ball 206 to electrically couple to a print circuit board (PCB) or external parts(not shown). The contact metal ball 206 may be a conductive ball such as solder ball 206. The material of the elastic dielectric layer 205 may be formed of dielectric such as BCB, SINR (Siloxane polymer), epoxy, polyimides or resin etc..

The conductive layer 204 adjacent to the fixed area 210 of the package structure will not directly stretch the bonding pads 201 of inter-connector of the IC device 200 due to the passivation layer 202 tightly "catches" the conductive layer 204 by the scheme disclosed by the present invention. The temperature influence will be reduced owing to the conductive layer 204 directly joint to the passivation layer 202 when the solder ball 206 mounts to the print circuit board, it may

induce thermal stress.

Besides, in the buffer area 209 of the package structure, the conductive layer 204 is partially attached to the passivation layer 202 and partially formed on the elastic dielectric layer 203 so that the conductive layer 204 is configured to have a curve or zigzag pattern. The stress generated by temperature variation will be distributed due to the shape of the conductive layer and the zigzag structure of the conductive layer acts as a cushion to release the thermal stress. The adhesion between the conductive layer 204 and the elastic dielectric layer 203 is poor, and the conductive layer 204 will slightly peel from the surface of the elastic dielectric layer 203 when external force applied. The extension of the conductive layer will be increased owing to curved conductive layer pattern with zigzag scheme will slightly peel and absorbs the thermal stress. Therefore, the life time of the package structure will be increased. Especially, when the solder ball 206 is far away from the bonding pad.

Furthermore, the zigzag structure of the conductive layer 204 is extending from the bonding pad 201 to solder pad under the solder ball 206. An included angle ϕ between a line segment from center C1 of the chip to center C2 of the solder ball 206 and the orientation of the radius from the center C2 of ball 206 to the initial direction of the zigzag structure of the conductive layer 204 departing from the solder

ball 206 is greater than 45º(degrees), as shown in fig.3. The solder ball 206 can be lifted without broken due to performance of the first and second elastic dielectric layer 203,205 and poor adhesion between the conductive layer 204 and the first and second elastic dielectric layer 203,205 when the thermal extension of the substrate is higher than the flip chip. Therefore, under the arrangement of the shape and the extending angle of the conductive trace from the ball 206, the under-fill material can be omitted. The cost and the processes are simplified by the design. For example, from figure 3, it is the top view of the bonding balls. Solder bump A13 from bonding Pad to solder pad, the trace X/Y direction (paper surface) has been modified, once the thermal extension of substrate is higher than the silicon, the solder bump of A13 can be lifted without broken the solder join due to the dielectric material performance – elastic and high elongation and the adhesion between metal and SINR is Poor.

The present invention also comprises a patterned elastic dielectric layer 208 formed between the elastic dielectric layer 203 and the conductive layer 204 to increase the zigzag level (namely, increase the number of the zigzag shape) of the conductive layer under the solder ball. The material of the elastic dielectric layer 208 comprises BCB, SINR (Siloxane polymer), epoxy, polyimides or resin.

As shown in Fig. 4, it is a schematic diagram of a flip chip ball grid

array (BGA) package structure according to the present invention. The flip chip solder bumping structure is the same as the package structure of fig.2. An under-fill material 404 is formed to fill among the plurality of solder bumps 402 on the chip 400. The redistribution layer (RDL) 401 is configured with a zigzag or winding conductive layer pattern to electrically couple with solder bumps 402. An elastic dielectric layer 403 is formed to isolate from redistribution layer (RDL) 401. The contact pad 407 and conductive trace 408 of a substrate 405 are formed to electrically couple with solder bumps 402 and solder balls 406 respectively. Besides, the solder balls 406 formed on the substrate 405 may be electrically coupled to a print circuit board(PCB) or external parts (not shown).

As shown in Fig. 5, it is a schematic diagram of a flip chip ball grid array (FCBGA) package structure according to the present invention. The flip chip solder bumping structure is almost the same as the package structure of fig.2. In the embodiment, the under-fill material is omitted, namely, it will not be filled among the plurality of solder bumps 502 on the chip 500. The redistribution layer (RDL) 501 is configured with a zigzag or winding conductive layer pattern to electrically couple with solder bumps 502. The contacts 504,505 of a substrate 503 are formed to electrically couple with solder bumps 502 and solder balls 506 respectively. Besides, the solder balls 506 formed on the substrate 503 may be electrically coupled to a print circuit

board (PCB) 507 through solder balls 506 coupled to the contact 508.

Hence, according to the present invention, the aforementioned package structure has the advantages list as follow: the FCBGA package structure of the present invention can avoid open circuit of the solder ball cracking generated by reinforcing stress due to temperature variation after the solder balls placed on the print circuit board. Moreover, it does not need an additional material to intensively fix the solder ball.

Although specific embodiments have been illustrated and described, it will be obvious to those skilled in the art that various modifications may be made without departing from what is intended to be limited solely by the appended claims.

CLAIMS

What is claimed is:

1. A structure of package, comprising:

a substrate having a plurality of conductive lines;

solder bumps electrically coupling with said plurality of conductive lines;

a patterned first elastic dielectric layer covering a partial region of a passivation layer formed on chips;

a conductive layer formed on said patterned first elastic dielectric layer to form a zigzag conductive layer pattern due to the topography of said patterned first elastic dielectric layer, wherein said zigzag conductive layer pattern is partially attached on said passivation layer and partially attached on said first elastic dielectric layer; and

a second elastic dielectric layer covering said conductive layer, said second elastic dielectric layer having a plurality of openings, each of said openings having one of said plurality of solder bumps formed thereon electrically coupling with one of said plurality of conductive lines.

2. The structure in claim 1, further comprising a print circuit board, having a plurality of solder balls electrically coupling with said plurality of conductive lines.

3. The structure in claim 2, further comprising an under-fill material formed among said plurality of solder bumps.

4. The structure in claim 1, wherein said conductive layer at a fixed area of said structure of package will not directly stretch bonding pads of said chips when said solder bumps are placed on said substrate, said zigzag conductive layer pattern acting as a buffer of said structure of package to absorb the stress.

5. The structure in claim 1, further comprising a patterned third elastic dielectric layer formed between said patterned first elastic dielectric layer and said conductive layer, wherein the material for said third elastic dielectric layer comprises BCB, SINR (Siloxane polymer), epoxy, polyimides or resin.

6. The structure in claim 1, wherein the material for said first elastic dielectric layer comprises BCB, SINR (Siloxane polymer), epoxy, polyimides or resin, wherein the material of said second elastic dielectric layer comprises BCB, SINR (Siloxane polymer), epoxy, polyimides or resin.

7. The structure in claim 1, wherein the material for said passivation layer is polyimides, wherein the material for said conductive layer is

metal alloy, wherein said metal alloy comprises Ti/Cu alloy or Cu/Ni/Au alloy, wherein said Ti/Cu alloy is formed by sputtering, wherein said Cu/Ni/Au alloy is formed by electroplating, wherein the thickness of said metal alloy is around 10~20 micron.

8. The structure in claim 4, wherein said zigzag conductive layer pattern extends from said bonding pad to solder pad under said solder bump, and an included angle between a line segment from center of said chip to center of said solder bump and a radius orientation from said center of said solder bump of said zigzag conductive layer pattern departing from said solder bump is greater than 45^0 (degrees).

9. The structure in claim 8, wherein said solder bump can be lifted without broken due to performance of said first and second elastic dielectric layer and poor adhesion between said conductive layer and said first and second elastic dielectric layer when the thermal extension of said substrate is higher than said chip.

10. A conductive bumping arrangement for a package, comprising:
a plurality of bonding pads formed on a die; and
a plurality of bumpings formed over said die and connected to said plurality of bonding pads by conductive traces, wherein an included angle between a line segment from center of said

die to center of said bumping and a radius orientation from said center of said bumping of said conductive traces departing from said bumping is greater than 45^0 (degrees).

11. The bumping arrangement in claim 10, wherein said conductive trace extends from a bonding pad to a pad under said bumping.