



METHOD AND APPARATUS FOR A GATED OSCILLATOR IN DIGITAL CIRCUITS

BACKGROUND OF THE INVENTION

5 The present invention relates to oscillators and more particularly to gated oscillators.

Oscillators have a wide range of uses. For example, microprocessor operation is synchronized by the periodic timing signals provided by an oscillator. Digital tachometers and digital speedometers in an automobile require a precision
10 reference to provide accurate read-outs. Medical devices such as pacemakers require an accurate pulse generator to ensure proper rhythmic stimulation of the heart.

A gated oscillator is an oscillator that starts or stops oscillating by an enabling signal. In a conventional gated oscillator, such as the one disclosed in U.S. Pat. No. 4,365,212, oscillations are produced by periodically charging and discharging a
15 capacitor between first and second voltage levels when the oscillator is enabled. If it is disabled, the oscillations are stopped by preventing the capacitor from periodically charging and discharging.

Let the first voltage level be lower than the second voltage level. If there is no extra circuitry associated with the capacitor, then the capacitor will continue to
20 discharge past the first voltage level toward the lower power supply voltage when the oscillation is stopped. When the oscillator is enabled, a certain amount of time is needed to charge the capacitor from lower power supply voltage to the first voltage level and then to the second voltage level, whereupon oscillatory behavior ensues. The delay in charging the capacitor from the lower power supply voltage to the first voltage level
25 causes the first pulse in the pulse train to be wider than the rest of the pulses. This error is undesirable in applications which require and expect predictable pulse widths. The error can be substantially corrected if extra circuitry is added to prevent the capacitor from discharging past the first voltage level. This, of course, increases the complexity of the gated oscillator circuitry.

30 Gated oscillators have many applications in digital circuits. In an article entitled "Gated oscillator emulates a flip-flop," published in the March 16, 1995 issue of EDN Magazine, a gated oscillator circuit is described in a flip-flop configuration. In another article entitled "Oscillator meets three requirements," published in the December



3, 1998 issue of EDN Magazine, a gated oscillator is described for use in clock circuit as the clocking source in a digital application.

A design that can be used as a gated oscillator is disclosed in U.S. Pat. No. 5,339,053. A shortcoming of this design, however, is that the enable signal and the gated
5 oscillation are mixed at the circuit's output. Additional external circuitry is therefore required to separate the two signals.

A simplistic gated oscillator circuit can be built using an AND logic gate. An enable signal is applied to one of its terminals and a continuous free running oscillator is applied to the other terminal. The output produces the desired gated oscillations. This
10 prior art gated oscillator requires an external continuous free running oscillator. A problem with this design is the inability of the enable signal to synchronize with the free running oscillator, thus producing indeterminate behavior. Another problem is that the free running oscillation fixes the frequency and duty cycle of the gated oscillator output. Yet another is that the free running oscillator is continually running, even when the
15 enable signal is removed. Consequently, there is unnecessary consumption of power.

There is a need, therefore, for digital circuit design using a gated oscillator circuit which requires reduced support circuitry. It is desirable to provide a design which is energy efficient. There is a need for a design which can provide a tunable oscillation frequency. There is a further for a design that can provide a tunable duty cycle of the
20 oscillation. It is also desirable that the design has an ability to synchronize the onset of oscillatory behavior with the enable signal.

SUMMARY OF THE INVENTION

A method for generating pulses in a digital circuit includes providing a
25 circuit having a variable operating point. The circuit is defined by a transfer function characterized by having an unstable operating region bounded by a first stable operating region and a second stable operating region. The circuit produces oscillatory output when its operating point is moved into the unstable region. The circuit produces a non-oscillatory output when its operating point is placed into either of the first and second
30 stable regions. The method further includes forcing the operating point into the unstable region to produce oscillatory output. The method further includes forcing the operating point into one of the stable regions in order to terminate oscillations.

A gated oscillator circuit in accordance with the invention includes a circuit having a transfer function defined by an unstable operating region bounded by a

first stable operating region and by a second stable operating region. The transfer function defines a set of operating points. The circuit is adapted to produce oscillatory output when the operating point is positioned in the unstable region. The circuit is further adapted to produce a non-oscillatory output when its operating point is positioned in
5 either of the first and second stable regions. A function generator, which selectively produces an output of a first level and an output of a second level is coupled to the circuit as an input signal. The operating point is forced into the unstable region when the function generator output is at the first level. This level is called an enable signal. The operating point is forced into one of the stable regions when the function generator output
10 is at its second output level. This level is referred to as a disable signal.

Consequently, the invention requires only the application of an enable signal to enable oscillations or a disable signal to terminate oscillations. The inventive circuit is advantageous in that its oscillations start and stop substantially instantaneously. There are no transients between the ON and OFF state of the oscillator. Another
15 advantage is that the period of the first cycle of oscillation during an ON period is the same as the subsequent cycles in that ON period. There is no need for additional supporting circuit elements or special circuits for maintaining standby levels in the capacitor. The circuit does not require any external free running oscillation. The circuit will generate its own oscillation when triggered by the enable signal. The circuit is
20 inherently synchronized with the enable signal. By tuning the circuit parameter, without changing the circuit configuration, the duty cycle and the frequency of oscillation can be varied. The gated oscillation at the output of the circuit is not overlapping with the enable signal and therefore no additional circuit is required to separate them.

25 BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A – 1C show how the present invention obviates the need for a clock in conventional clocked digital circuit designs.

Fig. 2 illustrates generally the transfer function of a circuit used in Figs. 1b and 1c.

30 Fig. 3 illustrates schematically a circuit arrangement for forcing the operating point between stable and unstable regions.

Figs. 4 – 6 are examples of circuit configurations in accordance with the invention.

Fig. 7 illustrates measurements taken from a circuit constructed in accordance with the invention.

DESCRIPTION OF THE SPECIFIC EMBODIMENTS

5 Referring to Fig. 1A, a typical digital circuit such as the illustrated dual slope analog-to-digital converter is shown. V_R is a referenced voltage and V_A is an analog voltage to be converted to a digital representation. The output of integrator 110 is an analog waveform that contains information of the amplitude of V_A with respect to V_R . A comparator that converts this analog waveform to an enable signal and AND gate
10 combination 112 that receives an external clocking signal together produce a gated oscillation output 114 which drives the counter.

Fig. 1B shows how a gated oscillator 100 in accordance with the present invention can be used to replace the conventional gated clock generation circuit 112 of conventional digital circuits. As shown in Fig. 1C, generally, the clock input of most
15 conventional digital circuits can be driven by the gated oscillator circuit of the present invention. The discussion which follows will focus on the inventive oscillator. It is understood that digital circuits encompass a wide range of applications. The invention is therefore not limited to any one particular digital circuit. Rather, the invention relates to digital circuits having a clock/oscillation generation function provided by the circuit
20 disclosed hereinbelow.

Referring to Fig. 2, gated oscillator circuits in accordance with the present invention exhibit a transfer function whose curve has a generally N-shaped appearance. For the purposes of the present invention, the "transfer function" of a circuit refers to the relationship between any two state variables of that circuit. For example, electronic
25 circuits are typically characterized by their I-V curves, the two state variables being current (I) and voltage (V). Such curves indicate how one state variable (e.g., current, I) changes as the other state variable (voltage, V) varies. As can be seen in Fig. 2, a transfer function curve 202 includes a portion which lies within a region 204, referred to herein as an "unstable" region. The unstable region is bounded on either side by regions 206 and
30 208, each of which is herein referred to as the "stable" region. As can be seen in Fig. 2, portions of the transfer function curve 202 also lie in the stable regions.

A circuit in accordance with the invention has an associated "operating point" which is defined as its location on the transfer function 202. Fig. 2 shows three operating point positions, 210, 210', and 210". The nature of the output of the circuit

depends on the location of the operating point along the transfer function. If the operating point is positioned along the portion 214 of the transfer function that lies within region 204, the output of the circuit will exhibit an oscillatory behavior. Hence, the region 204 in which this portion of the transfer function is found is referred to as an unstable region.

- 5 If the operating point is positioned along the portions 216, 218 of the transfer function that lie within either of regions 206 and 208, the output of the circuit will exhibit a generally time-varying but otherwise non-oscillatory behavior. For this reason, regions 206 and 208 are referred to as stable regions.

Referring to Figs. 2 and 3, a general configuration for varying the
10 operating point of a circuit is shown. The figure shows a circuit 302 having an input defined by terminals 303 and 305. An inductive element 304 is coupled to terminal 305. A function generator 310 is coupled between the other end of inductive element 304 and terminal 303 of circuit 302, thus completing the circuit. In accordance with the invention, circuit 302 has a transfer function which appears N-shaped. Further in accordance with
15 the invention, circuit 302 is characterized in that its operating point can be moved into and out of the unstable region 204 depending on the level of the output V_o of function generator 310. This action controls the onset of oscillatory behavior, and cessation of such oscillatory behavior, at the output V_{out} of circuit 302. Forcing the operation point to be on a portion of the transfer function that lies in the unstable region 204 will result in
20 oscillatory behavior. Forcing the operating point to lie on the transfer function found in one of the stable regions 206, 208 will result in non-oscillatory behavior.

An example of a circuit that exhibits the N-shaped transfer function is an operation amplifier (op-amp) configured with a feedback resistor between the op-amp output and its non-inverting input. Fig. 4 shows such a circuit 400. An op-amp 402
25 includes a positive feedback path wherein the op-amp's output V_{out} feeds back to its non-inverting input via feedback resistor 408 having a resistance R_f . A portion of the output voltage of op-amp 402 is provided to its inverting input. Fig. 4 shows a voltage dividing circuit comprising resistors 404 and 406, having respectively resistances R_1 and R_2 , to supply a portion of the op-amp output back to its inverting input. Completing the circuit
30 is an inductor 410 and function generator 310 coupled in series between the non-inverting input of op-amp 402 and ground. A typical off-the-shelf op-amp can be used, such as the commonly available LM-358 op-amp.

Another example of a circuit having an N-shaped transfer function is shown in Fig. 5. Here, circuit 500 comprises a tunnel diode 502 coupled to function

generator 310 through inductive element 410. The output V_{out} is taken across resistor 504, which is coupled between the other end of diode 502 and ground.

The foregoing circuits can be expressed by the following generalized pair of coupled equations which describe a two-variable Van der Pol (VdP) oscillator:

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$$L \frac{dy}{dt} = f(t) - x \quad (1)$$

$$\varepsilon \frac{dx}{dt} = y - \Psi(x) \quad (2)$$

10 where x and y are the state variables of the VdP oscillator,

L and ε are parameters of the VdP oscillator,

$f(t)$ is a time varying forcing function that is controllable and can be used to move the operating point of the VdP oscillator, and

$\Psi(x)$ is a cubic function of variable x . $\Psi(x)$ is the key for establishing a

15 controllable VdP oscillator.

Equations (1) and (2) relate to the circuit of Fig. 4 by replacing variables x and y respectively with V and i to represent physical variables that are commonly used in a circuit design. Hence,

$$L \frac{di}{dt} = V_s - V \quad (3)$$

20 $\lim_{C \rightarrow 0} C \frac{dV}{dt} = i - \Psi(V) \quad (4)$

Parameter C in Eq. (4) represents a small parasitic capacitor 420 across the voltage V , shown in Fig. 4 by phantom lines. V_s is the time varying voltage source of function generator 310 which acts as forcing function. The operating point of circuit 400
25 is obtained by setting $\frac{dV}{dt} = 0$ and $\frac{di}{dt} \approx 0$. Equations (3) and (4) become $V = V_s$ and $i = \Psi(V)$, respectively. $i = \Psi(V)$ is the transfer function of the op amp with R_0 , R_1 and R_2 combinations. Thus, with reference back to Fig. 2, it can be seen that transfer function curve 202 is defined by $i = \Psi(V)$.

The intersection between the line $V = V_s$ and the curve $i = \Psi(V)$ defines
30 the operating point 210 of the circuit. A closer inspection of transfer function 202 defined by $i = \Psi(V)$ reveals that segments 216, 218 have positive slope ($di/dV > 0$) and segment

214 has a negative slope ($dl/dV < 0$). When op-amp 402 (Fig. 4) is saturated, operating point 210 lies along one of the two positive sloped segments 216, 218. When op-amp 402 is operating linearly, the operating point lies along the negative sloped segment. When the operating point is on the negative sloped segment 214, oscillatory behavior will be
 5 observed at the output V_{out} of circuit 400. Hence the negative sloped segment is said to lie in unstable region 204 as is operating point 210. When the operating point 210', 210'' is on a positive sloped segment, a non-oscillatory output is observed. Hence the positive segments are said to lie in stable regions 206, 208.

The operating point 210 can be moved along the transfer function by
 10 changing the output V_s of function generator 310 as it is applied to the input of circuit 400. In particular, the operating point can be moved into unstable region 204 when an enable signal is provided by the function generator. Conversely, the operating point can be moved out of the unstable region and into one of the stable regions 206, 208 by the application of a disable signal. The resulting behavior of circuit 400 is that of a gated
 15 oscillator.

Fig. 6 shows yet another embodiment of the gated oscillator of the invention. As in the foregoing figures, a function generator 310 provide a variable voltage signal V_s . This signal feeds through inductor 410 into a first inverter 602. The output of inverter 602 is coupled to a second inverter 604. The output of inverter 604 is
 20 taken across resistor 608 to provide output V_{out} . A feedback path from the output of inverter 604 to the input of inverter 602 is provided via resistor 606.

Referring now to Fig. 7, an oscilloscope trace is shown, illustrating the foregoing described behavior. Trace 1 is the output V_s of function generator 310 as applied to the input of circuit 400. A first portion of the trace constitutes the ENABLE
 25 signal. This is followed by a second portion which constitutes the DISABLE signal. Preferably, the function generator output is a digital waveform. For example, a typical digital waveform is a square wave such as shown in Fig. 7. It is noted that typically, the digital waveform will be asymmetric along the time axis, since the periods of ON time and OFF time will depend on the nature of the particular application of the gated
 30 oscillator.

Trace 2 is the output voltage V_{out} of circuit 400. As can be seen, the circuit begins to oscillate when an enable signal is received. The oscillations continue for the duration of the enable signal. It can be further seen that the first period T_1 of the first

cycle has the same duration as each of the remaining cycles, T_2 . The pulse width can be varied by changing the circuit parameters R_f , R_1 , and R_2 or the op-amp DC bias V_{CC} . When the disable signal is received, the circuit stops oscillating instantaneously.

5 The location of the operating point along the transfer curve in the unstable region affects the period of oscillations of the output of circuit 400. The location of the operating point within the unstable region (and the stable regions for that matter) can be determined by adjusting the level of the forcing function. It can be seen, therefore, that different oscillation periods can be attained from circuit 400 by applying an enable signal of different levels. The gated oscillator of the invention can thus be made to produce
10 different pulse widths by the use of a function generator in which the level of the enable signal can be controlled.

The invention described herein uses an unconventional method of controlling the operating point of a VdP oscillator to provide a significantly simplified digital circuit design which obviates the need for a clock circuit. The inventive circuit
15 does not need additional supporting components. The invention obviates the need for a charging and a discharging capacitor for generating pulses. The invention dispenses with the support circuitry conventionally required to maintain capacitor potential when oscillation is stopped.

The invention requires only that an enabling signal be provided to "force"
20 the VdP oscillator to oscillate and a disabling signal to stop oscillations. These signals can be readily generated by any of a number of known circuit designs.

The inventive gated oscillator circuit is advantageous in that its oscillations start and stop substantially instantaneously. Consequently, there are no transients between the ON and OFF state of the oscillator. Another advantage is that the period of
25 the first cycle of oscillation during an ON period is the same as the subsequent cycles during that ON period.

Another advantage is that the circuit does not require any external free running oscillator. The circuit will generate its own oscillations when triggered by an enable signal. Consequently, this allows for significant reductions in power consumption
30 in digital circuit applications. This is especially advantageous given the low power requirements of many of today's digital applications.

Yet another advantage, the circuit is inherently synchronized with the enable signal. By tuning the circuit parameter, without changing the circuit configuration, the duty cycle and the frequency of oscillation can be varied. The gated

oscillation at the output of the circuit does not overlap with the enable signal and therefore no additional circuitry is required to separate the signals, thus realizing a simplification in the gated oscillator circuitry.

WHAT IS CLAIMED IS:

- 1 1. A method for providing pulses in a digital circuit comprising steps
2 of:
3 providing a digital circuit; and
4 providing a clocking circuit, said clocking circuit coupled to said digital
5 circuit,
6 said clocking circuit having an input terminal and an output terminal, said
7 circuit further having a variable operating point, said circuit further having a transfer
8 function characterized by having an unstable operating region bounded by a first stable
9 operating region and a second stable operating region so that said circuit produces
10 oscillatory output when said operating point is varied into said unstable region and said
11 circuit has a non-oscillatory output when said operating point is varied into either of said
12 first and second stable regions;
13 forcing said operating point into said unstable region to initiate operation
14 of said circuit to produce at least one oscillation; and
15 forcing said operating point to vary into either one of said stable operating
16 regions in order to terminate said at least one oscillation without transient effects.
- 1 2. The method according to claim 1 wherein said step of forcing
2 includes applying a forcing function to said input of said circuit, said forcing function
3 having a first output level and a second output level, said circuit characterized in that said
4 operating point is located in said unstable region when said forcing function produces
5 said first output level, said circuit further characterized in that said operating point is
6 located in one of said stable regions when said forcing function produces said second
7 output level.
- 1 3. The method of claim 2 wherein said forcing function produces a
2 third output level, said circuit characterized in that said operating point is located in a part
3 of said unstable region, when said forcing function produces said third output level, that is
4 different from the location of said operating point when said forcing function produces
5 said first output level.
- 1 4. The method of claim 1 wherein said forcing function is
2 asymmetrical along a time axis.

1 5. The method of claim 1 wherein said forcing function is cyclical.

1 6. The method of claim 1 wherein said forcing function is a square
2 wave.

1 7. The method according to claim 1 wherein said circuit includes an
2 operational amplifier circuit with feedback, said circuit having a series input through an
3 inductor, wherein said unstable operating region is a negative resistance region, and
4 wherein said operating point is forced into said unstable region by a changing voltage
5 applied to said inductor.

1 8. The method according to claim 1 wherein said circuit includes an
2 element having negative impedance, said circuit having a series input through an
3 inductor, wherein said unstable operating region is a negative impedance region, and
4 wherein said operating point is forced into said unstable region by a changing current
5 applied through said inductor.

1 9. The method according to claim 8 wherein said element is a tunnel
2 diode.

1 10. In a digital circuit, a clocking circuit, comprising:
2 a circuit having an input and an output, said circuit having a transfer
3 function, said transfer function having an unstable operating region bounded by a first
4 stable operating region and by a second stable operating region, said transfer function
5 defining a set of operating points of said circuit, said circuit adapted to produce
6 oscillatory output when said operating point is varied into said unstable region, said
7 circuit further adapted to produce a non-oscillatory output when said operating point is
8 varied into either of said first and second stable regions; and

9 a function generator having an output adapted to selectively produce an
10 output of a first level and an output of a second level, said function generator output
11 coupled to said circuit input;

12 said operating point is forced into said unstable region when said function
13 generator output is at said first level;

14 said circuit further adapted so that said operating point is forced to said
15 stable region when said function generator output is at said second level.

1 11. The digital circuit according to claim 10 wherein said function
2 generator produces an output of a third level; said operating point is forced into said
3 unstable region when said function generator output is at said third level; said operating
4 point being located in said unstable region based on whether said function generator
5 output is at said first level or said third level.

1 12. The digital circuit according to claim 10 wherein said function
2 generator produces a cyclical output.

1 13. The digital circuit of claim 10 wherein said function generator
2 output produces a square wave.

1 14. The digital circuit of claim 10 wherein said function generator
2 output has an asymmetrical shape.

1 15. The digital circuit according to claim 10 wherein said circuit
2 includes a negative impedance element, wherein said unstable operating region is a
3 negative impedance region, and wherein said operating point is forced into said unstable
4 region by a time varying input signal.

1 16. The digital circuit according to claim 10 wherein said circuit
2 includes a negative impedance element, said circuit having a series input through an
3 inductor, wherein said unstable operating region is a negative impedance region, and
4 wherein said operating point is forced into said unstable region by a changing current
5 applied through said inductor.

1 17. The digital circuit of claim 16 wherein said element is a tunnel
2 diode.

1 18. A method for providing clocking pulses, comprising:
2 providing a circuit having an input terminal and an output terminal, said
3 circuit further having a variable operating point, said circuit further having a transfer
4 function characterized by having an unstable operating region bounded by a first stable
5 operating region and a second stable operating region so that said circuit produces
6 oscillatory output when said operating point is varied into said unstable region and said

7 circuit has a non-oscillatory output when said operating point is varied into either of said
8 first and second stable regions;
9 forcing said operating point into said unstable region to initiate operation
10 of said circuit to produce at least one oscillation; and
11 forcing said operating point to vary into either one of said stable operating
12 regions in order to terminate said at least one oscillation without transient effects.

1 19. The method according to claim 18 wherein said step of forcing
2 includes applying a forcing function to said input of said circuit, said forcing function
3 having a first output level and a second output level, said circuit characterized in that said
4 operating point is located in said unstable region when said forcing function produces
5 said first output level, said circuit further characterized in that said operating point is
6 located in one of said stable regions when said forcing function produces said second
7 output level.

1 20. The method of claim 19 wherein said forcing function produces a
2 third output level, said circuit characterized in that said operating point is located in a part
3 of said unstable region, when said forcing function produces said third output level, that is
4 different from the location of said operating point when said forcing function produces
5 said first output level.

1 21. The method according to claim 18 wherein said circuit includes an
2 operational amplifier circuit with feedback, said circuit having a series input through an
3 inductor, wherein said unstable operating region is a negative resistance region, and
4 wherein said operating point is forced into said unstable region by a changing voltage
5 applied to said inductor.

1 22. The method according to claim 18 wherein said circuit includes an
2 element having negative impedance, said circuit having a series input through an
3 inductor, wherein said unstable operating region is a negative impedance region, and
4 wherein said operating point is forced into said unstable region by a changing current
5 applied through said inductor.

1 23. A gated oscillator circuit, comprising:
2 a circuit having an input and an output, said circuit having a transfer
3 function, said transfer function having an unstable operating region bounded by a first

4 stable operating region and by a second stable operating region, said transfer function
5 defining a set of operating points of said circuit, said circuit adapted to produce
6 oscillatory output when said operating point is varied into said unstable region, said
7 circuit further adapted to produce a non-oscillatory output when said operating point is
8 varied into either of said first and second stable regions; and
9 a function generator having an output adapted to selectively produce an
10 output of a first level and an output of a second level, said function generator output
11 coupled to said circuit input;
12 said operating point is forced into said unstable region when said function
13 generator output is at said first level;
14 said circuit further adapted so that said operating point is forced to said
15 stable region when said function generator output is at said second level.

1 24. The gated oscillator according to claim 23 wherein said function
2 generator produces an output of a third level; said operating point is forced into said
3 unstable region when said function generator output is at said third level; said operating
4 point being located in said unstable region based on whether said function generator
5 output is at said first level or said third level.

1 25. The gated oscillator according to claim 23 wherein said circuit
2 includes a negative impedance element, wherein said unstable operating region is a
3 negative impedance region, and wherein said operating point is forced into said unstable
4 region by a time varying input signal.

1 26. The gated oscillator according to claim 23 wherein said circuit
2 includes a negative impedance element, said circuit having a series input through an
3 inductor, wherein said unstable operating region is a negative impedance region, and
4 wherein said operating point is forced into said unstable region by a changing current
5 applied through said inductor.