Claims

1. Apparatus for inspecting Z height and profile of overlapping bonding wires on multi stacked dies or like article, comprising:

an imaging device mounted on a means capable of moving in the X, Y & Z axis coupled with encoders, to capture images of focused points on overlapping bonding wires and their respective X, Y & Z positions, at different planes;

the imaging device optically coupled with a lens having a pre-determined focal depth;

a processor associated with the imaging device configured to analyse the captured images and calculate heights, and lateral displacement of the focused points on the overlapping bonding wires and linearly interpolate each point to their neighbouring point to form an angular profile of the overlapping bonding wires;

a strobed illuminating means having a pre-determined angle to enable image capture of illuminated overlapping bonding wires to eliminate image noise of closely placed overlapping bonded wires;

a second illumination means mounted on a pedestal to illuminate the overlapping bonding wires under inspection to enable capturing of a backlit image.

2. An apparatus of claim 1 further comprising a third illuminating means that creates a dark area behind the area of interest viewed by the imaging device;

3. An apparatus of claim 1 further comprising a liquid lens to enable high speed focussing, coupled to the image capturing device.

4. A method for measuring Z height and profile of wires bonded between pads of two or more stacked semiconductor chips and a substrate, said method comprising the steps of:

moving an image capturing system in X, Y & Z directions to focus said image capturing system onto pre-set multiple points on the bonded wires;

capturing images of said multiple points on the bonding wires in multiple Z axis planes using strobed illumination;

reading encoder positions of every point on the set of bonding wires and tabulating their respective X Y & Z points;

calculating heights, and lateral displacement of said tabulated points of the bonding wires around the stacked semiconductor chips and linearly interpolating each point to their neighbouring point to form an angular profile of the bonding wires;

plotting a 3D graph using said tabulated points.

analysing the 3D graph to detect bonding wires in close proximity in the XY or Z position and comparing them with pre-set parameters for rejecting or accepting a bonded multi stacked die;

communicating results and analysed parameters to an external interface.

5. The method of according to claim 4 further comprising analysing the 3D graph to determine a reference plane to arrive at a height of the bonding wires.