MASS SIMULTANEOUS SEALING AND ELECTRICAL CONNECTION OF ELECTRONIC DEVICES

ABSTRACT

The present invention provides a new and effective method for the sealing and electrical testing of electronic devices; and particularly for surface acoustic wave devices. In accordance with the present invention, the cost and size of making hermetically sealed packages for electronic devices and of electrically testing each device is significantly reduced over the prior art by making use of mass simultaneous sealing and electrical connection at the wafer level, and by using substrates with hermetically sealed and electrically conductive via holes. Further, cost reduction is effected by making use of final electrical testing with wafer probe test techniques before dicing.