

ABSTRACT

An image processing device includes a multimedia intellectual (IP) block which processes image data; a memory; and a frame buffer compressor (FBC) which compresses the image data to generate compressed data and stores the compressed data in the memory. The frame buffer compressor includes a logic circuit which determines a combination of a quantization parameter (QP) table and an entropy table and controls compression of the image data based on the determined combination of the QP table and the entropy table.

FIG. 1