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(71) Applicant: MICRON TECHNOLOGY, INC. [US/US];
8000 S. Federal Way, Boise, Idaho 83706 (US).

(72) Inventors; and

(75) Inventors/Applicants (for US only): HWANG, David, K.
[US/US]; 3454 S. Shortleaf Avenue, Boise, Idaho 83716
(US). PAREKH, Kunal [US/US]; 677 N. Morningside
Way, Boise, Idaho 83712 (US). WILLETT, Michael
[US/US]; 3916 E. Immigrant Pass Ct., Boise, Idaho 83702
(US). TRIVEDI, Jigish [IN/US]; 750 S. Granite Way,
Boise, Idaho 83712 (US). MATHEW, Suraj [IN/US];
2832 East Red Fir Court, Boise, Idaho 83716 (US). PE-
TERSON, Greg [US/US]; 2220 Stewart Avenue, Nampa,
Idaho 83686 (US).

(74) Agent: AMERSON, Mike, J.; 10333 Richmond, Suite
1100, Houston, Texas 77042 (US).

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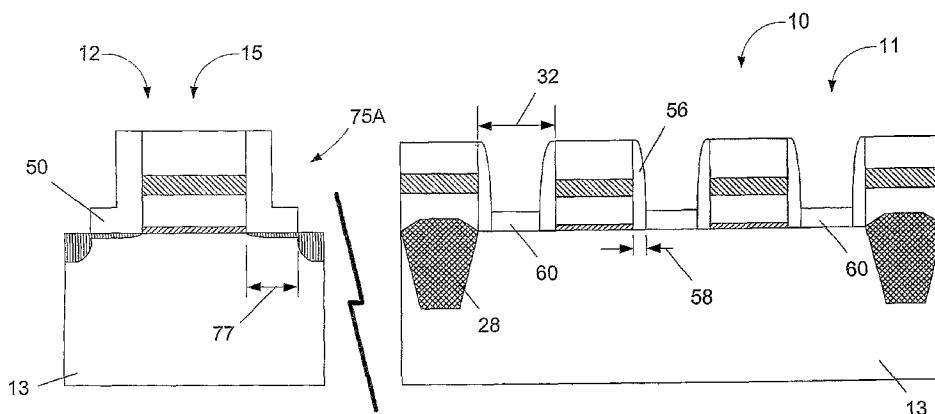
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(54) Title: SIDEWALL SPACERS ON A MEMORY DEVICE



(57) Abstract: The present invention is generally directed to a method of manufacturing sidewall spacers on a memory device, and a memory device comprising such sidewall spacers. In one illustrative embodiment, the method includes forming sidewall spacers on a memory device comprised of a memory array and at least one peripheral circuit by forming a first sidewall spacer adjacent a word line structure in the memory array, the first sidewall spacer having a first thickness and forming a second sidewall spacer adjacent a transistor structure in the peripheral circuit, the second sidewall spacer having a second thickness that is greater than the first thickness, wherein the first and second sidewall spacers comprise material from a single layer of spacer material. In one illustrative embodiment, the device includes a memory array comprised of a plurality of word line structures, each of the plurality of word line structures having a first sidewall spacer formed adjacent thereto, the first sidewall spacer having a first thickness, and a peripheral circuit comprised of at least one transistor having a second sidewall spacer formed adjacent thereto, the second sidewall spacer having a second thickness that is greater than the first thickness, the first and second sidewall spacers comprised of a material from a single layer of spacer material.



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