Abstract

ULTRA-LOW SHEET RESISTANCE METAL/POLY-SI GATE FOR DEEP SUB-MICRON CMOS APPLICATION

A method for fabricating a deep sub-micron gate electrode, comprising polysilicon and metal, having ultra-low sheet resistance. The process begins by forming shallow trench isolation regions 14 in a silicon substrate 10. A gate oxide layer is formed on device areas. A doped blanket polysilicon layer 16 is formed on the gate oxide layer. A cap layer 20 composed of silicon nitride is formed on the polysilicon layer 16. The cap layer 20 and the polysilicon layer 16 are patterned by photoresist masking and anisotropic etching to form a bottom gate electrode 16A and a gate cap 20A. Lightly doped source/drain areas 22 are formed adjacent to the gate bottom electrodes 16A by ion implantation. Sidewall spacers 21 are formed on the gate electrode 16A and gate cap 20A. Source/drain regions 24 are formed by ion implantation adjacent to said sidewall spacers 21. A metal silicide 23 is formed on the source/drain regions 24. An interlevel dielectric layer (ILD) 28 is deposited and planarized by CMP using the gate cap 20A as a CMP stop. The gate cap 20 is selectively removed. A barrier layer 32 composed of a TaN, CoWP, TiN or W_xN_y is formed over the planarized IDL 28A. A top gate layer 36 composed of copper or tungsten is formed on the barrier layer 32. The top gate layer 36 and the barrier layer 32 are removed down to the level of the top of the ILD 28 using CMP; thereby forming a top gate electrode. A passivation layer 40, composed of Pd or NiP is selectively deposited over the gate top electrode 36A.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)