ABSTRACT

Disclosed are techniques that teach the replacement of the typical organic, plastic, or ceramic package substrate used in semiconductor package devices with a low-CTE package substrate. In or embodiment, a semiconductor device implementing the disclosed techniques is provided, where the device comprises an integrated circuit chip having at least one coupling component formed on an exterior surface thereof. Also, the device includes a package substrate having a mounting surface with bonding pads that are configured to receive the at least one coupling component. In such embodiments, the package substrate is selected or manufactured such that it has a coefficient of thermal expansion in a direction perpendicular to its mounting surface that is less than approximate twice a coefficient of thermal expansion along a plane parallel to its mounting surface.

Figure 1