

PATENT SPECIFICATION

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(54) MANUFACTURE OF SEMICONDUCTOR DEVICES

(71) We, PHILIPS ELECTRONIC AND ASSOCIATED INDUSTRIES LIMITED, of Abacus House, 33 Gutter Lane, London EC2V 8AH, a British Company, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to a semiconductor device and to a method of manufacturing a semiconductor device.

According to a first aspect of the invention there is provided a semiconductor device having a semiconductor body comprising a silicon epitaxial layer on a semiconductor substrate, regions of one or more semiconductor circuit elements being present in semiconductor parts of the epitaxial layer, which epitaxial-layer parts are separated laterally in the layer by oxidized parts of the epitaxial layer, which oxidized parts form parts of an oxide layer pattern sunk over at least part of its thickness in the semiconductor body, and at least one zone of opposite conductivity type to the substrate being present partly in the substrate, which zone extends across the whole bottom of at least one of the said epitaxial-layer parts, adjoins the sunken oxide layer pattern around this epitaxial-layer part, forms a *p-n* junction with the bulk of the substrate, and has such a high doping concentration that the formation of undesirable channels adjoining the sunken oxide layer pattern is prevented.

According to a second aspect of the invention there is provided a method of manufacturing a semiconductor device comprising providing a silicon epitaxial layer on a semiconductor substrate to form a semiconductor body, and subjecting the epitaxial layer to an oxidation treatment while locally masking the surface of the

epitaxial layer against oxidation and so causing an oxide of silicon to grow into the unmasked silicon until the grown oxide forms a layer pattern which is sunk over at least part of its thickness in the semiconductor body for mutually separating parts of the epitaxial layer, in which epitaxial-layer parts regions of one or more circuit elements are to be or are provided, in which method at least one zone of opposite conductivity type to the substrate is provided partly in the substrate to extend across the whole bottom of at least one of the said epitaxial-layer parts, adjoins the sunken oxide layer pattern around this epitaxial-layer part, forms a *p-n* junction with the bulk of the substrate, and has such a high doping concentration that the formation of undesirable channels adjoining the sunken oxide layer pattern is prevented.

An embodiment of the present invention will now be described with reference to Figures 1 and 2 of the accompanying diagrammatic drawings, in which:—

Figure 1 is a cross-sectional view of part of a semiconductor device shown at a stage in manufacture and,

Figure 2 is a cross-sectional view at an earlier stage in manufacture.

The semiconductor device whose manufacture is illustrated in the accompanying drawings has a semiconductor body comprising a silicon epitaxial layer 61 on a semiconductor substrate 68. Regions of one or more semiconductor circuit elements are provided in semiconductor parts such as the part 69 of the epitaxial layer 61. These epitaxial-layer parts are separated laterally in the layer by oxidized parts 65 of the epitaxial layer 61. These oxidized parts 65 form parts of an oxide layer pattern sunk over at least part of its thickness in the semiconductor body. At least one zone 62 of opposite conductivity type to the substrate

68 is present partly in the substrate 68 which zone extends across the whole bottom of at least one of the said epitaxial-layer parts 69, adjoins the sunken oxide layer pattern 65 around this epitaxial-layer part 69, forms a *p-n* junction with the bulk of the substrate 68, and has such a high doping concentration that the formation of undesirable channels adjoining the sunken oxide layer pattern 65 is prevented.

In the present embodiment, the starting material is a semiconductor substrate body 68, which is entirely of the same conductivity type in the epitaxial layer 61 to be provided thereon. The semiconductor body 68 is formed, for example, by an *n*-type silicon crystal, the resistivity of which generally is not critical and in this case is, for example, from 2 to 5 ohm-cm.

The semiconductor body 68 is provided with the highly doped *p*-type surface zones 62 adjacent the surface 66 where the epitaxial layer 61 is to be provided. The surface zones can be obtained, for example, by diffusion of boron, the surface concentration being approximately 10^{19} boron atoms per ccm.

In the present embodiment the surface zones 62 are interrupted at the area of the oxide layer pattern 65 to be provided, as is clearly shown in Figures 1 and 2. Proceeding from one separate epitaxial-layer part 69 of the semiconductor device *via* the semiconductor material to another, at least four *p-n* junctions are passed, two successive *p-n* junctions each time forming a pair of diodes arranged in opposition. By this structure, for example, the capacitive coupling between the separate epitaxial-layer parts can be kept small.

After providing the surface zones 62, the *n*-type epitaxial layer 61 is provided in known manner by vapour-depositing semiconductor material on the substrate 68. The oxide layer pattern 65 is subsequently provided by local oxidation.

For the oxidation treatment to form the pattern 65, the epitaxial layer 61 is provided with a masking layer which masks against oxidation. The masking layer may consist of silicon nitride, but may also consist, for example, of a double layer of silicon-oxide and silicon-nitride. The silicon-nitride layer is provided in normal manner, for example, by heating the body (61, 68) at a temperature of approximately 1000°C in a gas mixture of SiH_4 and NH_3 , and has a thickness of approximately $0.2\text{ }\mu\text{m}$, which thickness is considerably smaller than that of the pattern 65 to be provided. By means of a photolithographic process a part of the masking layer is removed so as to be able to provide the pattern 65.

In order to obtain a pattern 65 which is inset substantially throughout its thickness in

the silicon layer 61, the layer masking against oxidation is used as an etching mask prior to starting the oxidation treatment to remove the silicon layer 61 locally over approximately half its thickness by etching in a known manner.

By passing steam at a pressure of approximately 1 atmosphere and at a temperature of approximately $1,000^{\circ}\text{C}$, the pattern 65 is obtained by oxidation of the layer 61 where not masked by the masking layer. The oxidation treatment is continued until the resulting pattern 65 reaches at least down to the surface zone 62 and the substrate 68.

The epitaxial layer 61 is thus divided in a simple and efficacious manner into parts such as 69 which are insulated and separated from each other by the pattern 65. Since the pattern 65 is inset substantially throughout its thickness in the layer 61, the resulting configuration can be treated further by means of planar methods; in addition the pattern 65 consists of silicon oxide of a good quality. The highly doped zone 62 prevents undesirable channel formation adjacent the pattern 65.

In a modified form of the method the oxidation treatment may be interrupted and during this interruption the silicon oxide layer already obtained may be removed at least over part of its thickness by etching, the oxidation-masking layer being used as an etching mask. An etching treatment preceding the oxidation treatment is not necessary in this case. It is also possible to use no etching treatment at all. In that case, however, a pattern 65 is obtained which projects above the surface of the epitaxial layer 61. Particularly in the case of very thin epitaxial layers, this simplification of the method may be used without any objection. In other cases, the part of the pattern projecting above the epitaxial layer 61 may also be removed by an etching treatment afterwards, the oxidation-masking layer serving as an etching mask. It is possible for the pattern 65 to project slightly above the surface of the epitaxial layer 61 or to remain slightly below said surface.

After the formation of the pattern 65, zones of circuit elements, for example, transistors, diodes, resistors or capacitors, can be provided in the epitaxial-layer parts such as 69.

It will be obvious that many variations are possible within the scope of this invention as defined in the appended Claims. For example, the conductivity types of all the mentioned parts of the semiconductor device described may simultaneously be changed from *p*-type conductivity into *n*-type conductivity, and conversely.

Another variation consists in that the epitaxial layer 61 provided throughout the

surface with a surface zone of the opposite conductivity type, as a result of which a matrix structure is obtained of, for example, *p-n-p-n* circuit elements, which structure
 5 may be used, for example, as a photo-sensitive detector and in which the *p-n-p-n* circuit elements have juxtaposed zones present in the epitaxial layer 61 and separated from each other by the layer
 10 pattern of silicon-oxide 65. Thus, the zones 62 may also form circuit-element zones of the device.

In another form, instead of providing a separate zone 62 beneath each separate epitaxial-layer part 69, a single zone 62 may
 15 extend over the substrate surface 66 across the bottom of more than one separate epitaxial-layer part 69 and beneath the oxide layer part 65 therebetween.

20 Instead of diffusion, various zones in the semiconductor device may be provided by ion implantation.

WHAT WE CLAIM IS:—

25 1. A semiconductor device having a semiconductor body comprising a silicon epitaxial layer on a semiconductor substrate, regions of one or more semiconductor circuit elements being present in semiconductor parts of the epitaxial layer,
 30 which epitaxial-layer parts are separated laterally in the layer by oxidized parts of the epitaxial layer, which oxidized parts form parts of an oxide layer pattern sunk over at least part of its thickness in the semi-
 35 conductor body, and at least one zone of opposite conductivity type to the substrate being present partly in the substrate, which zone extends across the whole bottom of at least one of the said epitaxial-layer parts,
 40 adjoins the sunken oxide layer pattern around this epitaxial-layer part, forms a *p-n* junction with the bulk of the substrate, and has such a high doping concentration that the formation of undesirable channels adjoining the sunken oxide layer pattern is prevented.
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2. A semiconductor device as claimed in Claim 1, in which the epitaxial layer is of the same conductivity type as the substrate.

3. A semiconductor device as claimed in Claim 1 or Claim 2, in which the oxide layer pattern extends across the thickness of the epitaxial layer. 50

4. A method of manufacturing a semiconductor device comprising providing a silicon epitaxial layer on a semiconductor substrate to form a semiconductor body, and subjecting the epitaxial layer to an oxidation treatment while locally masking the surface of the epitaxial layer against oxidation and so causing an oxide of silicon to grow into the unmasked silicon until the grown oxide forms a layer pattern which is sunk over at least part of its thickness in the semiconductor body for mutually separating parts of the epitaxial layer, in which epitaxial-layer parts regions of one or more circuit elements are to be or are provided, in which method at least one zone of opposite conductivity type to the substrate is provided partly in the substrate to extend across the whole bottom of at least one of the said epitaxial-layer parts, adjoins the sunken oxide layer pattern around this epitaxial-layer part, forms a *p-n* junction with the bulk of the substrate, and has such a high doping concentration that the formation of undesirable channels adjoining the sunken oxide layer pattern is prevented. 55 60 65 70 75

5. A method as claimed in Claim 4, in which the epitaxial layer provided on the substrate is of the same conductivity type as the substrate. 80

6. A method as claimed in Claim 4 or Claim 5, in which the oxide layer pattern is sunk to extend across the thickness of the epitaxial layer. 85

7. A method of manufacturing a semiconductor device, substantially as herein described with reference to Figures 1 and 2 of the accompanying drawings. 90

8. A semiconductor device manufactured by a method claimed in any of Claims 4 to 7.

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surface with a surface zone of the opposite conductivity type, as a result of which a matrix structure is obtained of, for example, *p-n-p-n* circuit elements, which structure may be used, for example, as a photo-sensitive detector and in which the *p-n-p-n* circuit elements have juxtaposed zones present in the epitaxial layer 61 and separated from each other by the layer pattern of silicon-oxide 65. Thus, the zones 62 may also form circuit-element zones of the device.

In another form, instead of providing a separate zone 62 beneath each separate epitaxial-layer part 69, a single zone 62 may extend over the substrate surface 66 across the bottom of more than one separate epitaxial-layer part 69 and beneath the oxide layer part 65 therebetween.

Instead of diffusion, various zones in the semiconductor device may be provided by ion implantation.

WHAT WE CLAIM IS:—

1. A semiconductor device having a semiconductor body comprising a silicon epitaxial layer on a semiconductor substrate, regions of one or more semiconductor circuit elements being present in semiconductor parts of the epitaxial layer, which epitaxial-layer parts are separated laterally in the layer by oxidized parts of the epitaxial layer, which oxidized parts form parts of an oxide layer pattern sunk over at least part of its thickness in the semiconductor body, and at least one zone of opposite conductivity type to the substrate being present partly in the substrate, which zone extends across the whole bottom of at least one of the said epitaxial-layer parts, adjoins the sunken oxide layer pattern around this epitaxial-layer part, forms a *p-n* junction with the bulk of the substrate, and has such a high doping concentration that the formation of undesirable channels adjoining the sunken oxide layer pattern is prevented.

2. A semiconductor device as claimed in Claim 1, in which the epitaxial layer is of the same conductivity type as the substrate.

3. A semiconductor device as claimed in Claim 1 or Claim 2, in which the oxide layer pattern extends across the thickness of the epitaxial layer.

4. A method of manufacturing a semiconductor device comprising providing a silicon epitaxial layer on a semiconductor substrate to form a semiconductor body, and subjecting the epitaxial layer to an oxidation treatment while locally masking the surface of the epitaxial layer against oxidation and so causing an oxide of silicon to grow into the unmasked silicon until the grown oxide forms a layer pattern which is sunk over at least part of its thickness in the semiconductor body for mutually separating parts of the epitaxial layer, in which epitaxial-layer parts regions of one or more circuit elements are to be or are provided, in which method at least one zone of opposite conductivity type to the substrate is provided partly in the substrate to extend across the whole bottom of at least one of the said epitaxial-layer parts, adjoins the sunken oxide layer pattern around this epitaxial-layer part, forms a *p-n* junction with the bulk of the substrate, and has such a high doping concentration that the formation of undesirable channels adjoining the sunken oxide layer pattern is prevented.

5. A method as claimed in Claim 4, in which the epitaxial layer provided on the substrate is of the same conductivity type as the substrate.

6. A method as claimed in Claim 4 or Claim 5, in which the oxide layer pattern is sunk to extend across the thickness of the epitaxial layer.

7. A method of manufacturing a semiconductor device, substantially as herein described with reference to Figures 1 and 2 of the accompanying drawings.

8. A semiconductor device manufactured by a method claimed in any of Claims 4 to 7.

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