

*Fig. 1*

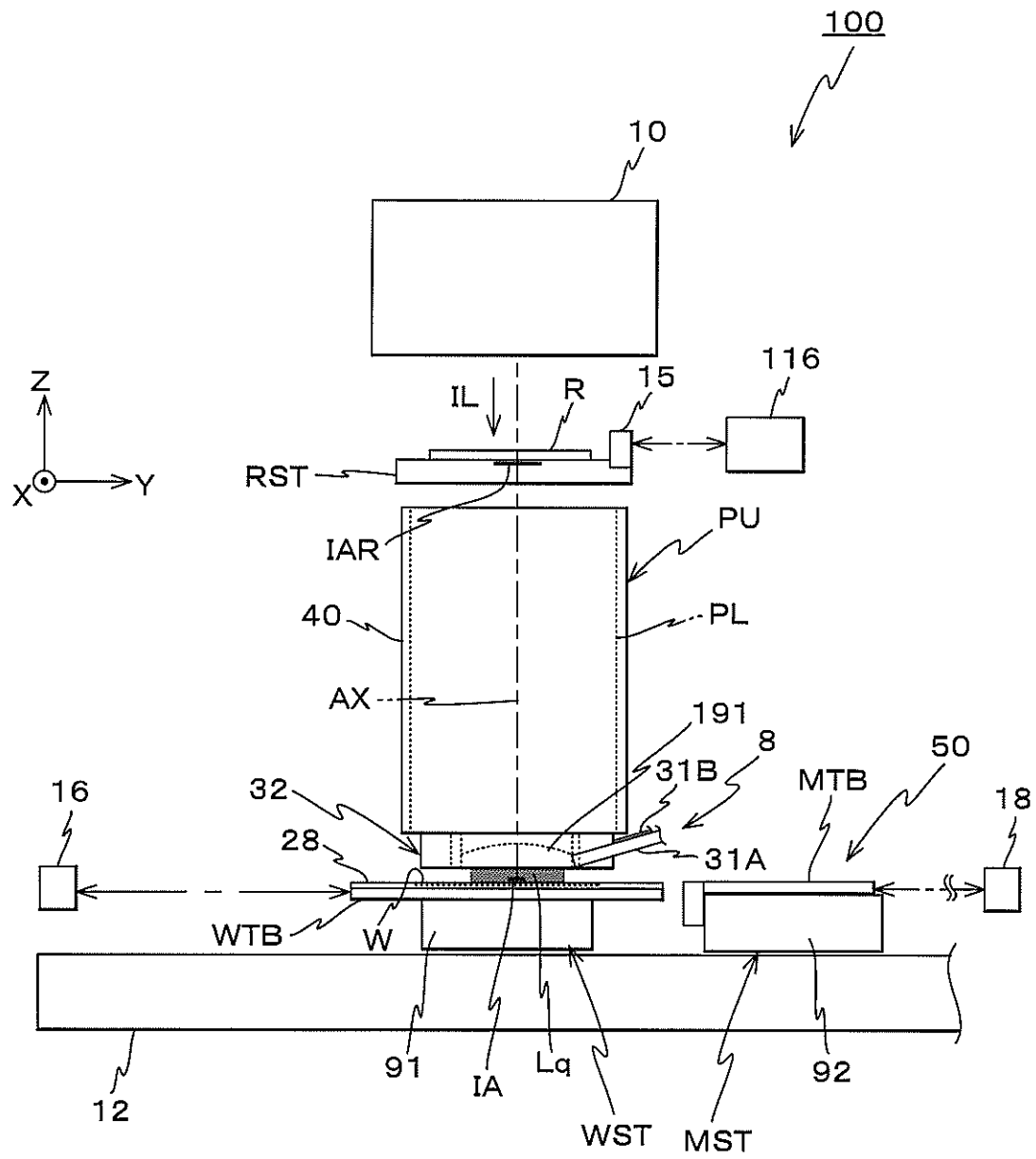
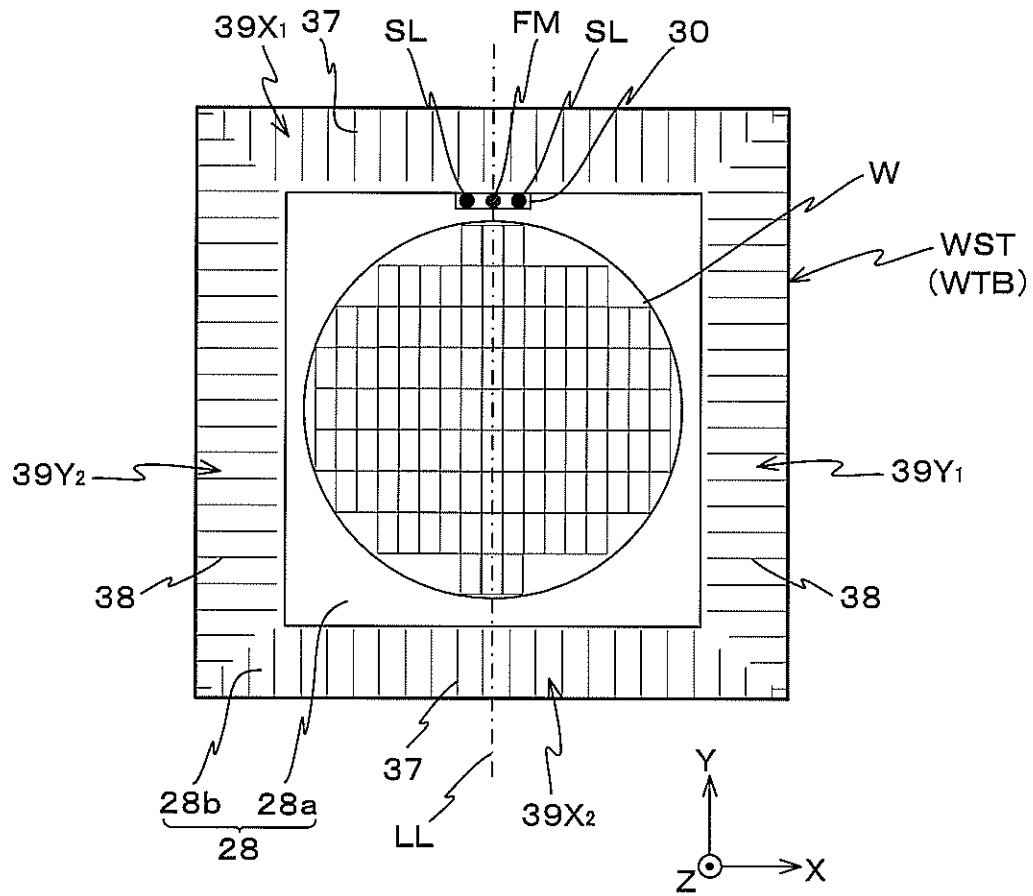
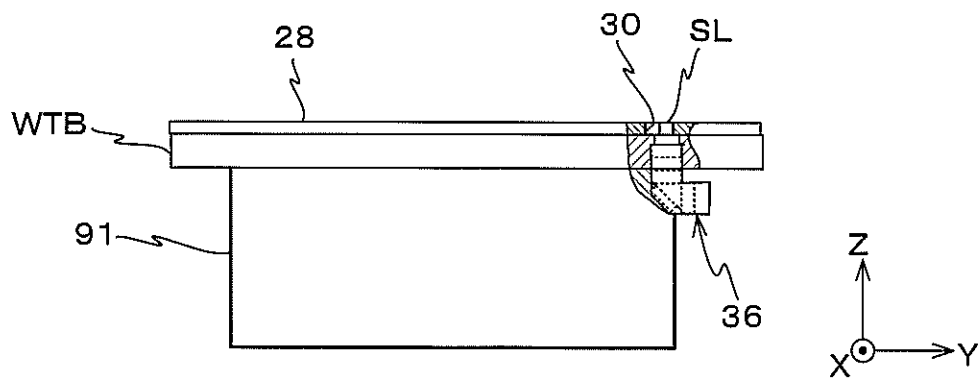
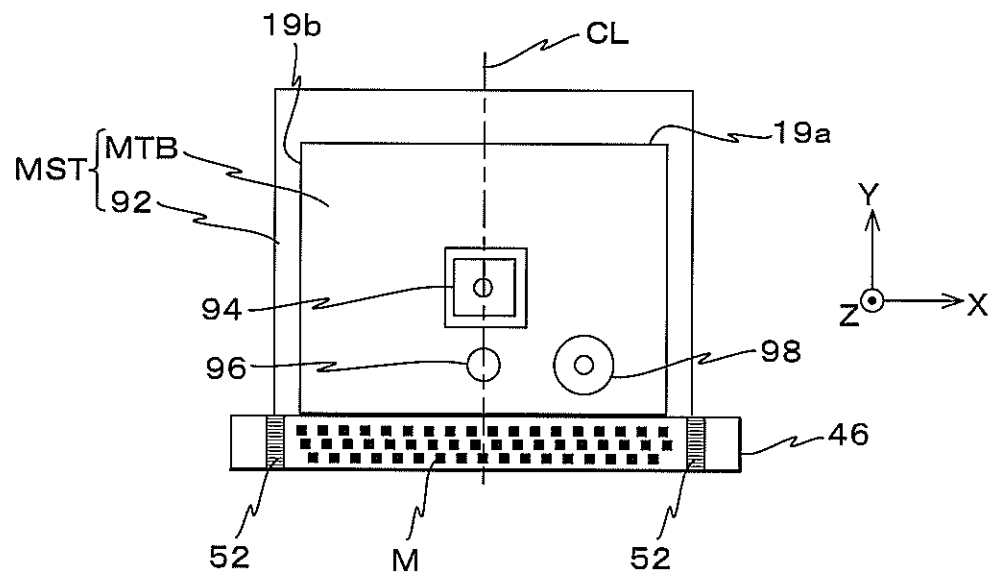
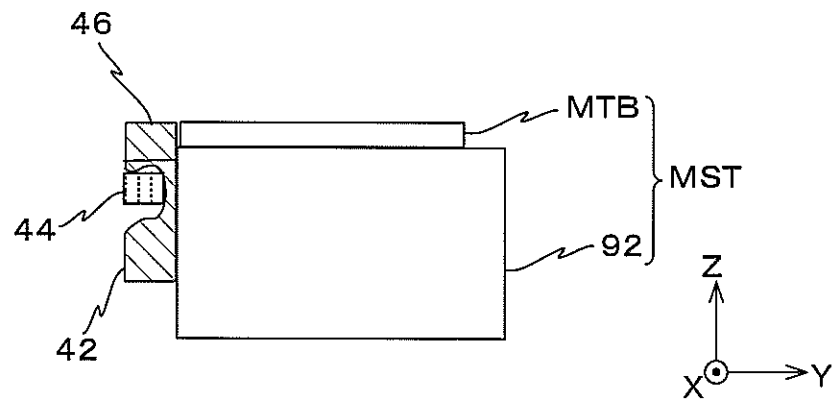
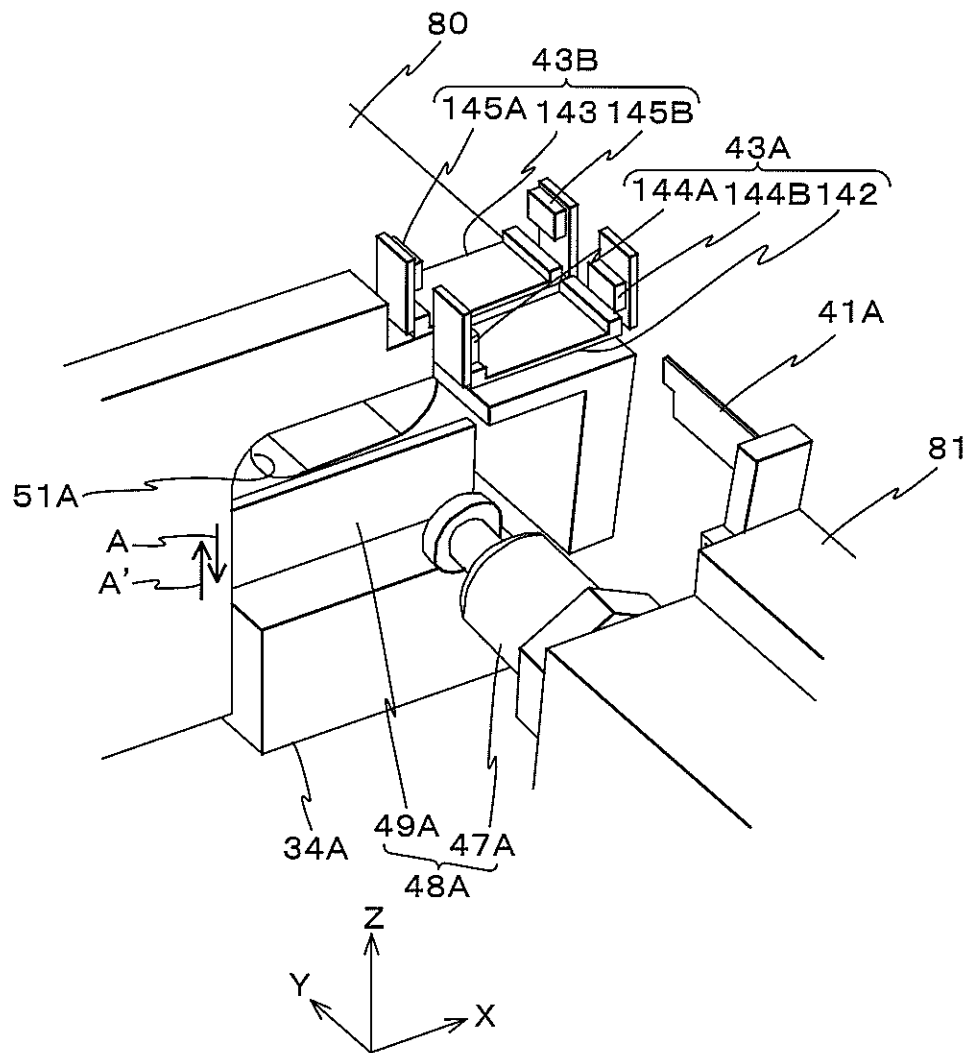


FIG. 1 is a schematic diagram of a semiconductor device in a top-down view. The device includes a central square region with a circular area inside, labeled with various components like WST, W, WTB, and Lq. It is surrounded by a frame with multiple layers and regions labeled with numbers such as 12, 17a, 17b, 41A, 41B, 43A, 43B, 43C, 43D, 47A, 47B, 48A, 48B, 49A, 49B, 51A, 51B, 80, 81, 82, 83, 84, 85, 86, 87, 92, 94, 96, 98, 126, 130, and 18. A coordinate system at the bottom center shows Z pointing up, Y pointing right, and X pointing down.



*Fig. 4A**Fig. 4B*

*Fig. 5A**Fig. 5B*

*Fig. 6*

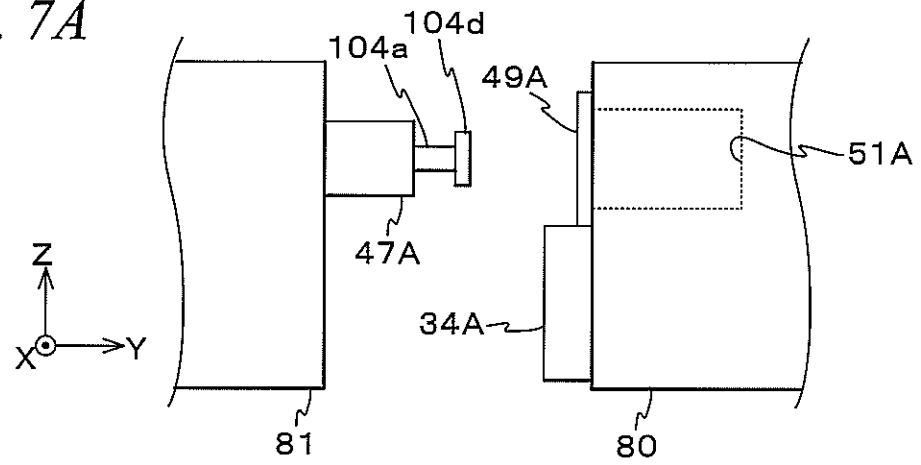
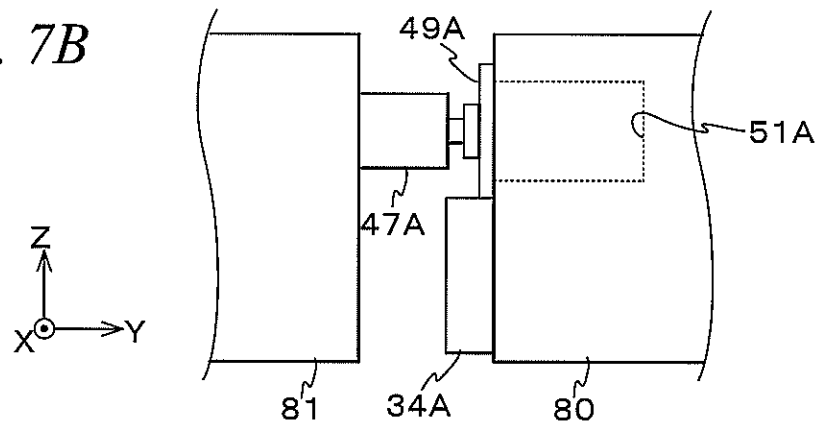
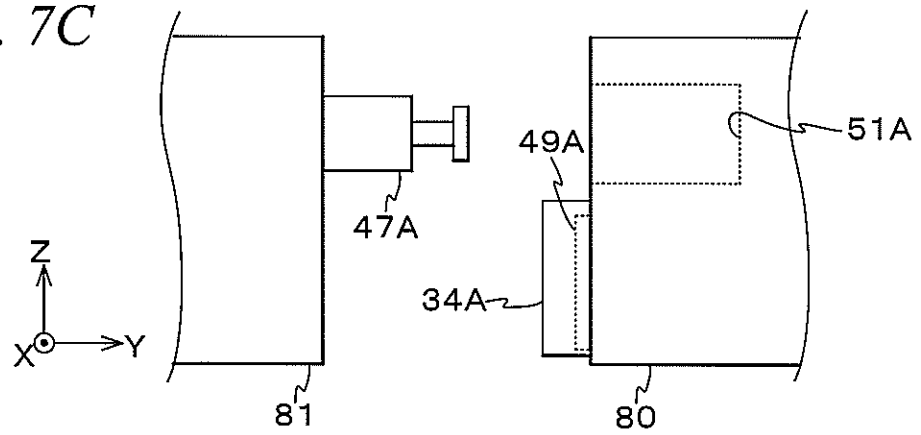
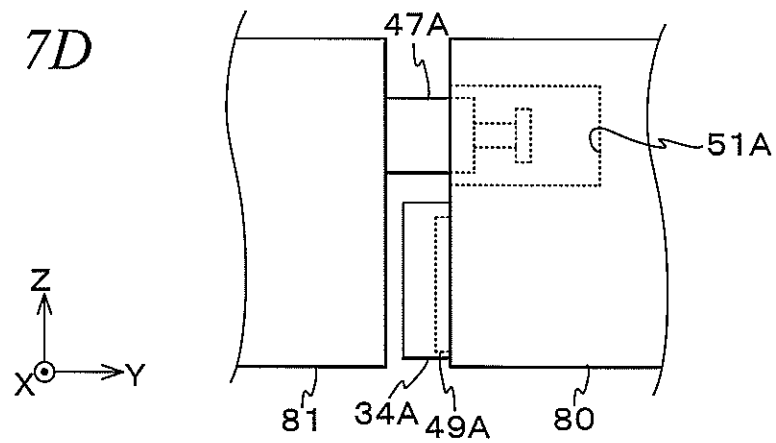
*Fig. 7A**Fig. 7B**Fig. 7C**Fig. 7D*

Fig. 8

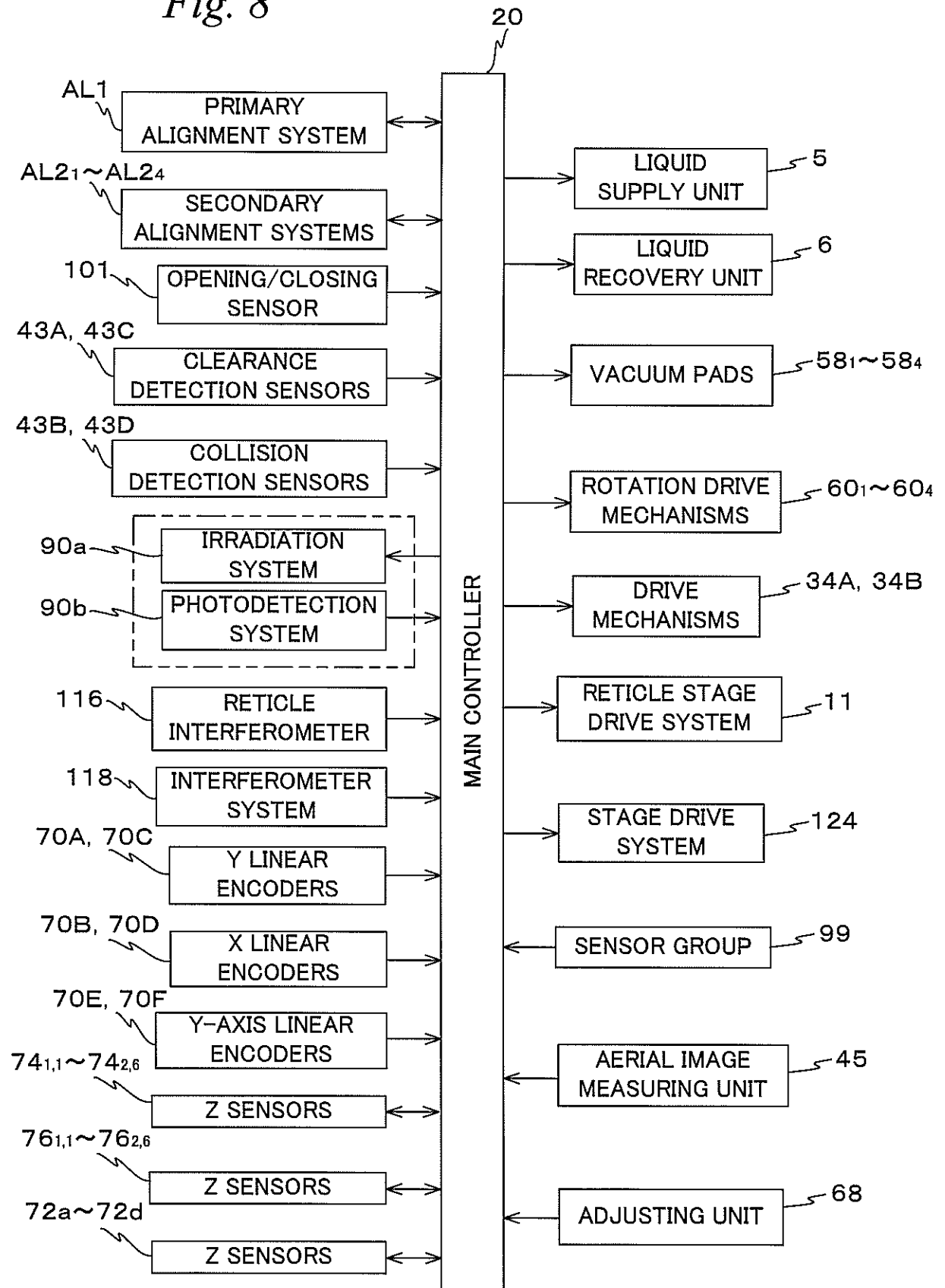


Fig. 9A

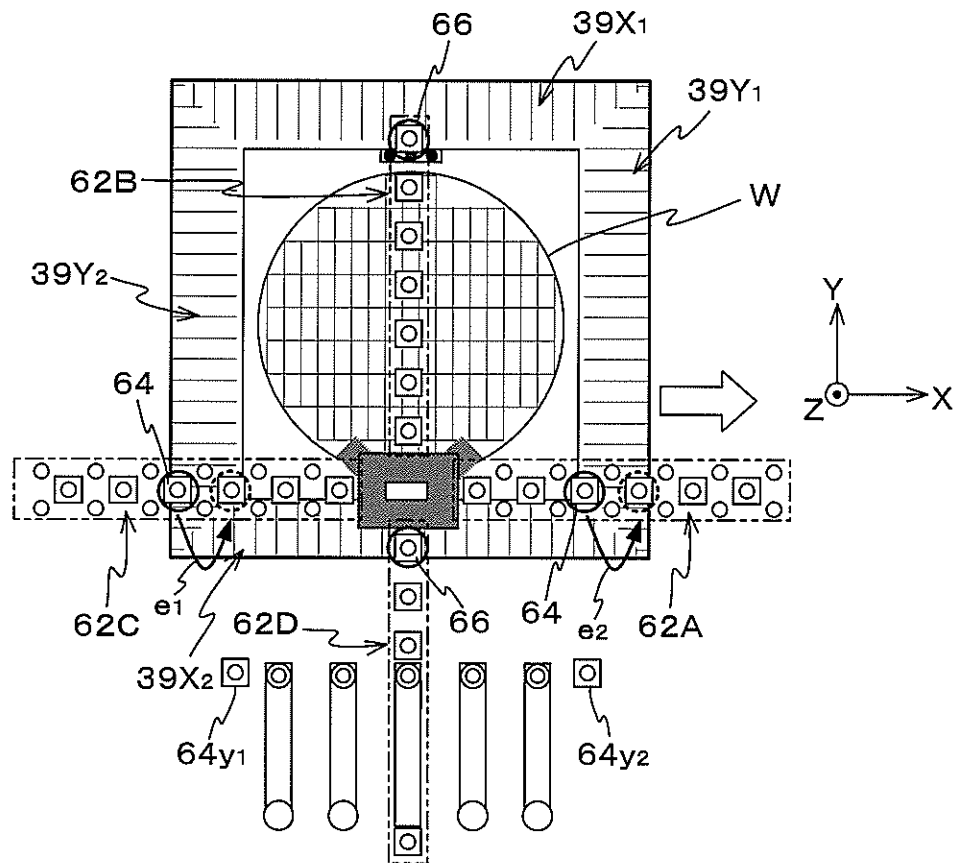
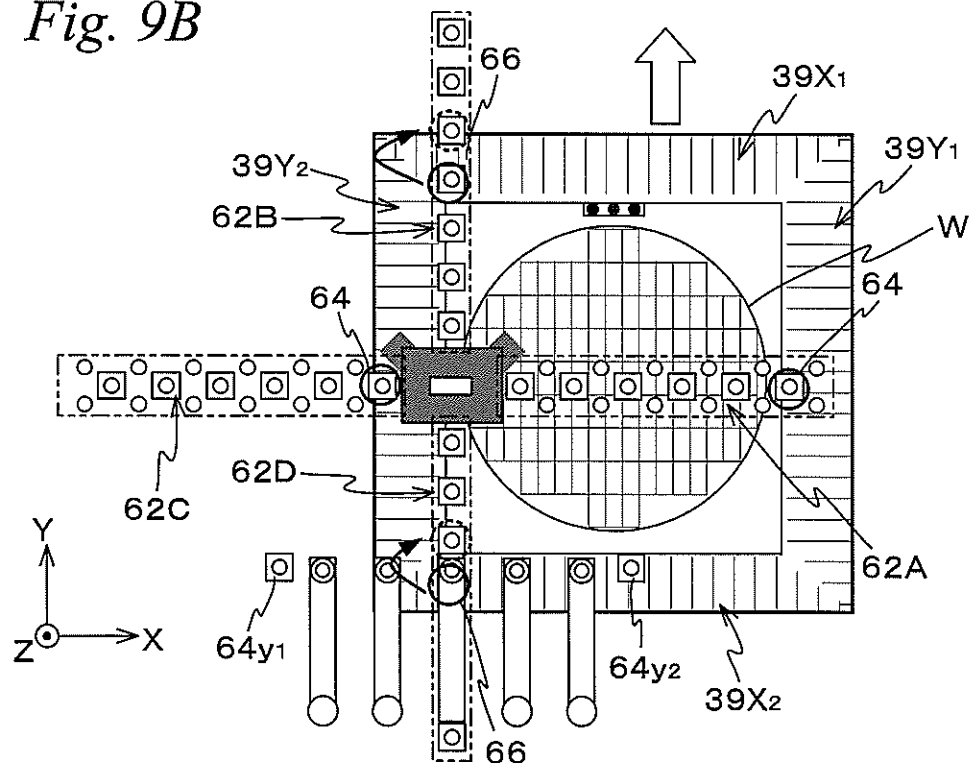


Fig. 9B



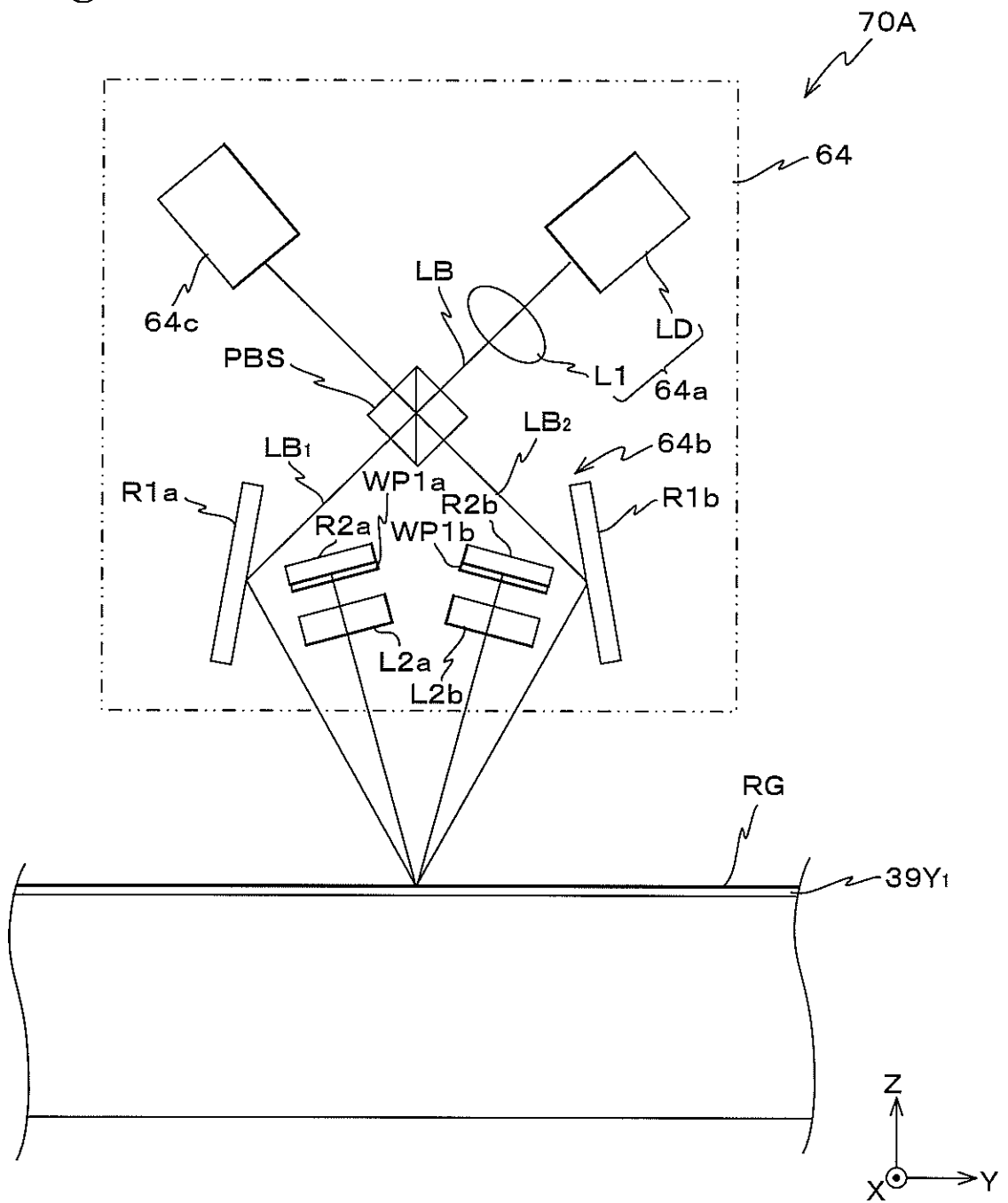
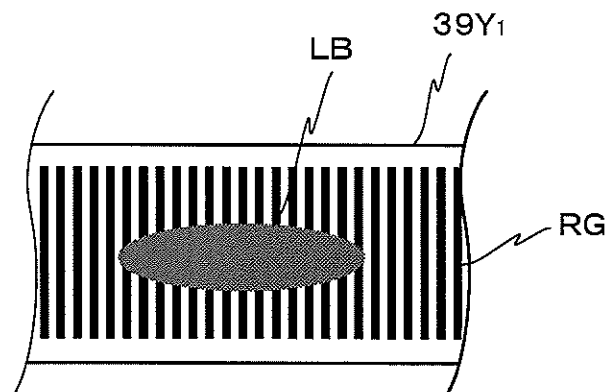
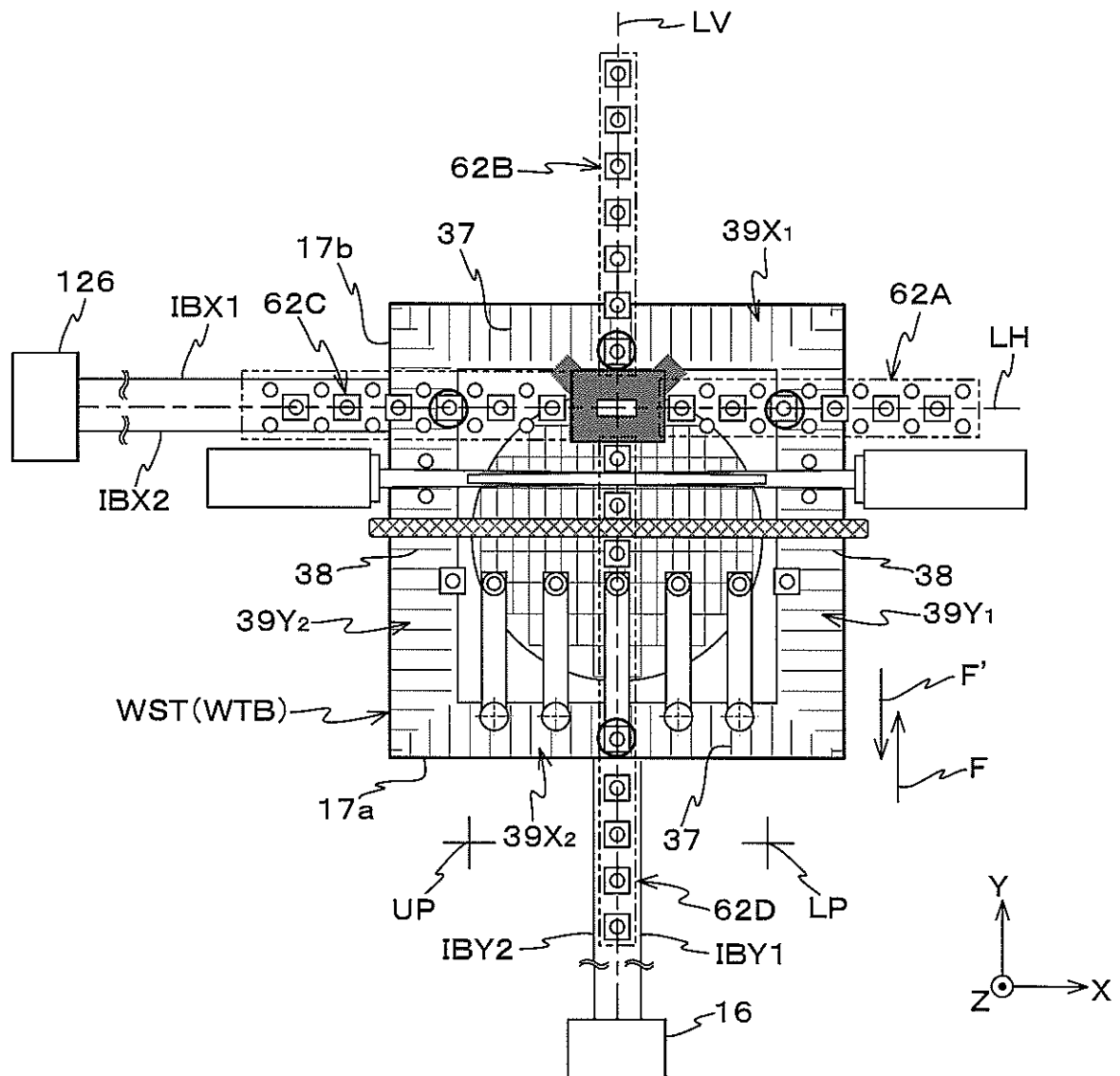
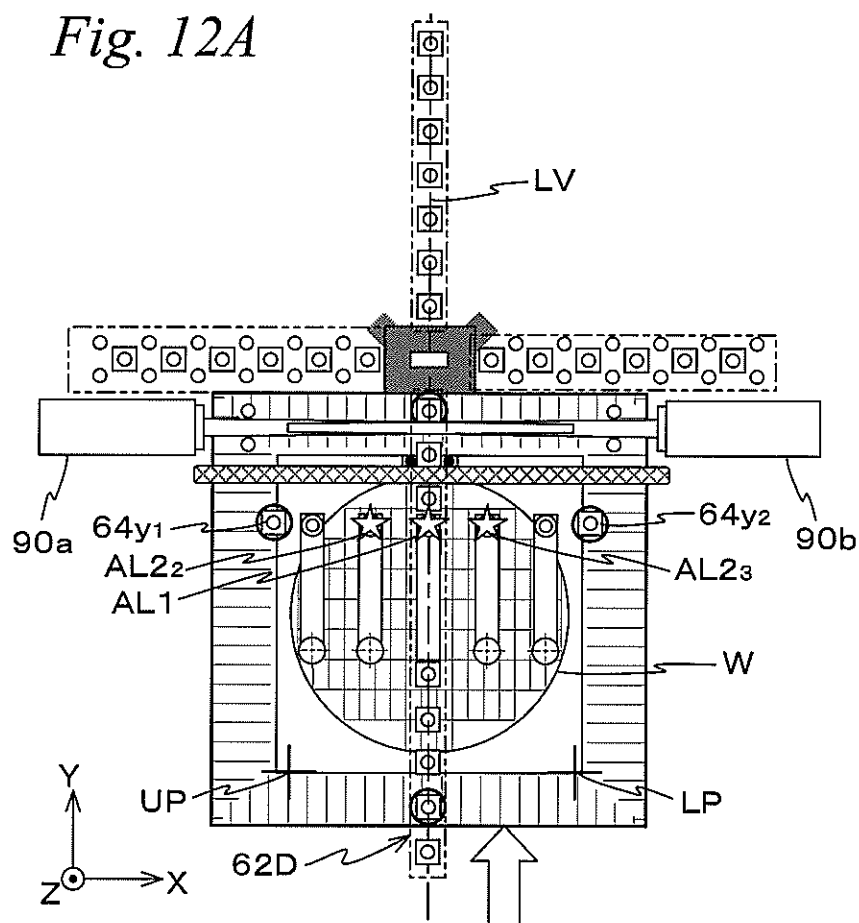
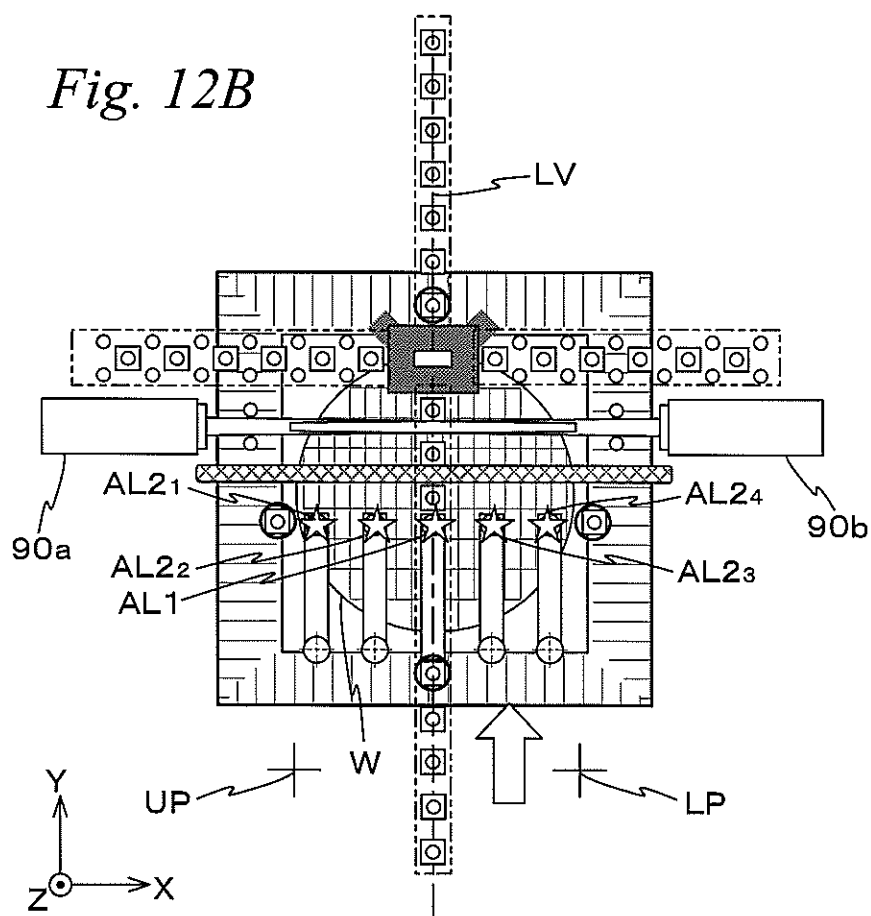
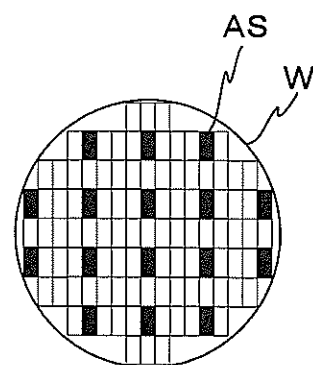
*Fig. 10A**Fig. 10B*

Fig. 11



*Fig. 12A**Fig. 12B**Fig. 12C*

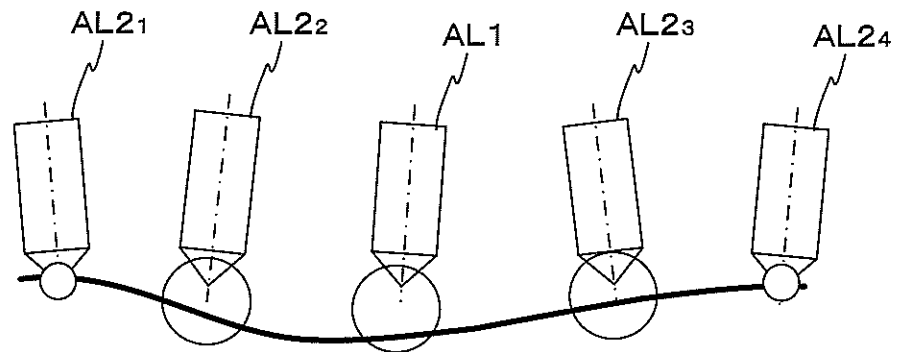
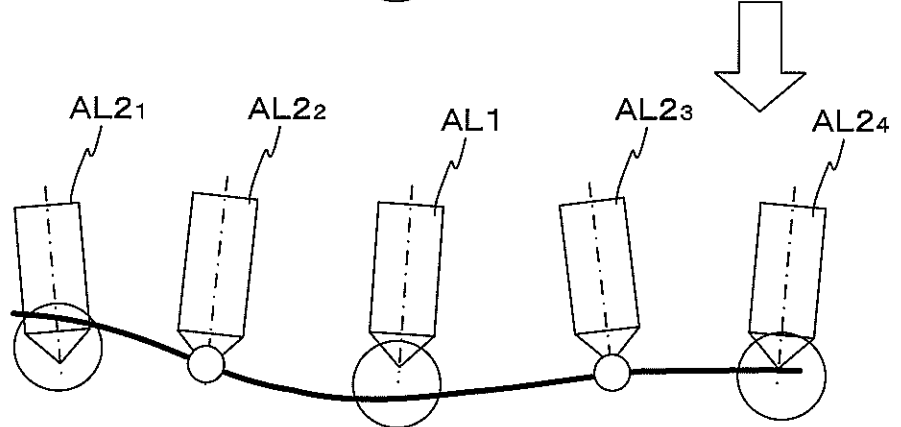
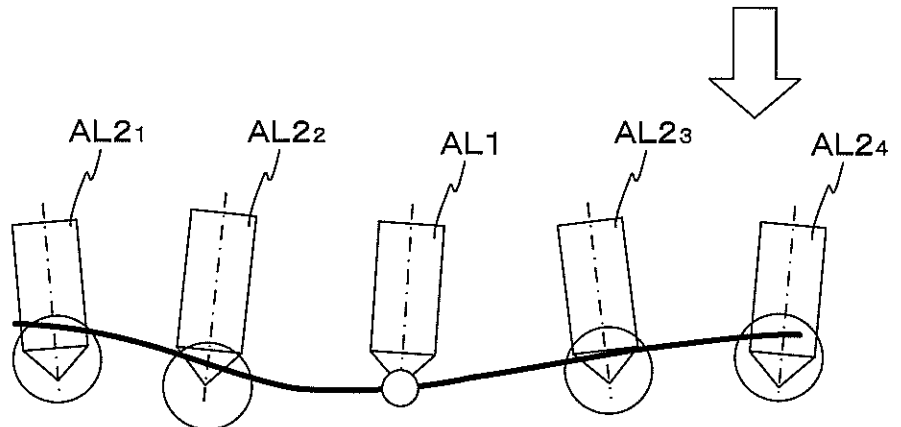
*Fig. 13A**Fig. 13B**Fig. 13C*

Fig. 14A

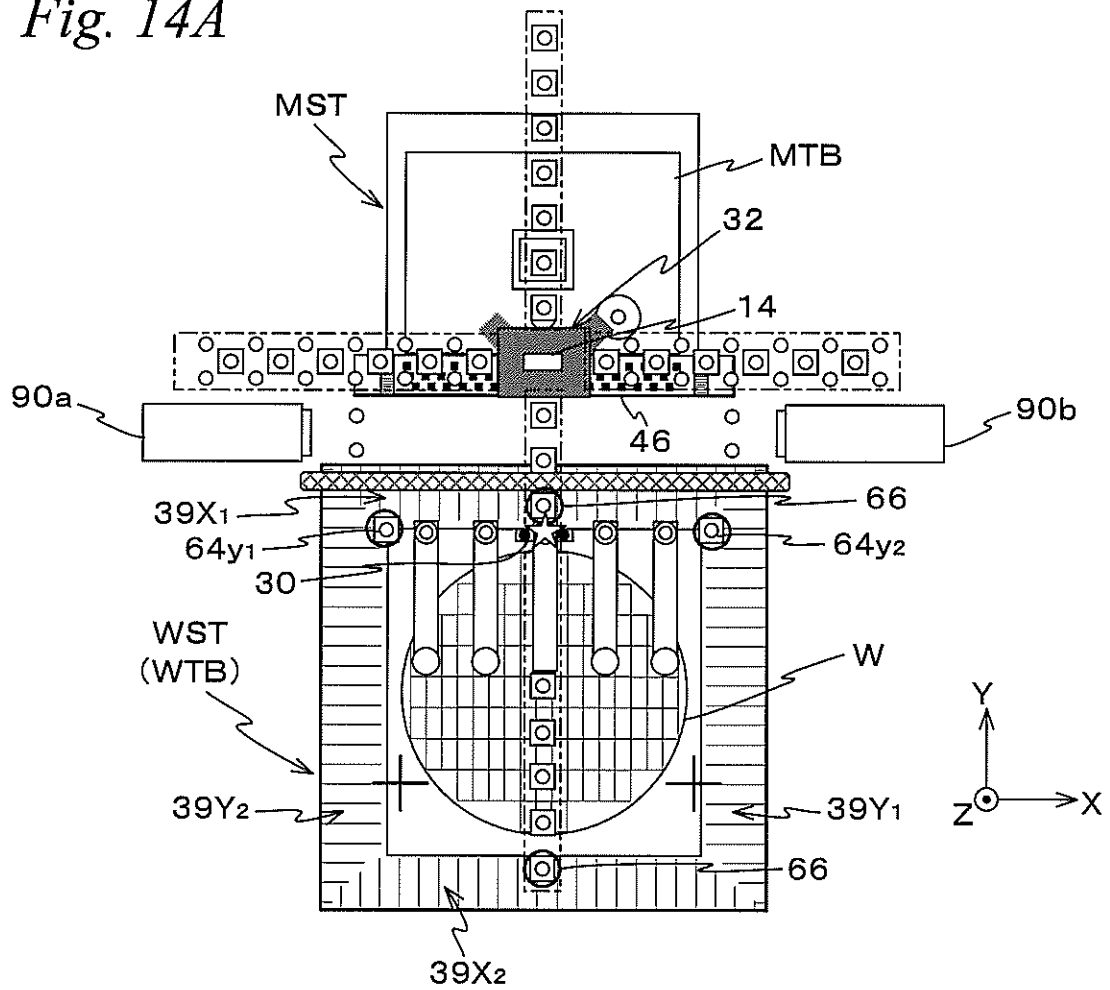


Fig. 14B

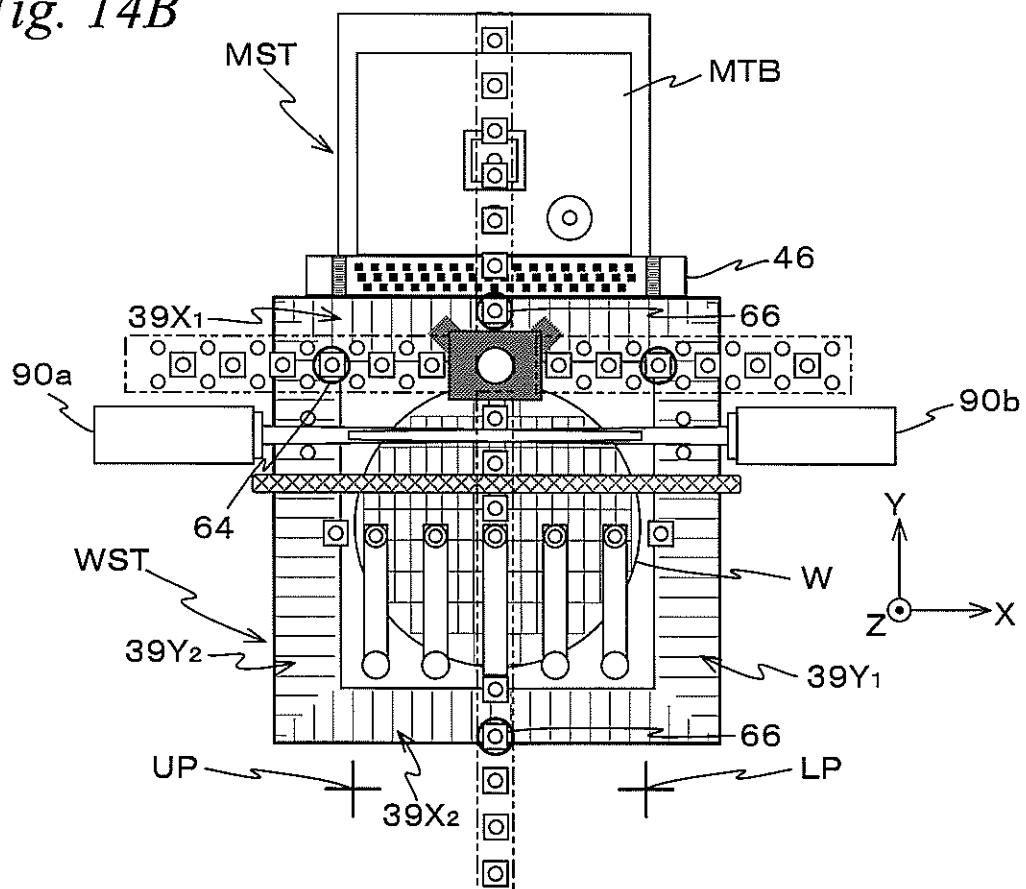


Fig. 15A

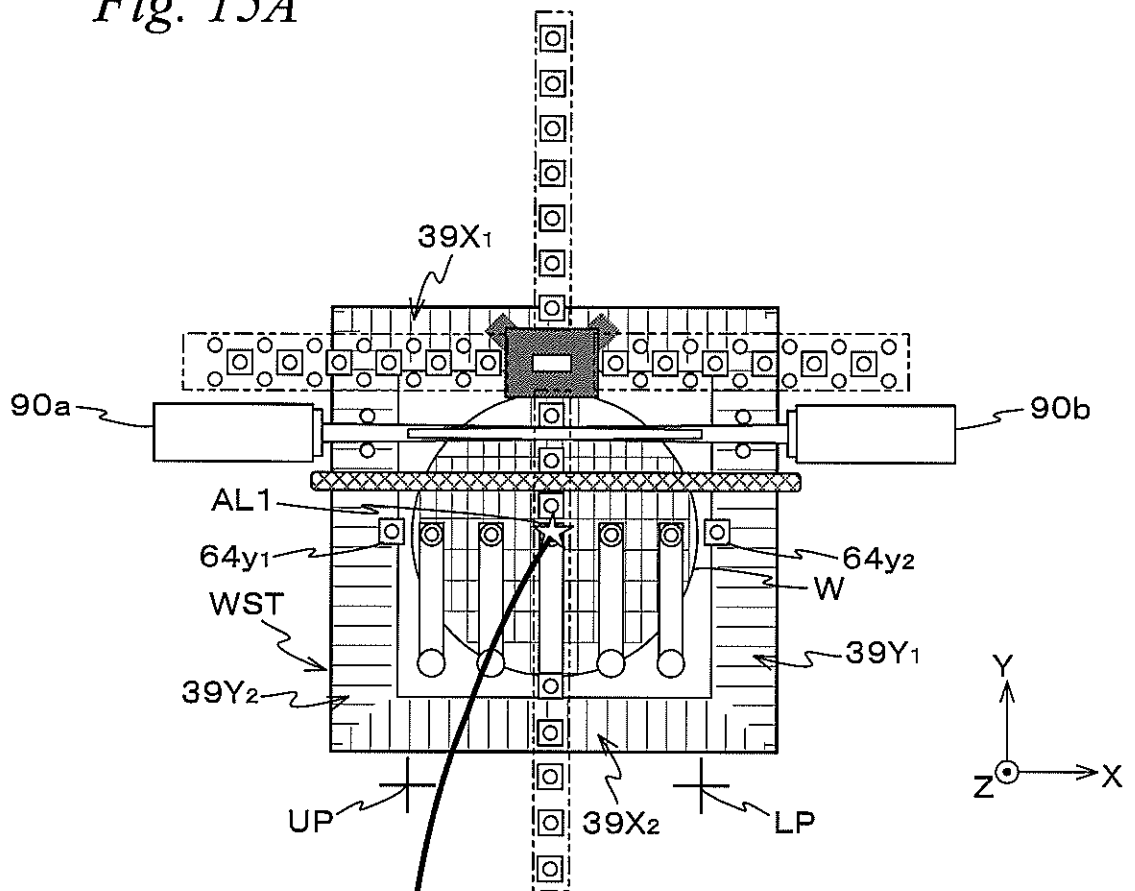


Fig. 15B

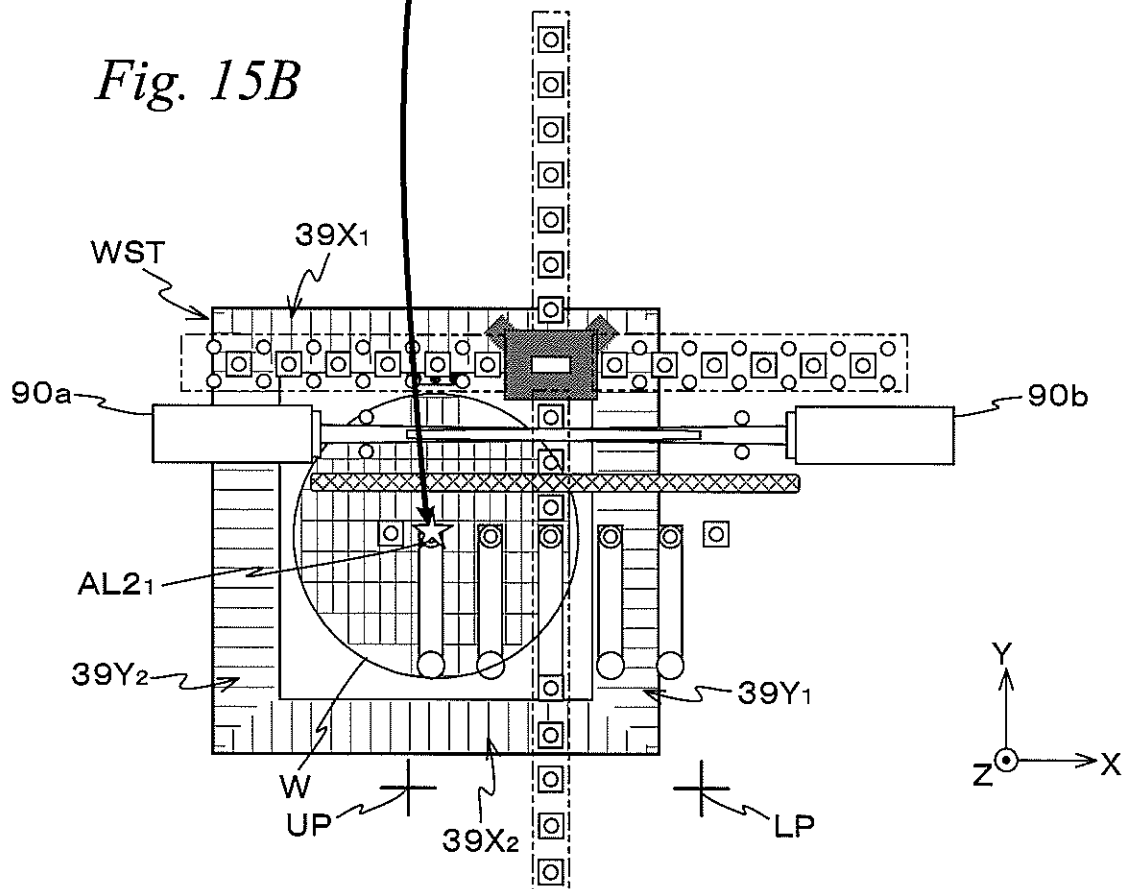


Fig. 16

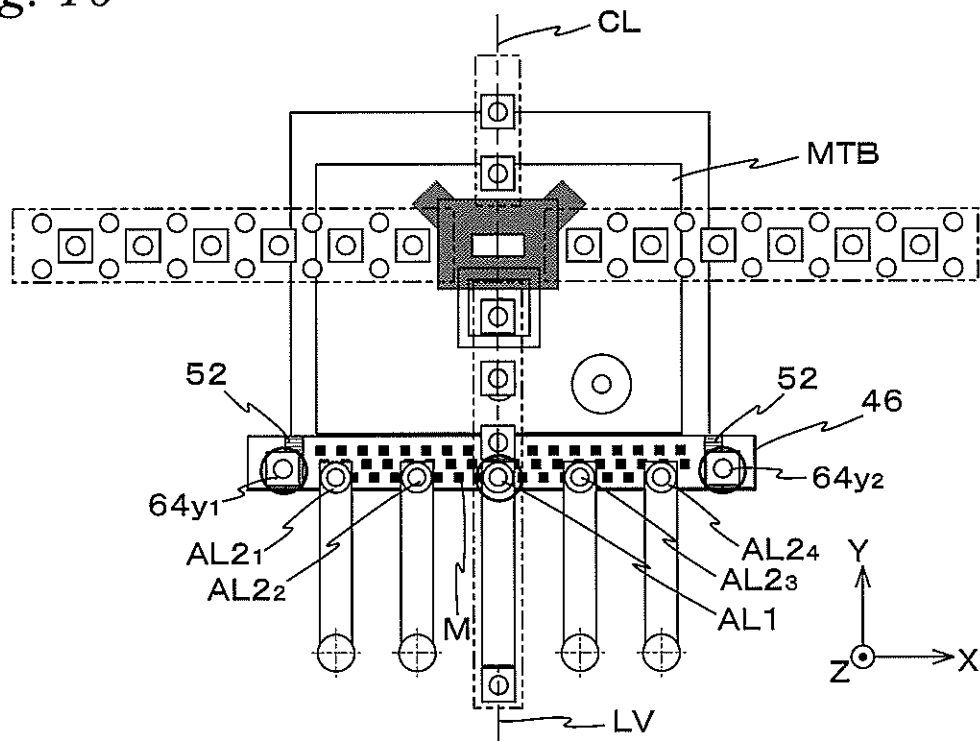


Fig. 17A

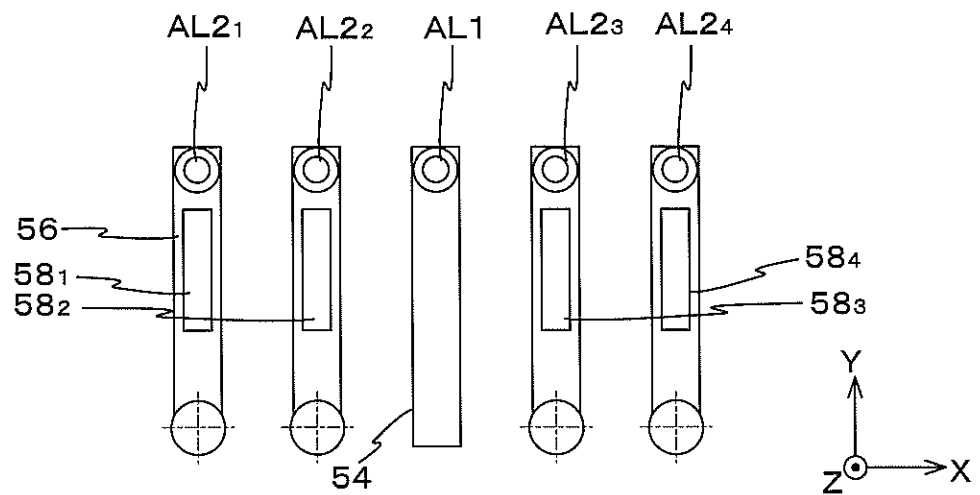
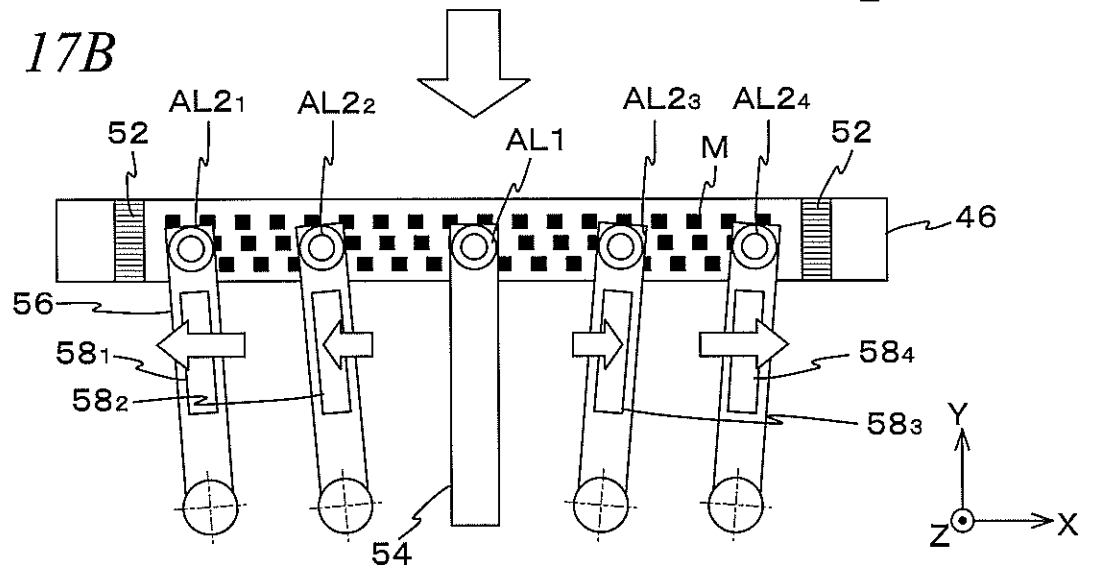
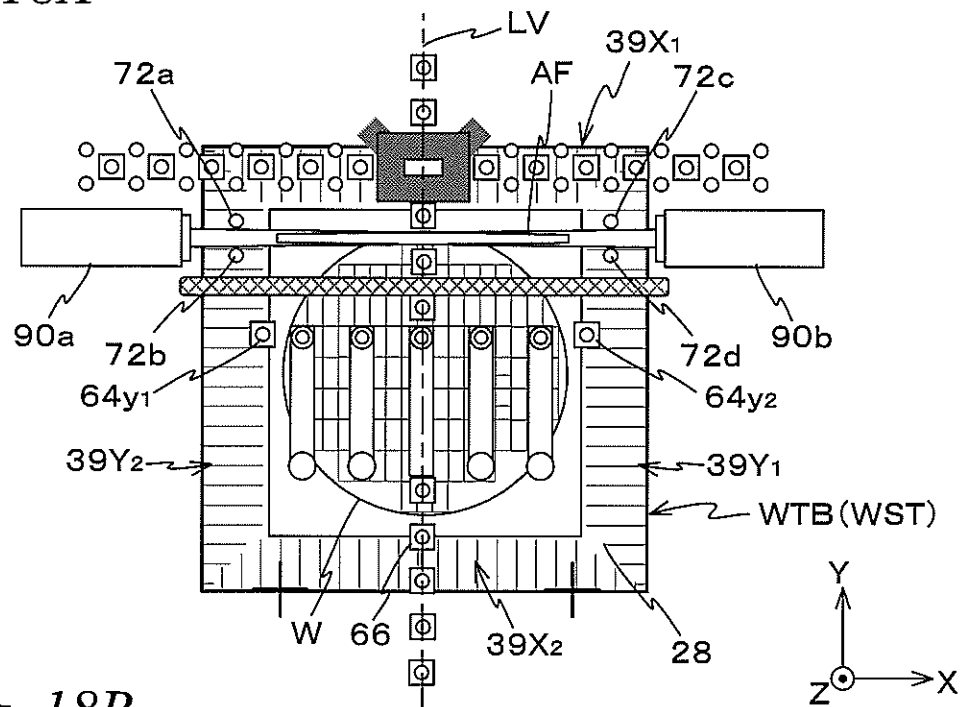


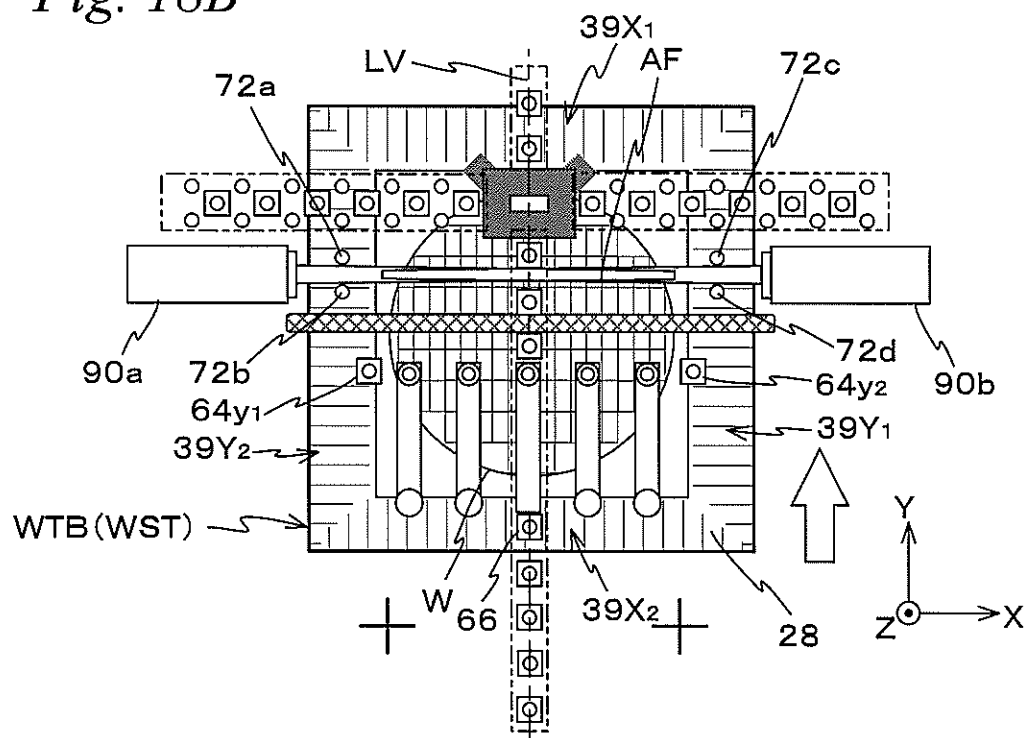
Fig. 17B



*Fig. 18A*



*Fig. 18B*



*Fig. 18C*

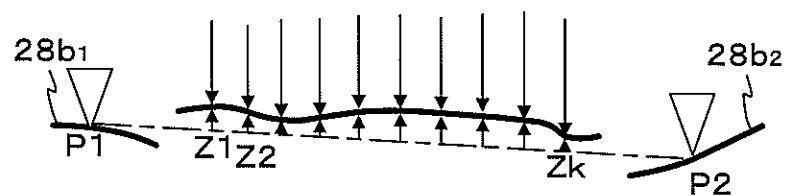


Fig. 19A

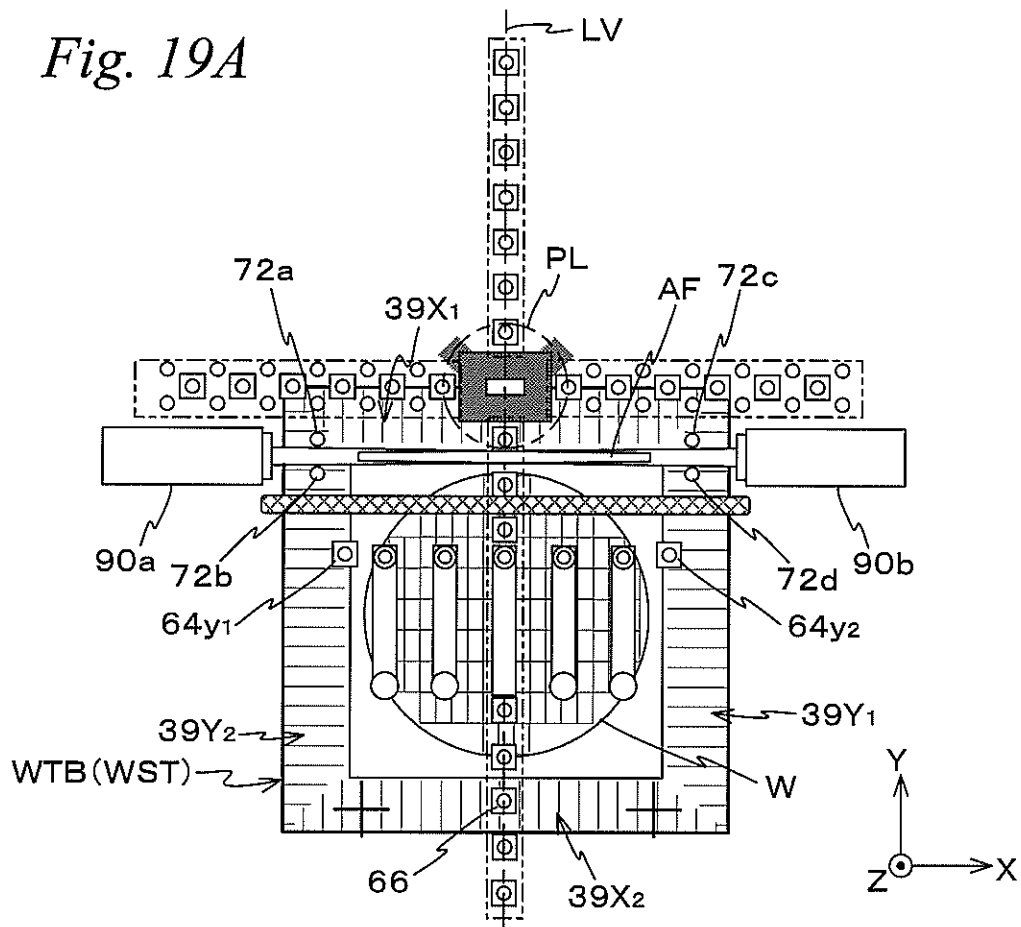
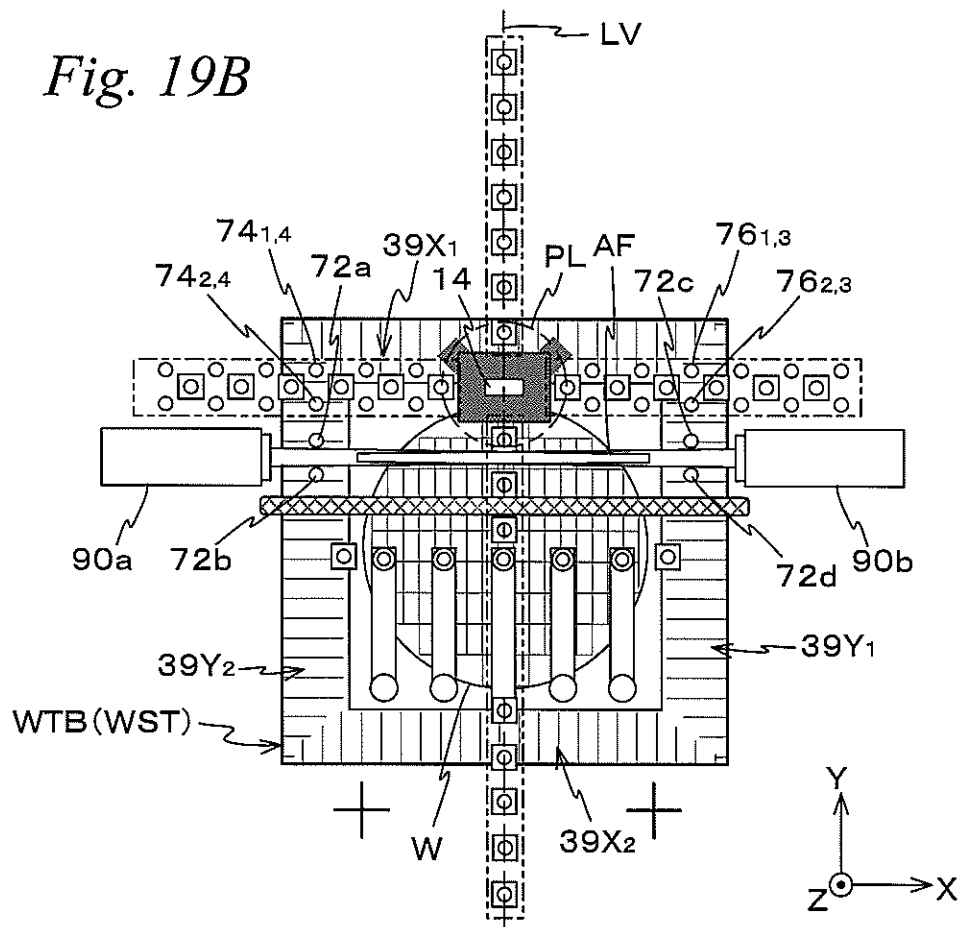


Fig. 19B



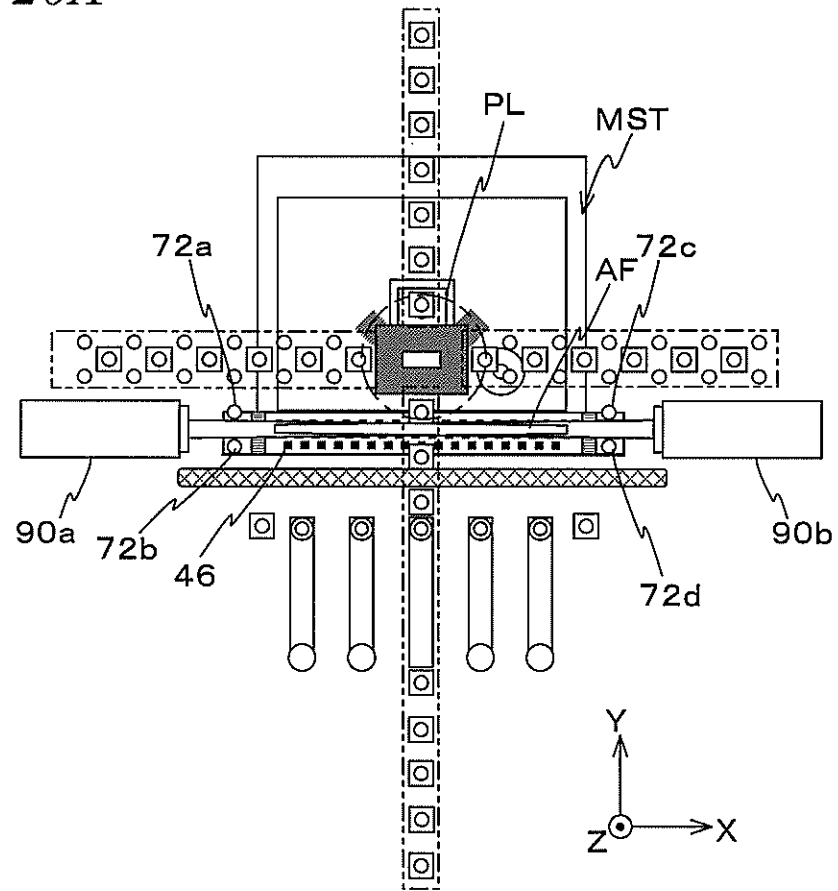
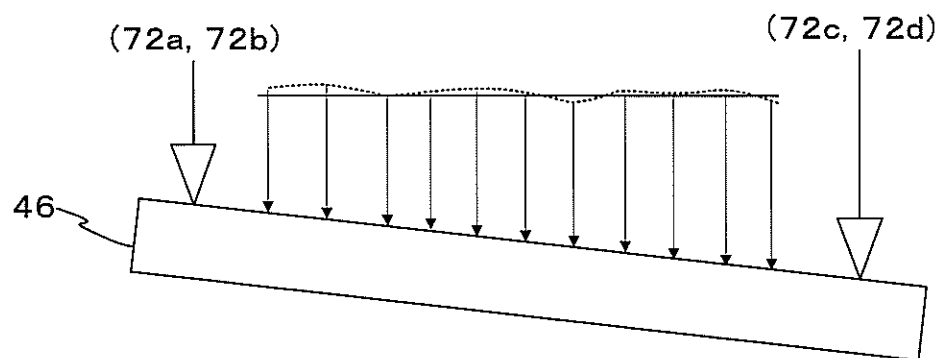
*Fig. 20A**Fig. 20B*

Fig. 21A

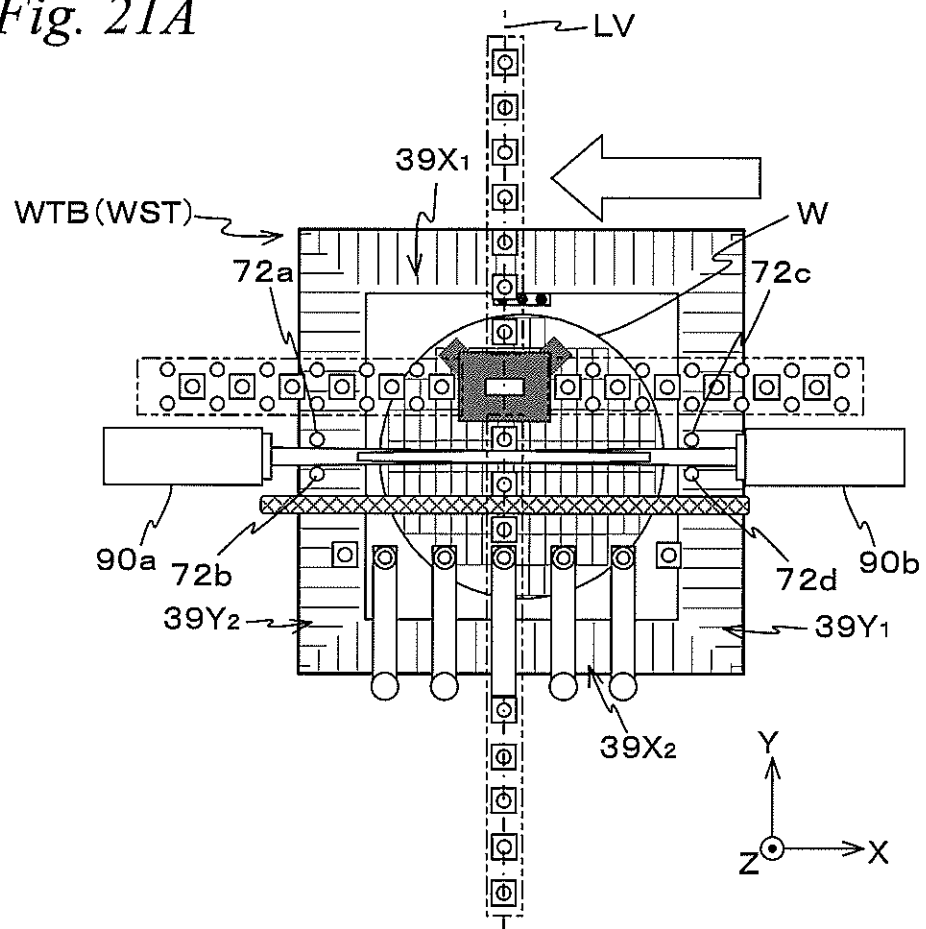


Fig. 21B

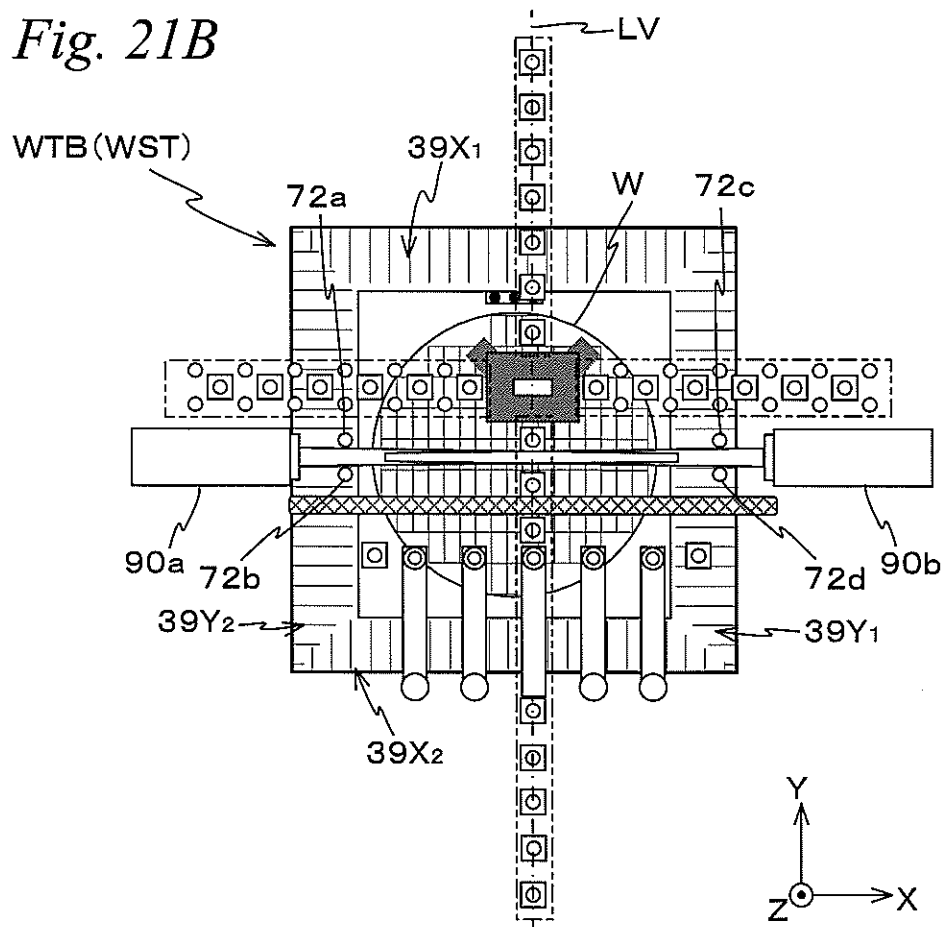


Fig. 22

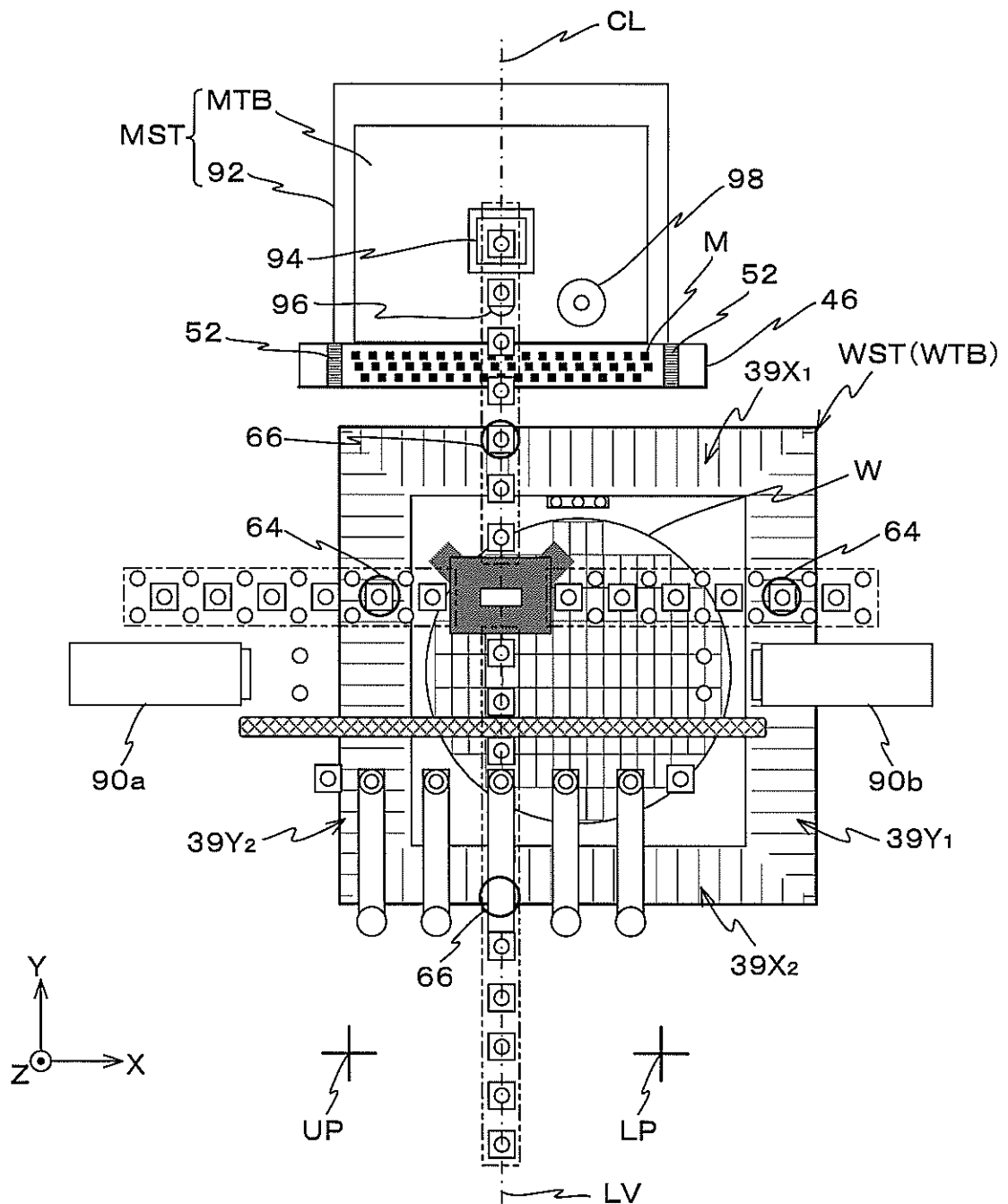


Fig. 23

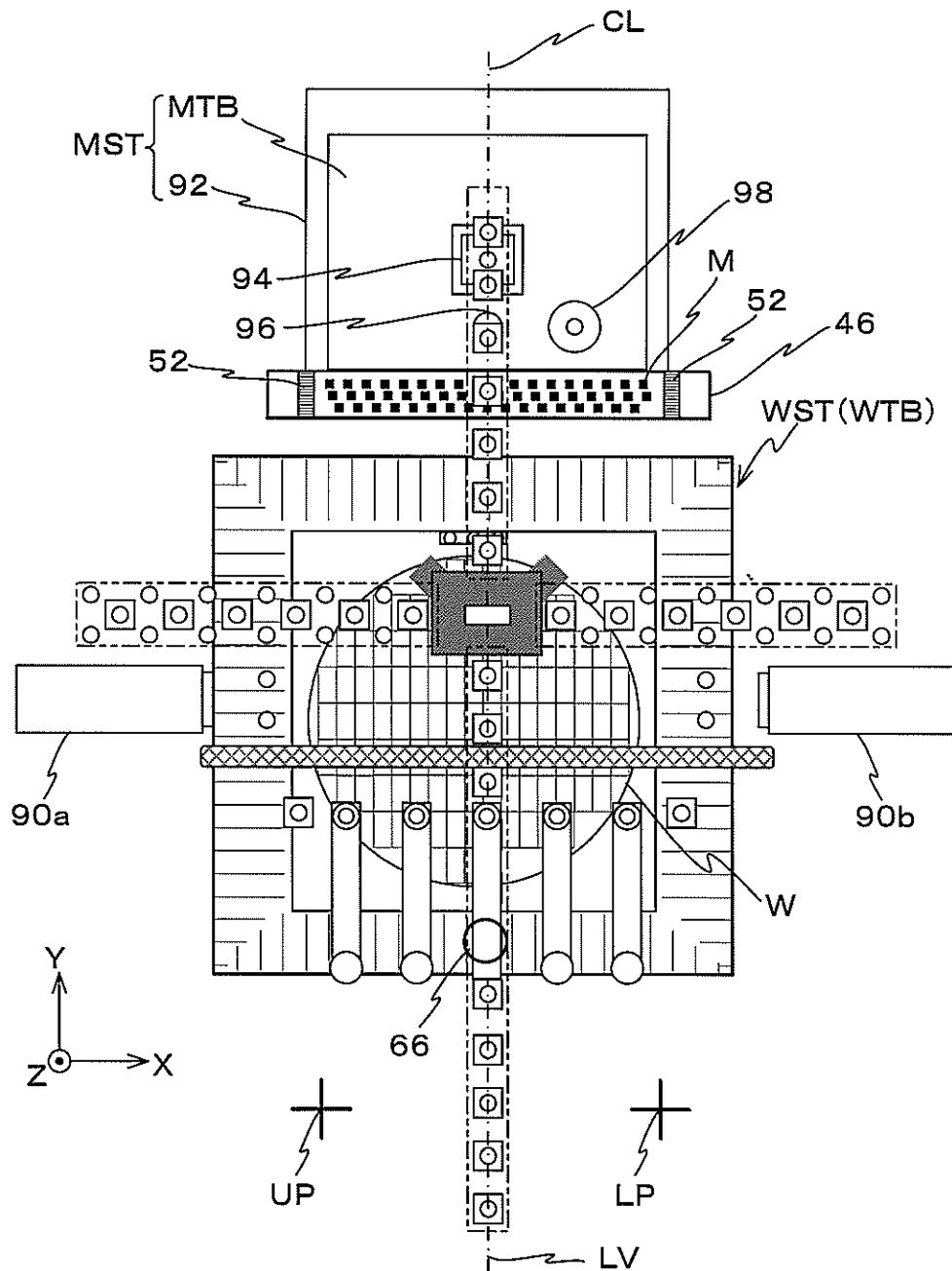
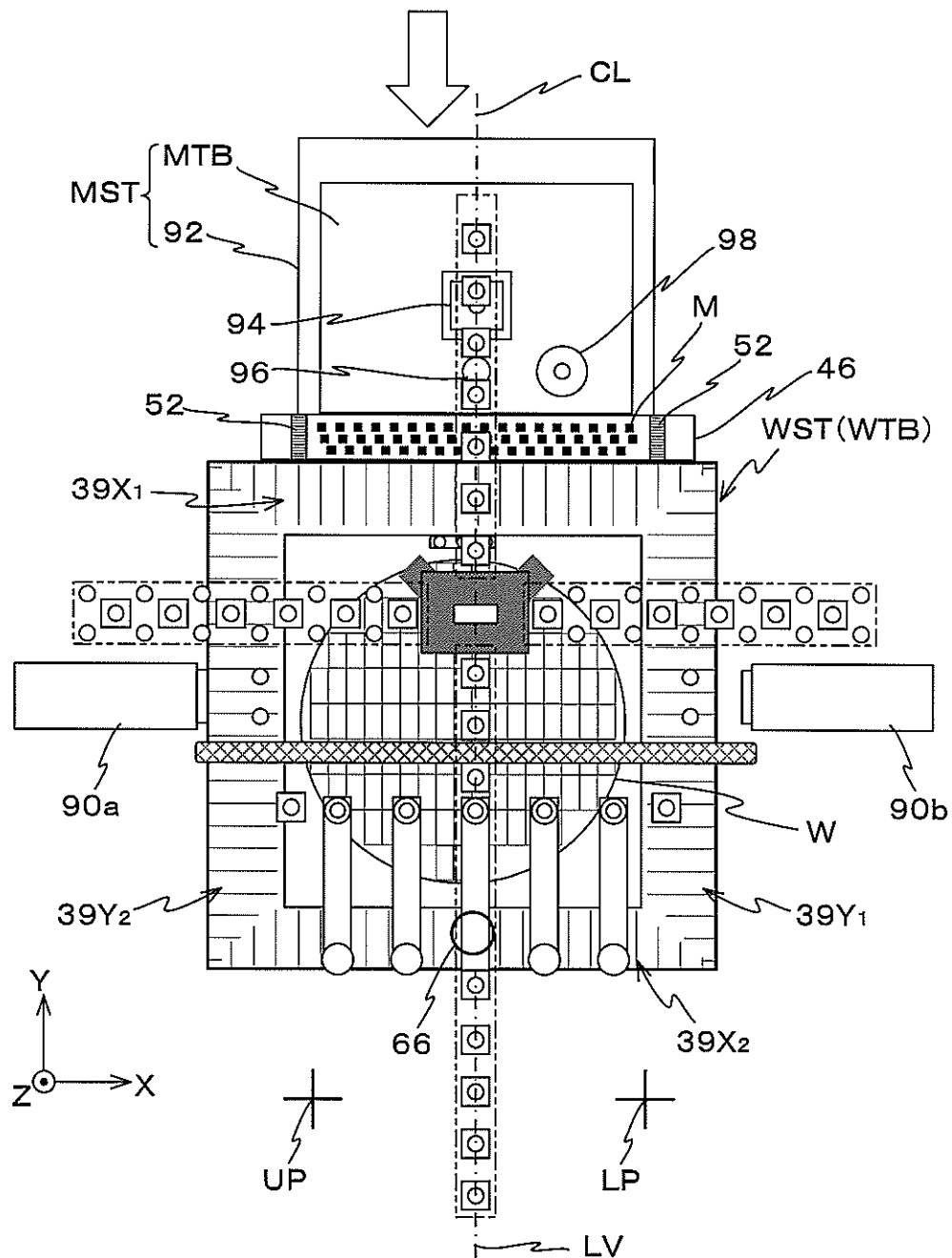


Fig. 24



*Fig. 25*

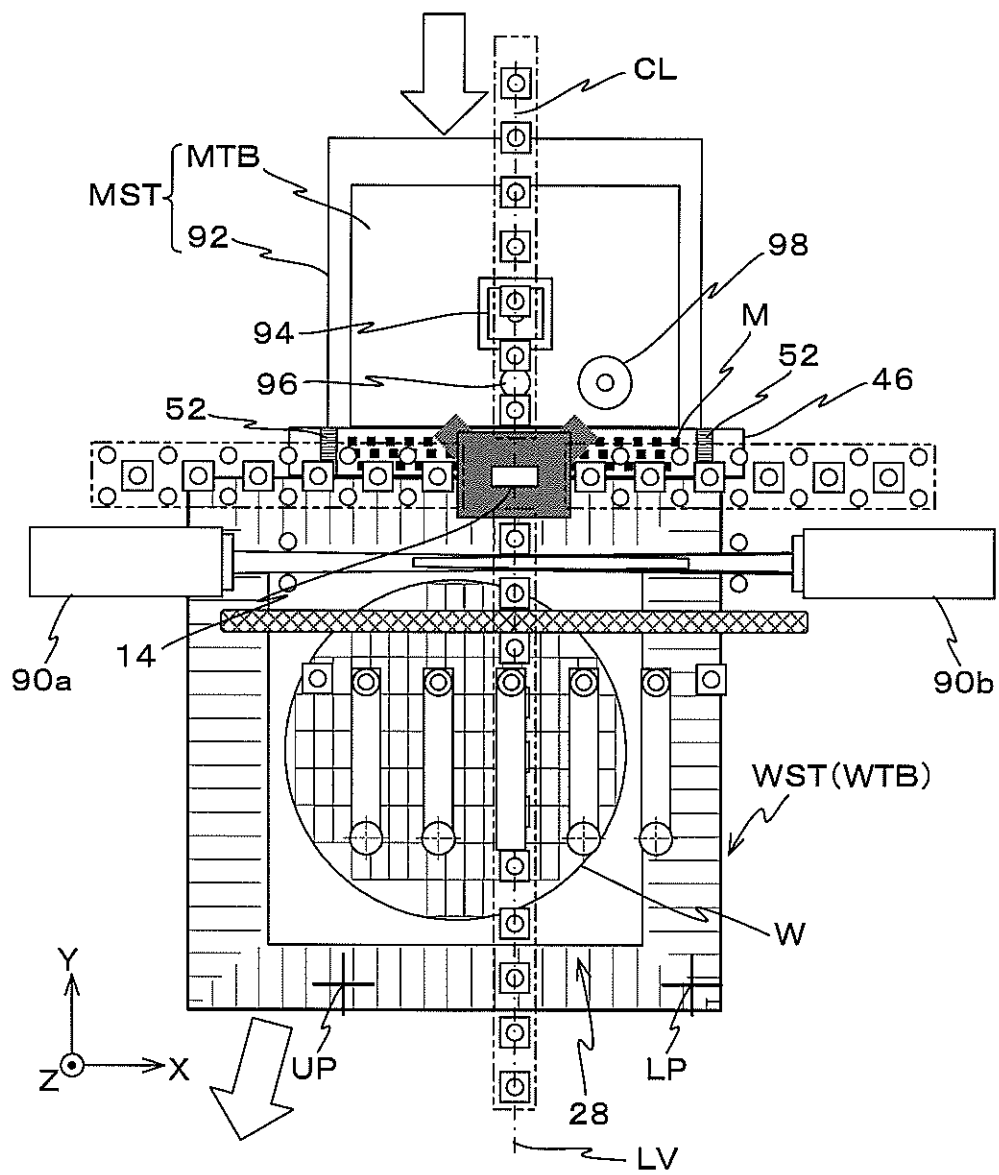


Fig. 26

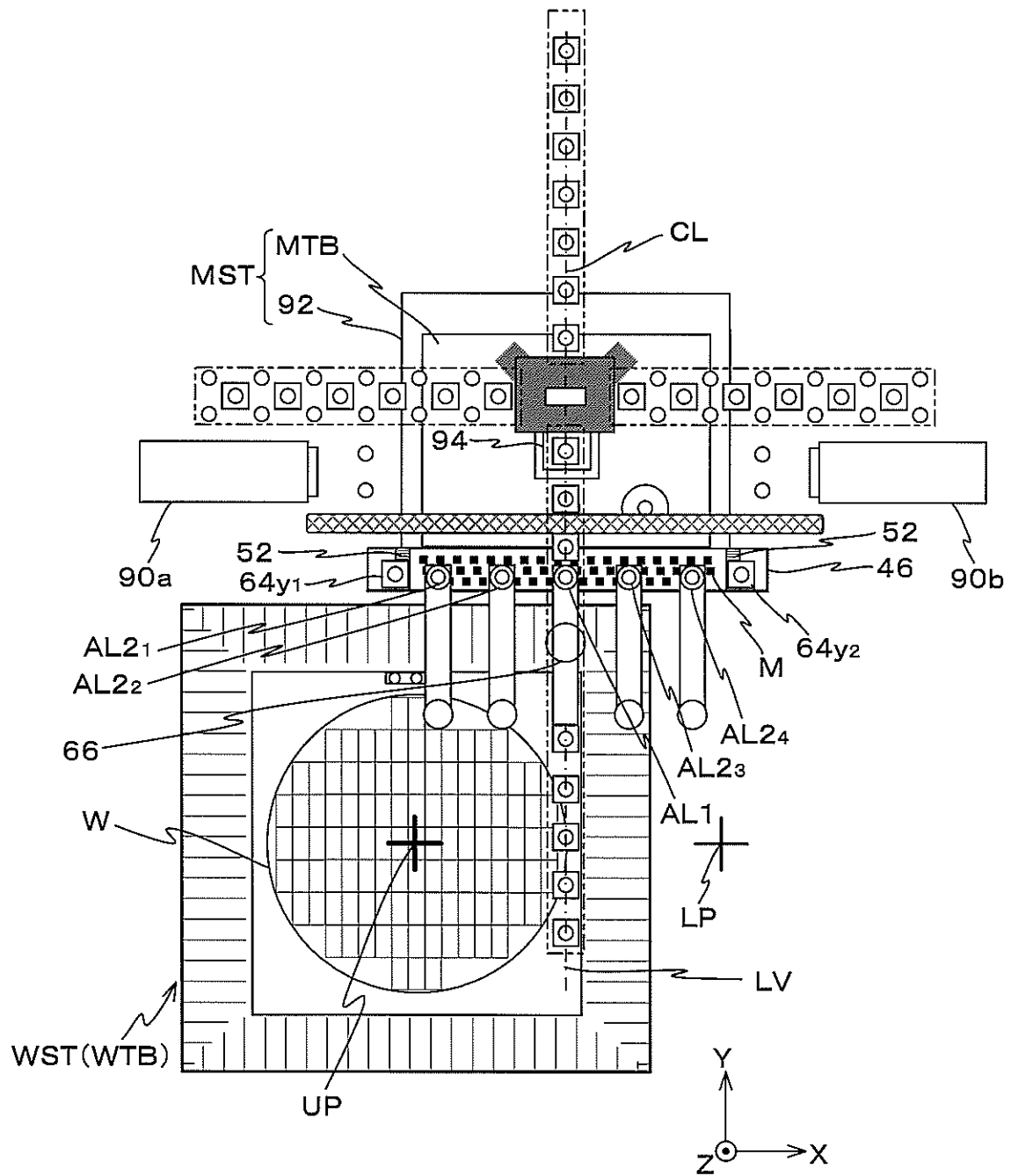


Fig. 27

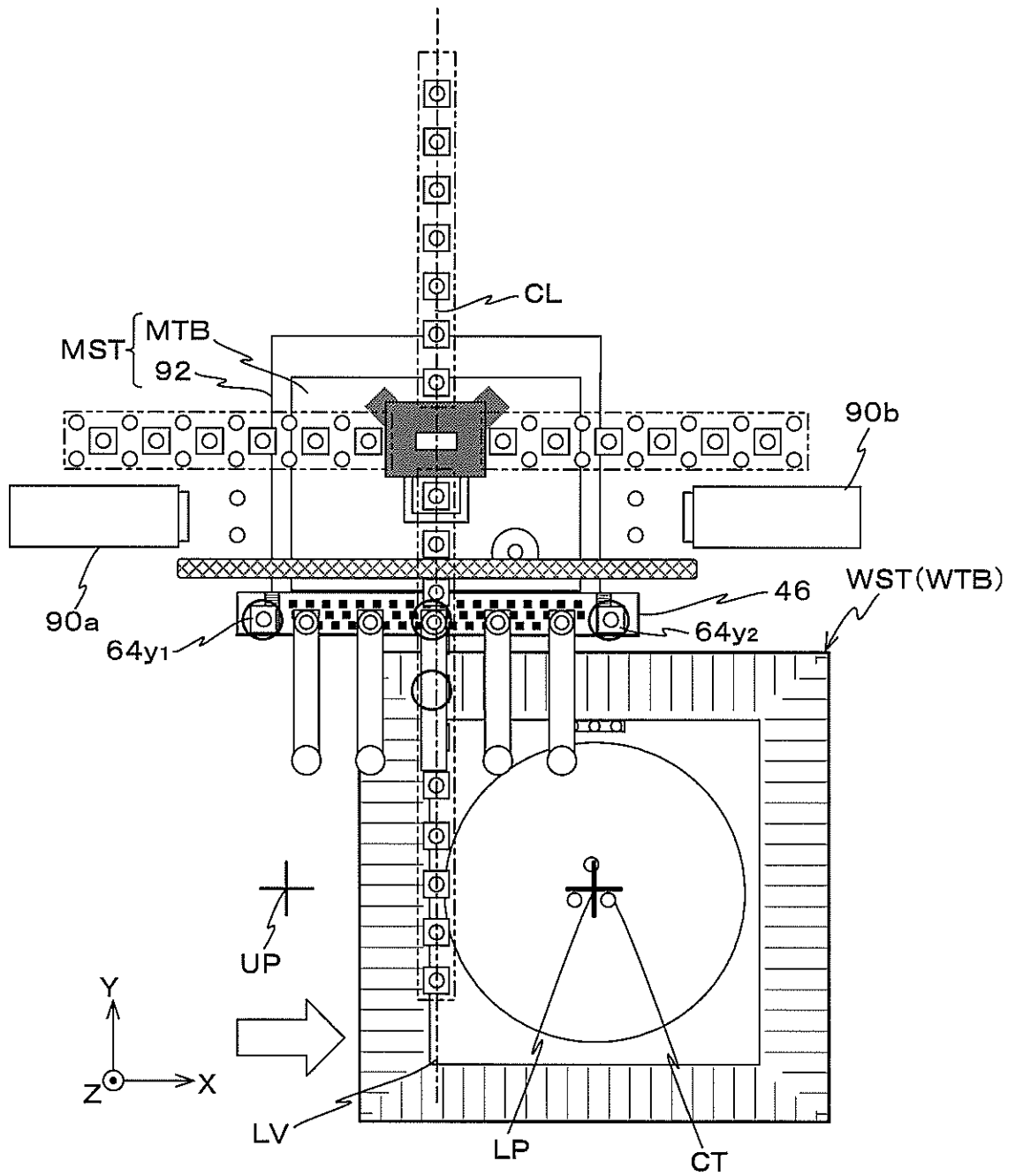


Fig. 28

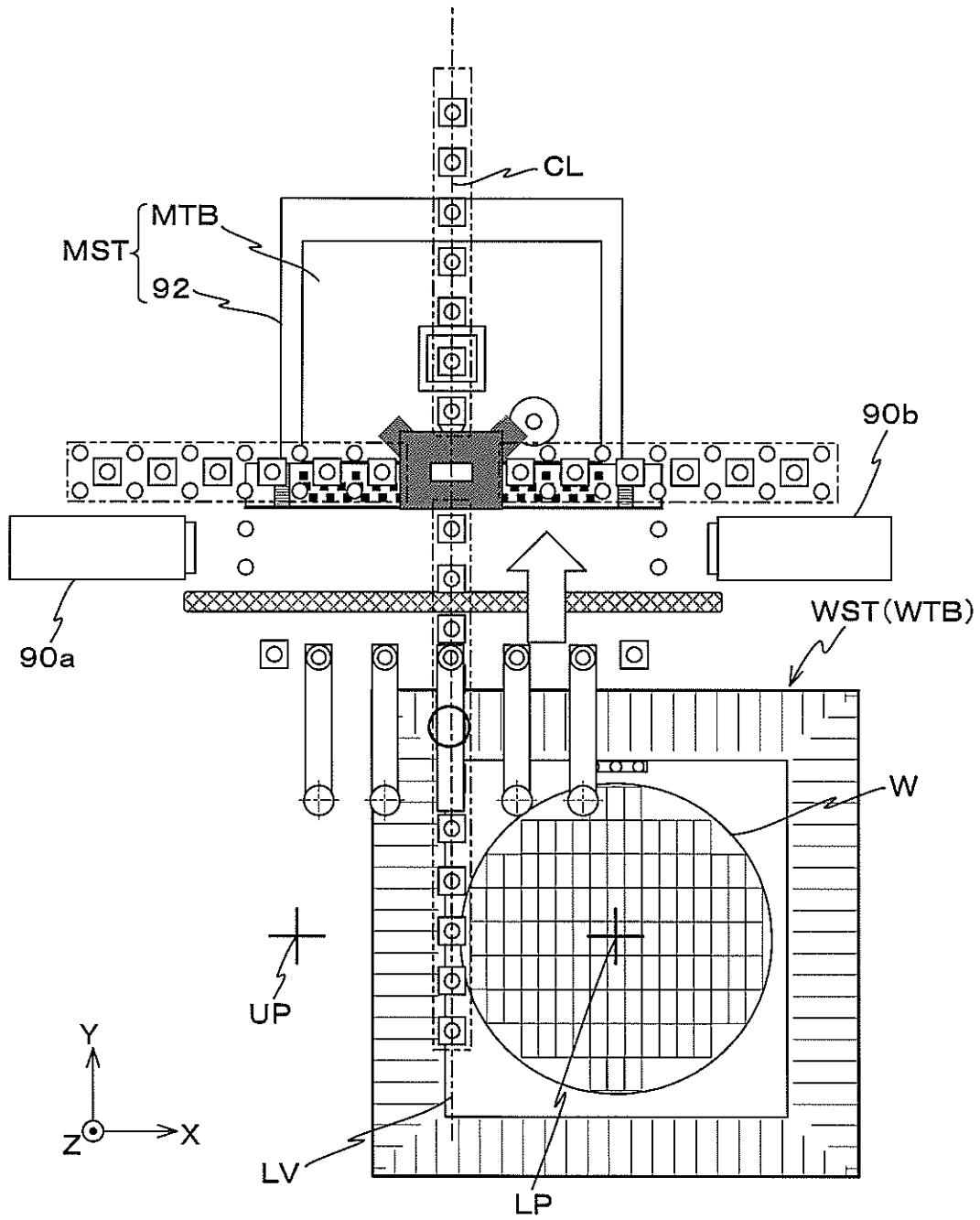


Fig. 29

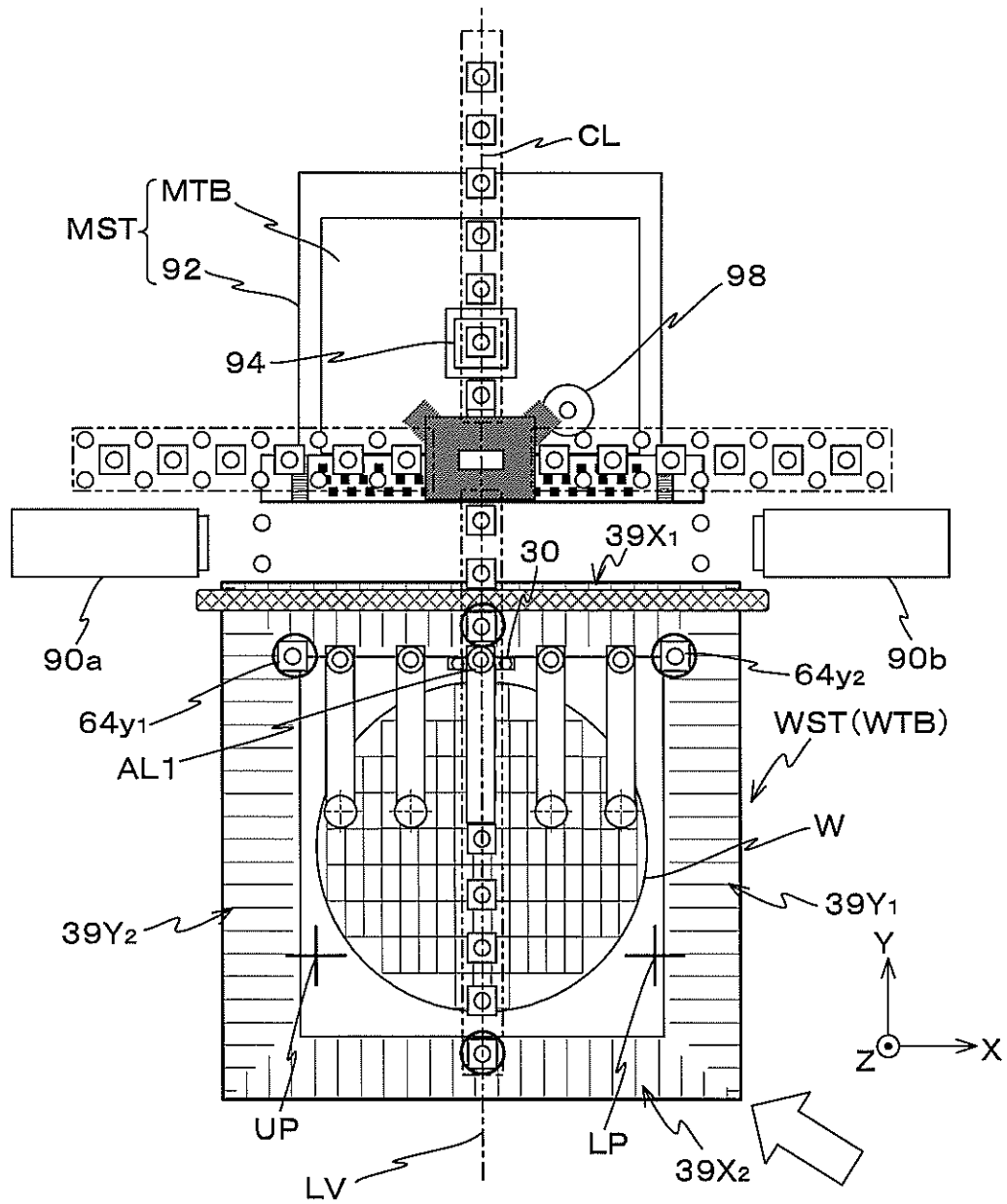


Fig. 30

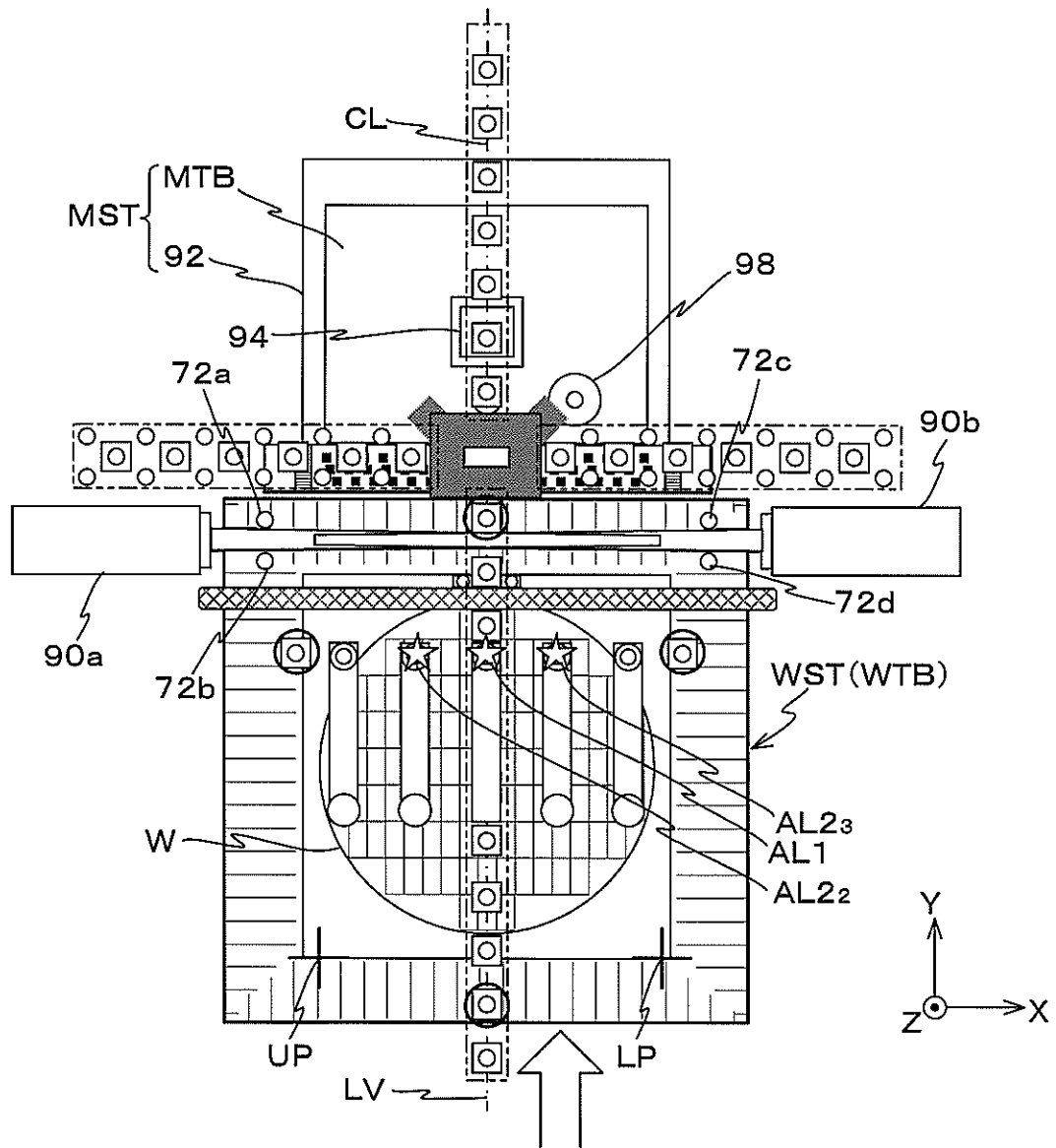




Fig. 32

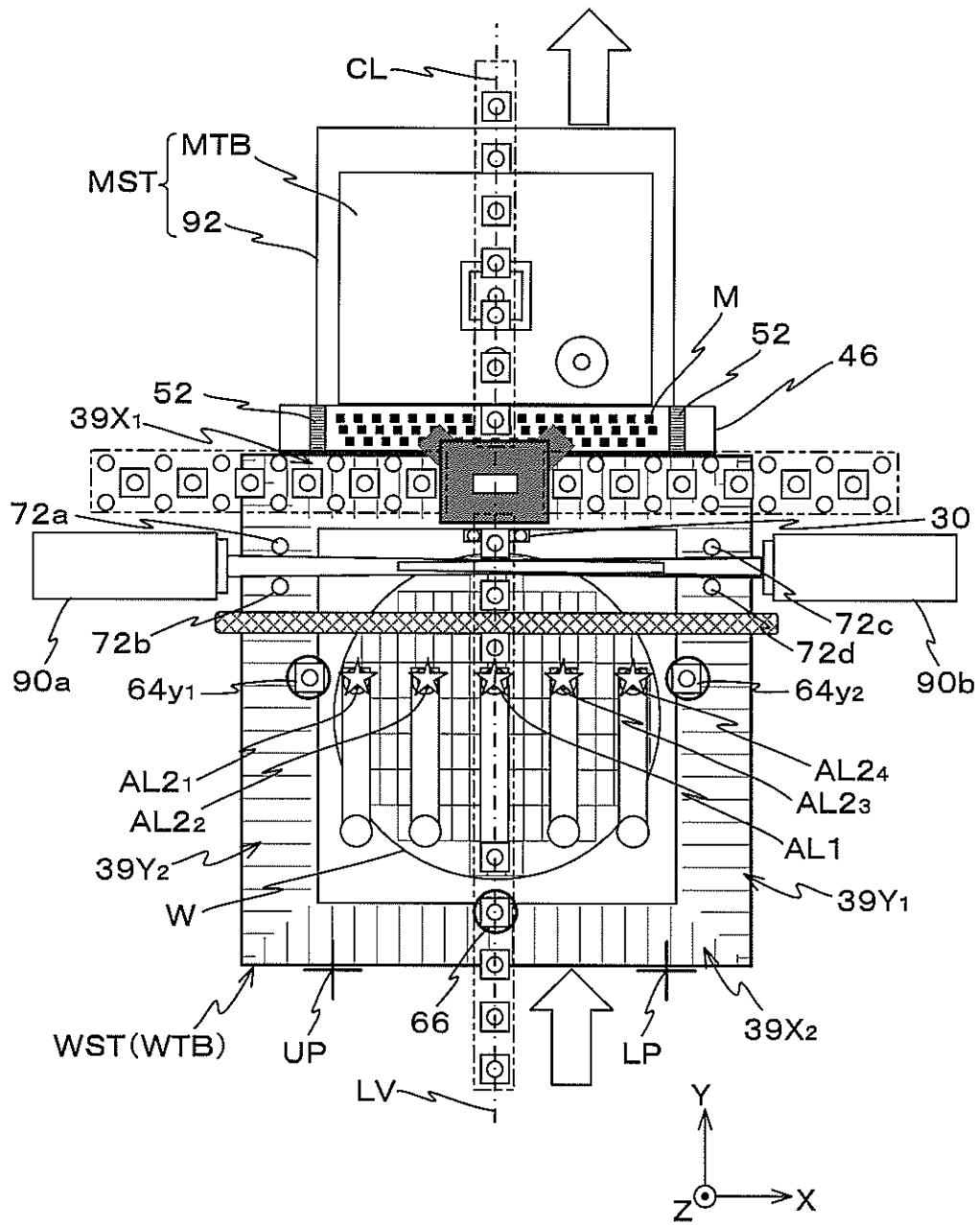






Fig. 35

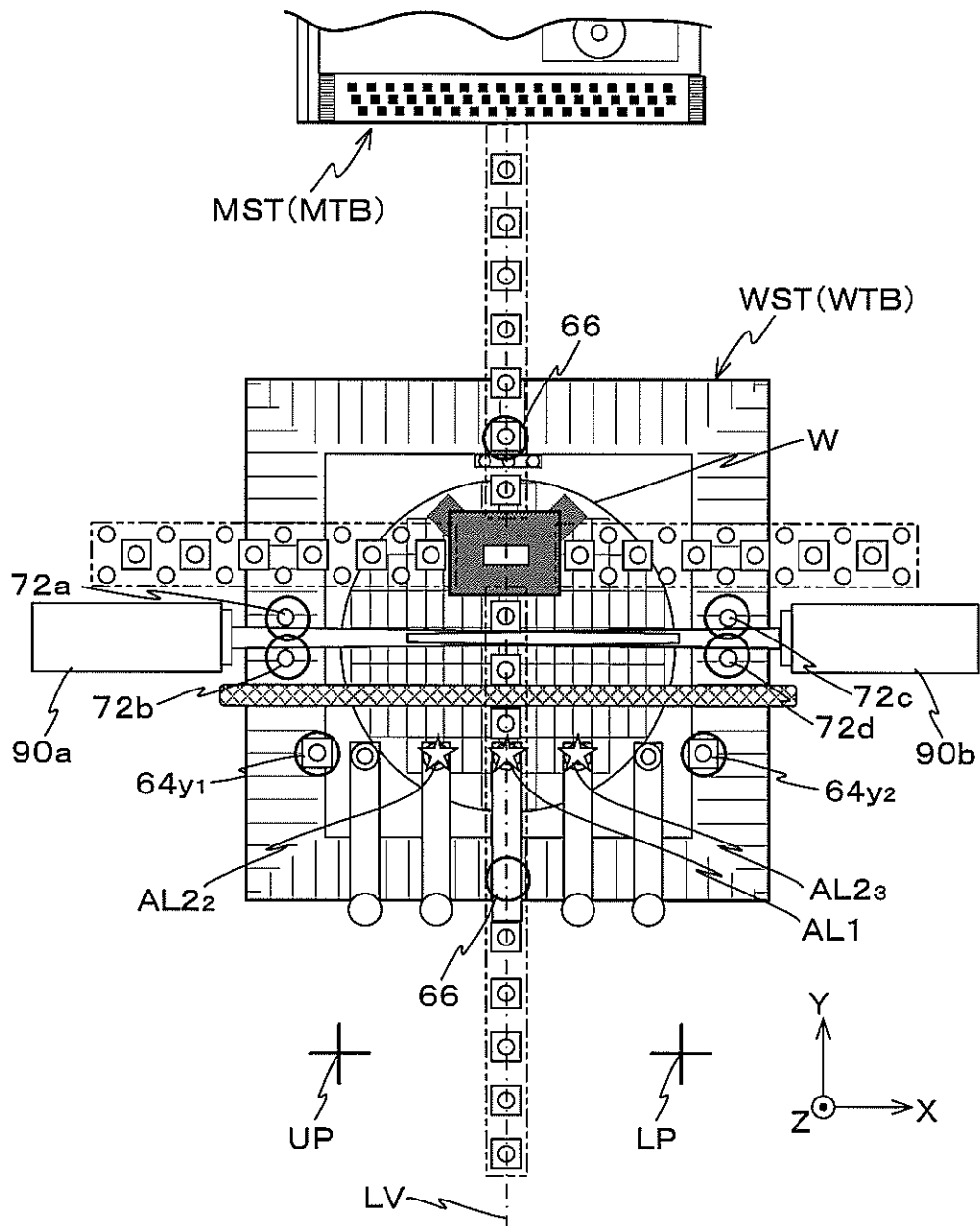
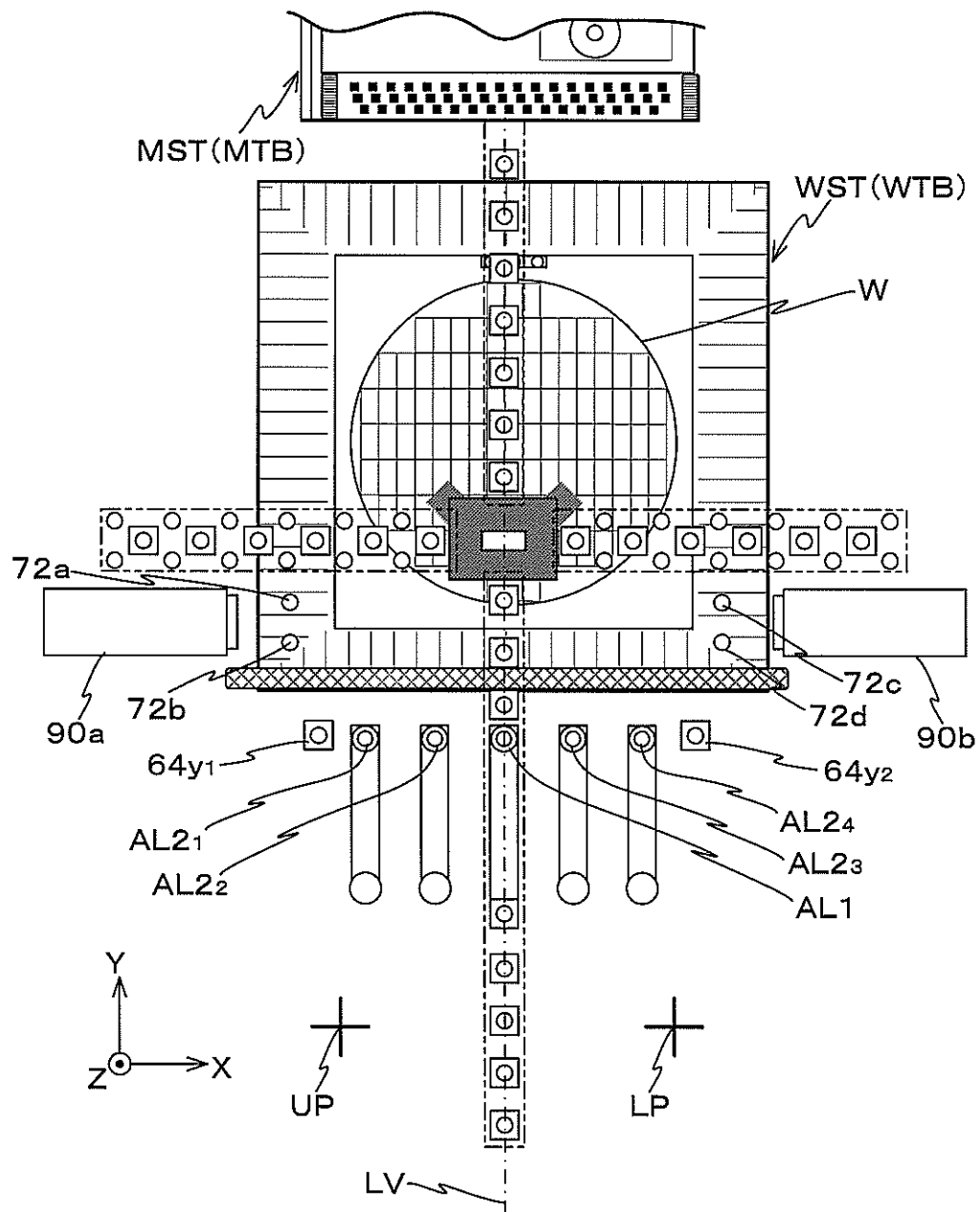
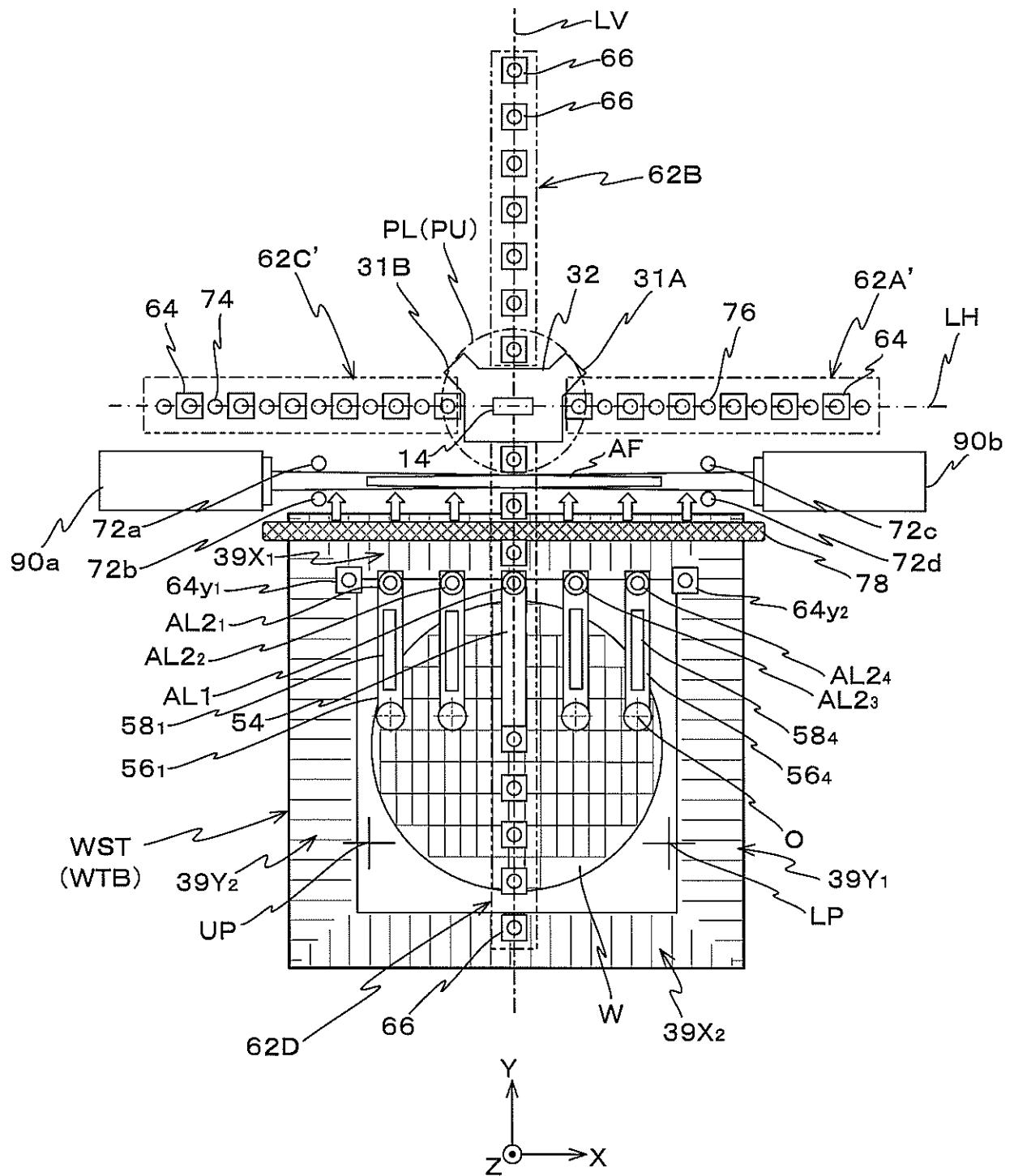


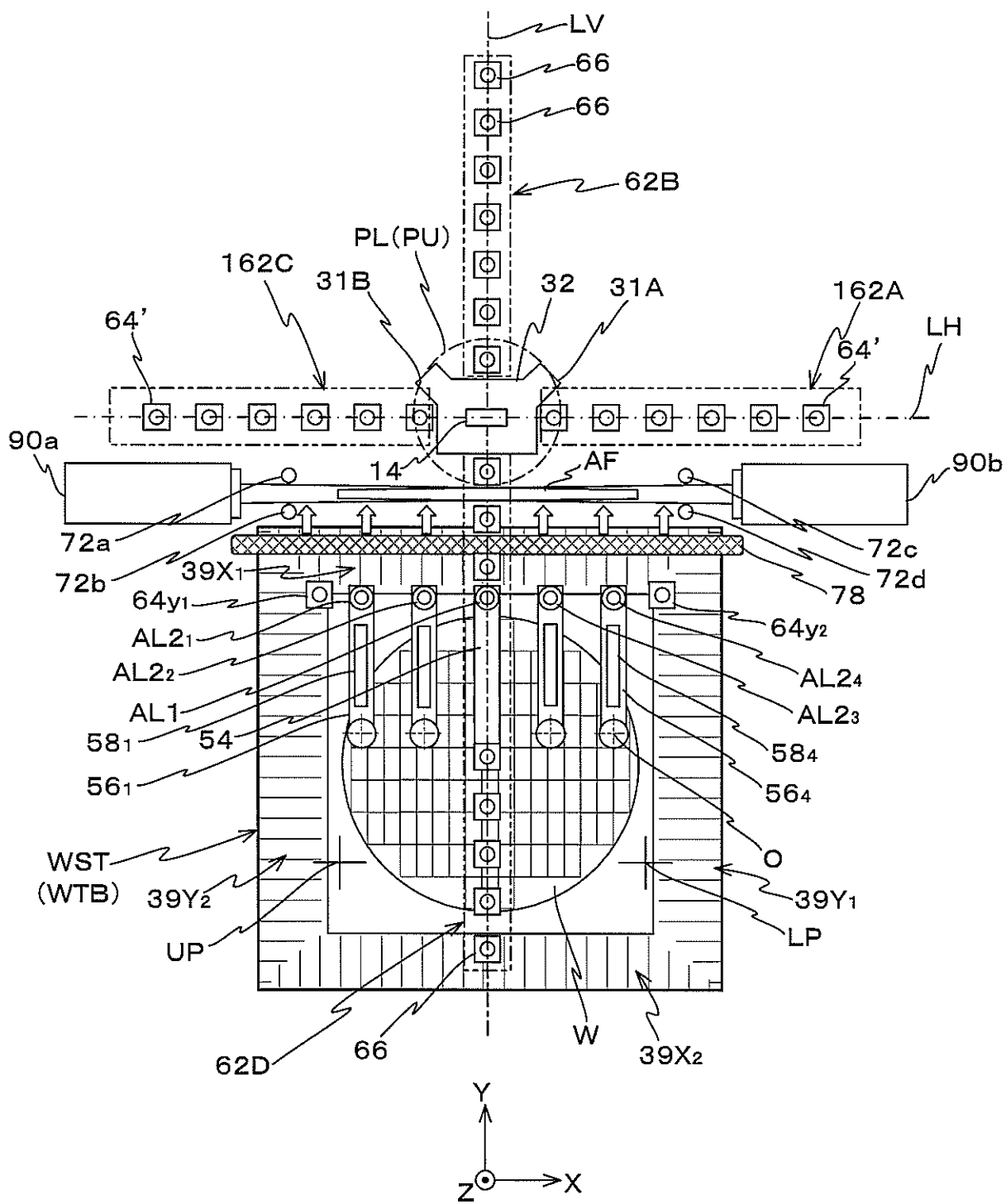
Fig. 36



*Fig. 37*



*Fig. 38*



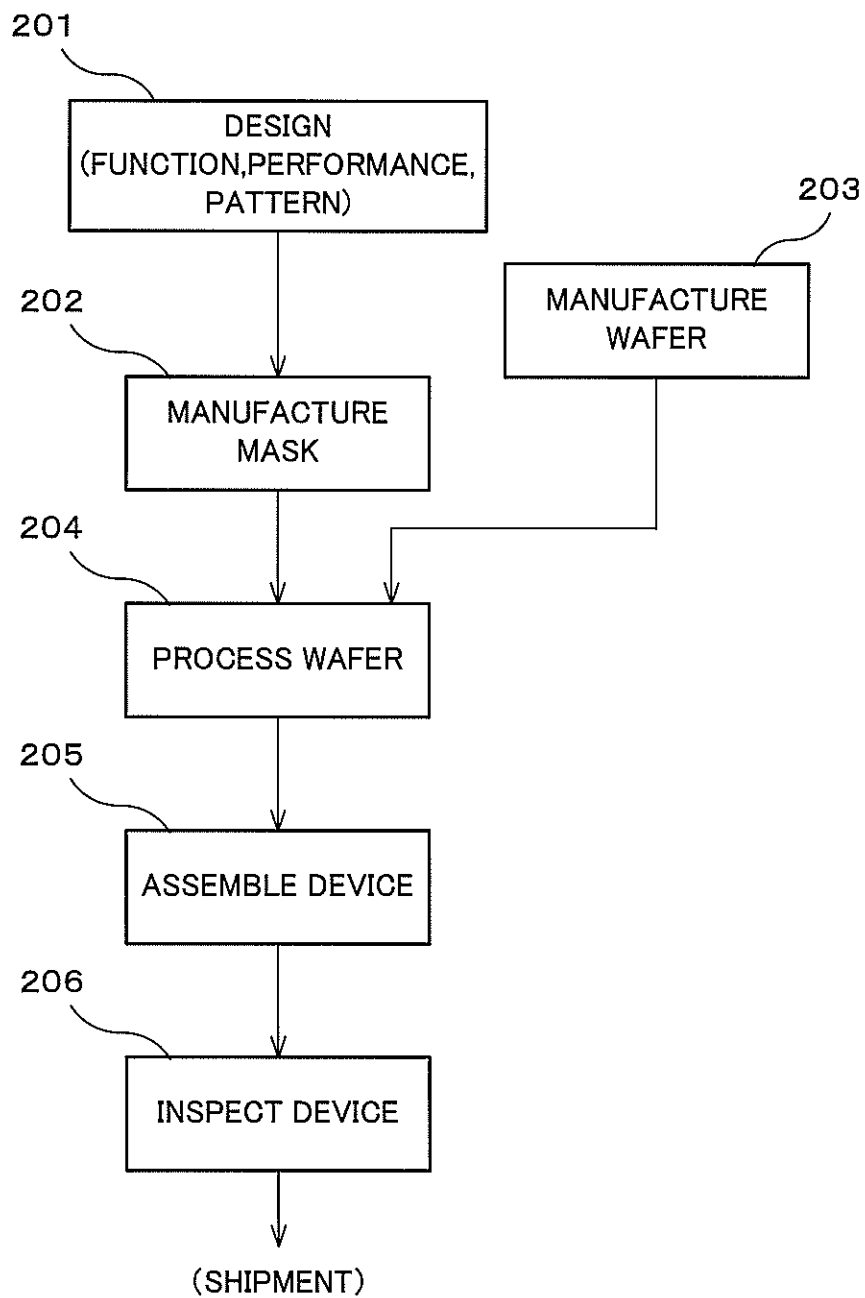
*Fig. 39*

Fig. 40

