

ABSTRACT

ELECTROSTATIC DISCHARGE PROTECTION TRANSISTOR STRUCTURE

5 A MOS transistor structure is provided for ESD protection in an integrated circuit device. A trench controls salicide deposition to prevent hot spot formation and allows control of the turn-on voltage. The structure includes source and drain diffusion regions formed in the silicon substrate, a gate, and n-wells formed under the source and drain diffusions on either side of the gate. A drain trench is located to separate the salicide between a drain contact and the gate edge,
10 and by controlling the size and location of the drain trench, the turn-on voltages can be controlled; i.e., the turn-on voltage due to drain diffusion region to substrate avalanche breakdown and the turn-on voltage due to source well to drain well punch-through. Thus, very low turn-on voltages may be achieved for ESD protection.

15 (FIGURE 1 IS SUGGESTED FOR PUBLICATION)