

ABSTRACT

A technique is provided that reduces dullness of a potential provided to a line such as gate line on an active-matrix substrate to enable driving the line at high speed and, at the same time, reduces the size of the picture frame region. On an active-matrix substrate (20a) are provided gate lines (13G) and source lines. On the active-matrix substrate (20a) are further provided: gate drivers (11) each including a plurality of switching elements, at least one of which is located in a pixel region, for supplying a scan signal to a gate line (13G); and lines (15L1) each for supplying a control signal to the associated gate driver (11). A control signal is supplied by a display control circuit (4) located outside the display region to the gate drivers (11) via the lines (15L1). In response to a control signal supplied, each gate driver (11) drives the gate line (13G) to which it is connected.