

The invention relates to a programmable frequency divider for integral divider ratios according to the preamble to Claim 1 and to a programmable frequency divider for integral and fractional divider ratios according to the preamble to Claim 2.

Such a frequency divider is known from D. Nüßmann, "Impuls- und Videotechnik, Infrarot-Systeme, digitale Signalverarbeitung und NF-Technik, Franzis Verlag GmbH Munich, 1984, pages 157-160 and 166-169. In this known frequency divider the output of the flipflop is connected to the control input of the first divider circuit by way of a logic element which alters an integral portion of the divider ratio.

A programmable frequency divider with the features set out above is also known from DE-OS 35 03 182. This known frequency divider makes it possible to predetermine divider ratios between the value 1.0 and 2.0. In order to achieve the desired divider ratio needle pulses are obtained from the output of a first divider circuit and from the outputs of a second divider circuit and these are supplied to one static input of a flipflop. The other static input of the flipflop receives high-frequency input signals, such as also reach the input of the first divider circuit. The input of the first divider circuit is both the input for the high-frequency signals and also the control input for predetermining the divider ratio. The divider ratio is then adjusted so that by corresponding setting of the flipflop the input of the first divider circuit is alternately cleared and locked for high frequency signals according to the desired ratio.

The known programmable frequency divider is not appropriate for all applications. This is the case when a very wide range of variations of the divider ratio is required. Such an application occurs for example in a magnetic or optical recording device in which after a predetermined function a write/read head is to be brought quickly and precisely to specific tracks or storage locations.

In order to achieve a high resolution corresponding to an integral and fractional divider ratio, in addition to the wide range of variations, a higher output frequency could also be used as the starting point and the divider ratio could then be restricted to integral values. However, such a solution has disadvantages since the high output frequencies which are then required could cause interference in a useful signal range or the necessary components would have to be designed for rapid signal processing, which would also be associated with the production of interference components in the signal processing.

The object of the invention is to create a programmable frequency divider for integral and/or fractional divider

ratios which offers a wide range of variations of the divider ratio as well as a high resolution in the case of fractional portions of the divider ratio.

This object is achieved in a programmable frequency divider according to the preamble to Claim 1 or 2 by the features set out in the characterising portion thereof.

By the use of a flipflop with dynamic input the control of the flipflop can be uncoupled from the high-frequency input side of the first divider circuit. This measure makes it possible to alter the divider ratio in another way than by timewise suppression of the high-frequency input signal. Thus abrupt frequency changes, which on average only when considered over a longer period of time would correspond to a fractional divider ratio, are avoided whilst on the other hand making possible a wide range of variations of the divider ratio which is continuously variable in fine gradations.

This takes place in that the integral component is predetermined in a manner which is known *per se* by way of the control input of the first divider circuit and the fractional component is obtained by switching the divider ratio to and fro between two values. Thus the low output frequency only swings to and fro between two values which preferably differ by the value "one". In this way the mean value is set over one period. This swinging to and fro is quite sufficient for most practical applications, since in the case of driving mass-loaded systems an equalisation is brought about by the inertia or there is a tolerance band width which is not exceeded in the short-duration range by the swinging of the output frequencies.

In the drawings;

Figure 1 shows a block diagram of the programmable frequency divider according to the invention,

Figure 2 shows pulse diagrams in a frequency divider according to Figure 1.

In the embodiment the programmable frequency divider serves for control of a motor for track guiding of a write/read head of a data recording device.

In this case the programmable frequency divider is formed by the assemblies in the block shown by broken lines. In detail it comprises a first divider circuit 1, a second divider circuit 5, a dynamic, i.e. single-edge-triggered flipflop 8, an adder 12 and a comparator 16. The first divider circuit receives a higher frequency signal at its input 2 by way of a pre-divider 21 which is supplied by an oscillator 20. A signal of a sub-divided low frequency can be tapped at an output 3 of the first divider circuit 1. By

way of a control input 4 the divider ratio is predetermined in the form of a data item for the first divider circuit 1. The data item comprises a total of 12 bits, of which the 9 bits of higher value make up an integral component of the divider ratio. The data item determined for the first divider circuit 1 is applied to a first input 13 of the adder 12 and is passed to the control input 4 of the first divider circuit by way of an output 15.

From the output 3 of the first divider circuit 1 a line A leads to an input 6 of the second divider circuit 5. An output 7 of the second divider circuit 5 comprises three lines B, C, D, all of which are directed to a first input 17 of the comparator 16. The line D which represents the highest-value place at the output 7 of the second divider circuit 5 is also connected to a dynamic input 9 of the flipflop 8. An output 11 of the flipflop 8 leads by way of a line F to a second input 14 of the adder 12. In this case the line F corresponds to the low-value place at the second input 14 of the adder 12.

A data item which comprises three bits and corresponds to the fractional portion of the divider ratio can be predetermined by way of a second input 18 of the comparator 16. A parity output 19 is connected by way of a line E to a static input 10 of the flipflop 8.

With the illustrated programmable frequency divider, by corresponding predetermination of the divider ratio from the constant high-frequency signal at the input 2 a signal of a desired lower frequency can be produced at the output 3. For this purpose corresponding data items are applied to the inputs 13 and 18. First of all it should be assumed that an integral divider ratio is desired. In this case it is sufficient only to predetermine the data item appropriately at the input 13 and to set the input 18 at all places to zero. The first divider circuit 1 then completely takes over the frequency division, whilst the assemblies designated by 5, 8, 12 and 16 are non-operational in practice.

If a fractional divider ratio should be chosen, a data item must also be applied to the second input 18 of the comparator 16. By feeding the signal at the output 3 of the first divider circuit into the input 6 of the second divider circuit 5 the dynamic input 9 of the flipflop 8 is triggered by way of the line D in each case after eight cycles and thereupon the output signal of the flipflop 8 is supplied to the second input 14 of the adder 12 by way of the line F with a transmission signal. The data item then appears increased by the value "one" at the output 15 of the adder 12. In this way the divider ratio of the first divider circuit 1 is altered.

After waiting a number of cycles corresponding to the data

item at the input 18 of the comparator 16, that is to say conformity of the signals is achieved at the first input 17 and at the second input 18, a parity signal appears at the parity output 19, passes by way of the line E to the static input 10 of the flipflop 8 and resets the latter. The transmission signal F disappears and at the control input 4 of the first divider circuit the data item again occurs in an identical manner as at the first input 13 of the adder 12.

This process is repeated cyclically, so that the divider ratio of the first divider circuit 1 swings to and fro between two values and thus a mean value is produced which corresponds to the entire predetermined divider ratio from the data items at the input 13 and at the input 18.

The operation of the programmable frequency divider according to the invention can also be explained with the aid of a pulse diagram such as that shown in Figure 2. First of all it may be remarked that the time scale of this representation is shown distorted, since the period of the illustrated cycles varies when the divider ratio changes.

In the upper four lines the signals are shown in the lines A, B, C, D. It is just assumed that the lines B, C and D at the output 7 of the second divider circuit 5 lie at precisely 1 potential and that when the next pulse arrives they switch over together to 0 potential. Since the flipflop 8 is triggered by the negative edge on the line D, this procedure leads to a 1 potential on the line F. In the central part of the illustration the signals on the lines E and F are given for three different data items at the input 18 of the comparator 16. These are 1) the data item 001, 2) the data item 011 and 3) the data item 111. According to the predetermined data item at the input 18 the same numbers of cycles on the line A are waited until the comparator 16 sets the flipflop 8 by way of the line E and the potential on the line F returns to zero.

As can be seen from the illustrations for the three different data items, in this way a different ratio of the duration of the potentials on the line F is produced. The divider ratio of the first divider circuit 1 is also varied accordingly. The effects of this measure on the frequency of the signal at the output 3 of the first divider circuit is illustrated for the third case, that is to say for the case of the data item 11, at the input 18, and in fact here the various frequencies are plotted over the time axis t .

Due to the alternation of potential on the line F the frequency divider is switched to and fro between the frequencies f_o and f_u . Thus a mean value f_m is set which is produced by the fractional divider ratio in relation to the input frequency.

The assemblies designated by 5, 8, 12 and 16 do not need to be provided as discrete components. It is also possible to provide a computer for this and to have the functions carried out appropriately under program control. This is particularly advantageous when a computer is necessary in any case for determining the divider ratio, e.g. for controlling a motor. In this case the cycles occurring at the output 3 of the first divider circuit 1 are counted by the computer. They are then set into the ratio with integral values of cycles of the signals corresponding to the fractional portion. Thus numerators and denominators of the fractional portion are extended so that they agree with integral values of cycles of the signal.

Then for the duration of the cycles corresponding to the numerator of the fractional portion the integral portion of the divider ratio is increased by "one" and then lowered in fact until the end of the cycles corresponding to the denominator of the fractional portion. Then the divider ratio is again increased by "one". This process can also be carried out by simple program commands, so that swinging to and fro of the divider ratio and thus of the frequency of the signal at the output 3 is equally achieved.

In applications which do not require any variation over the entire possible range of the divider ratio it can also be sufficient to restrict the integral divider ratio and instead to provide a constant pre-divider. If the programmable frequency divider is to be constructed for an even higher frequency resolution then instead of the three-place construction of the second divider circuit 5 and of the comparator 16 assemblies of four- or multi-place construction can also be used.

Claims

1. Programmable frequency divider for integral divider ratios, comprising a first divider circuit (1), wherein a high-frequency signal can be applied to the input (2) thereof and a signal of a sub-divided low frequency can be tapped at the output (3) thereof, with a control input (4) for predetermining a divider ratio, also comprising a second divider circuit (5), the input (6) of which lies at the output (3) of the first divider circuit (1), and a flipflop (8), the input (9) of which is connected to the output (7) of the second divider circuit (5) whilst the output (11) thereof is connected to the control input (4) of the first divider circuit (1), characterised in that the output (11) of the flipflop (8), which serves as a single-edge-triggered flipflop (8), is connected to the control input (4) of the first divider circuit (1) via an adder (12) which varies an integral part of the divider ratio, and that the control input (4) of the divider circuit (1) is constructed for predetermining a part of a multi-place data item, the output (11) of the flipflop (8) being assigned to the lowest-value place at the input (14) of the adder (12).

2. Programmable frequency divider for fractional divider ratios, comprising a first divider circuit (1) wherein a high-frequency signal can be applied to the input (2) thereof and a signal of a sub-divided low frequency can be tapped at the output (3) thereof, with a control input (4) for predetermining a divider ratio, also comprising a second divider circuit (5), the input (6) of which lies at the output (3) of the first divider circuit (1), and a flipflop (8), the input (9) of which is connected to the output (7) of the second divider circuit (5) whilst the output thereof is connected to the control input (4) of the first divider circuit (1), characterised in that the output (11) of the flipflop (8), which serves as a single-edge-triggered flipflop (8), is connected to the control input (4) of the first divider circuit (1) via an adder (12) which varies an integral part of the divider ratio, and that the control input (4) of the first divider circuit (1) is constructed for predetermining a part of a multi-place data item, the output (11) of the flipflop (8) being assigned to the lowest-value place at the input (14) of the adder (12), and that the dynamic input (9) of the flipflop (8) is connected to the highest-value bit equalisation line (7, D) of the output of the second divider circuit, that the output (7) of the second divider circuit (5) lies at a first input (17) of a comparator (16), the parity output (19) of which is connected to a static input (10) of the flipflop (8), and that a second input (18) of the comparator (16) is constructed for predetermining a data item which predetermines the fractional part of the divider ratio.

3. Programmable frequency divider according to Claim 1 or



2, characterised in that the control input (4) of the first divider circuit (1) and the second input (18) of the comparator (16) are jointly constructed for predetermining the data item which gives the complete divider ratio.

4. Programmable frequency divider according to one or more of Claims 1 to 3, characterised in that the second divider circuit (5) is a binary divider circuit comprising three bits.

