CLAIMS:

1. A spatial light modulator comprising:

a pixel array having a plurality of pixels whereby each pixel is communicatively connected to a digital pixel circuit whereby each digital pixel circuit comprises:

a Static Random Access Memory (SRAM) circuit configured to receive column data signals and a clock row enable signal, *ck_row*, whereby the SRAM circuit is triggered by the clock row enable signal, *ck_row*, to sample the received column data signals;

a hold buffer circuit coupled to an output of the SRAM circuit, the hold buffer circuit configured to receive a clock hold signal, *ck_hold*, whereby the hold buffer circuit is triggered by the clock hold signal, *ck_hold*, to receive and store the sampled signal from the output of the SRAM circuit.

2. The spatial light modulator according to claim 1 further comprising:

a bit-plane control circuit communicatively connected to all the digital pixel circuits, the bit-plane control circuit being configured to:

generate, using a pulse code modulation (PCM) scheme, bit-plane signals,

whereby each bit-plane signal comprises a variable holding time component for triggering the hold buffer circuit in each of the digital pixel circuits for a variable time period T_{Hold_N}, and a predetermined addressing time component for triggering the SRAM circuit in each of the digital pixel circuits for a predetermined time period T_{Add}.

3. The spatial light modulator according to claim 2 whereby the addressing time component is predetermined based on a unit duration of a Least Significant Bit (LSB) of a bit-plane signal and a pixel multiplier, α_p wherein the pixel multiplier, α_p is based on numbers of rows and columns, and data input-output ports of the pixel array.

4. The spatial light modulator according to claim 3 whereby the pixel multiplier, α_p, is defined as:

$$\alpha_p = \frac{(Number\ of\ rows)x(Number\ of\ columns)}{(Number\ of\ data\ input/output\ ports)}$$

5. The spatial light modulator according to claim 1 whereby each pixel in the pixel array comprises a liquid crystal layer provided between an indium tin oxide (ITO) electrode and a pixel electrode, whereby the ITO electrode is configured to receive an alternating voltage and the pixel electrode is connected to an output of the digital pixel circuit.

6. The spatial light modulator according to claim 2 whereby each pixel in the pixel array comprises a liquid crystal layer provided between an indium tin oxide (ITO) electrode and a pixel electrode, whereby the pixel electrode is connected to an output of the digital pixel circuit and the ITO electrode is configured to receive an alternating voltage from the bit-plane control circuit, whereby the alternating voltage is synchronized with an output signal at the output of the digital pixel circuit.

7. The spatial light modulator according to claim 1 whereby the hold buffer circuit comprises:

a first and a third transistor having input gates coupled to the output of the SRAM circuit;

a second and a fourth transistor having input gates configured to receive the clock hold signal, *ck_hold*,

whereby a drain node of the second transistor is coupled to a source node of the first and third transistors.

8. The spatial light modulator according to claim 7 whereby a transistor of the hold buffer circuit is shared between two or more digital pixel circuits.

9. A method for modulating spatial light using a spatial light modulator that has a pixel array which comprises a plurality of pixels whereby each pixel is communicatively connected to a digital pixel circuit, the method comprising

receiving, using a Static Random Access Memory (SRAM) circuit provided within each digital pixel circuit, column data signals and a clock row enable signal, *ck_row*, whereby the SRAM circuit is triggered by the clock row enable signal, *ck_row*, to sample the received column data signals;

receiving, using a hold buffer circuit coupled to an output of the SRAM circuit, a clock hold signal, *ck_hold*, whereby the hold buffer circuit is triggered by the clock hold signal, *ck_hold*, to receive and store the sampled signal from the output of the SRAM circuit.

10. The method according to claim 9 further comprising:

generating, using a bit-plane control circuit communicatively connected to all the digital pixel circuits, bit-plane signals based on a pulse code modulation (PCM) scheme,

whereby each bit-plane signal comprises a variable holding time component for triggering the hold buffer circuit in each of the digital pixel circuits for a variable time period T_{Hold_N}, and a predetermined addressing time component for triggering the SRAM circuit in each of the digital pixel circuits for a predetermined time period T_{Add}.

11. The method according to claim 10 whereby the addressing time component is predetermined based on a unit duration of a Least Significant Bit (LSB) of a bit-plane signal and a pixel multiplier, α_p wherein the pixel multiplier, α_p is based on numbers of rows and columns, and data input-output ports of the pixel array.

12. The method according to claim 11 whereby the pixel multiplier, α_p, is defined as

$$\alpha_p = \frac{(Number\ of\ rows)x(Number\ of\ columns)}{(Number\ of\ data\ input/output\ ports)}$$

13. The method according to claim 9 whereby each pixel in the pixel array comprises a liquid crystal layer provided between an indium tin oxide (ITO) electrode and a pixel electrode, whereby the ITO electrode is configured to receive an alternating voltage and the pixel electrode is connected to an output of the digital pixel circuit.

14. The method according to claim 10 whereby each pixel in the pixel array comprises a liquid crystal layer provided between an indium tin oxide (ITO) electrode and a pixel electrode, whereby the pixel electrode is connected to an output of the digital pixel circuit and the ITO electrode is configured to receive an alternating voltage from the bit-plane control circuit, whereby the alternating voltage is synchronized with an output signal at the output of the digital pixel circuit.

15. The method according to claim 9 whereby the hold buffer circuit comprises:

a first and a third transistor having input gates coupled to the output of the SRAM circuit;

a second and a fourth transistor having input gates configured to receive the clock hold signal, *ck_hold*,

whereby a drain node of the second transistor is coupled to a source node of the first and third transistors.

16. The method according to claim 15 whereby a transistor of the hold buffer circuit is shared between two or more digital pixel circuits.