

ABSTRACT

INTEGRATED CIRCUIT HAVING STATE MACHINE-DRIVEN FLOPS IN WRAPPER CHAINS FOR DEVICE TESTING

Integrated circuits are described that utilize internal state machine-driven logic elements (e.g., flops) within input and/or output wrapper chains that are used to test internal core logic of the integrated circuit. One or more individual logic elements of the wrapper chains within the integrated circuit is implemented as a multi-flop state machine rather than a single digital flip-flop. As multi-flop state machines, each enhanced logic element of a wrapper chain is individually configurable to output pre-selected values so as to disassociate the state machine-driven flops from signal transmission delays that may occur in the input or output wrapper chains of the integrated circuit.

(fig. 1)