

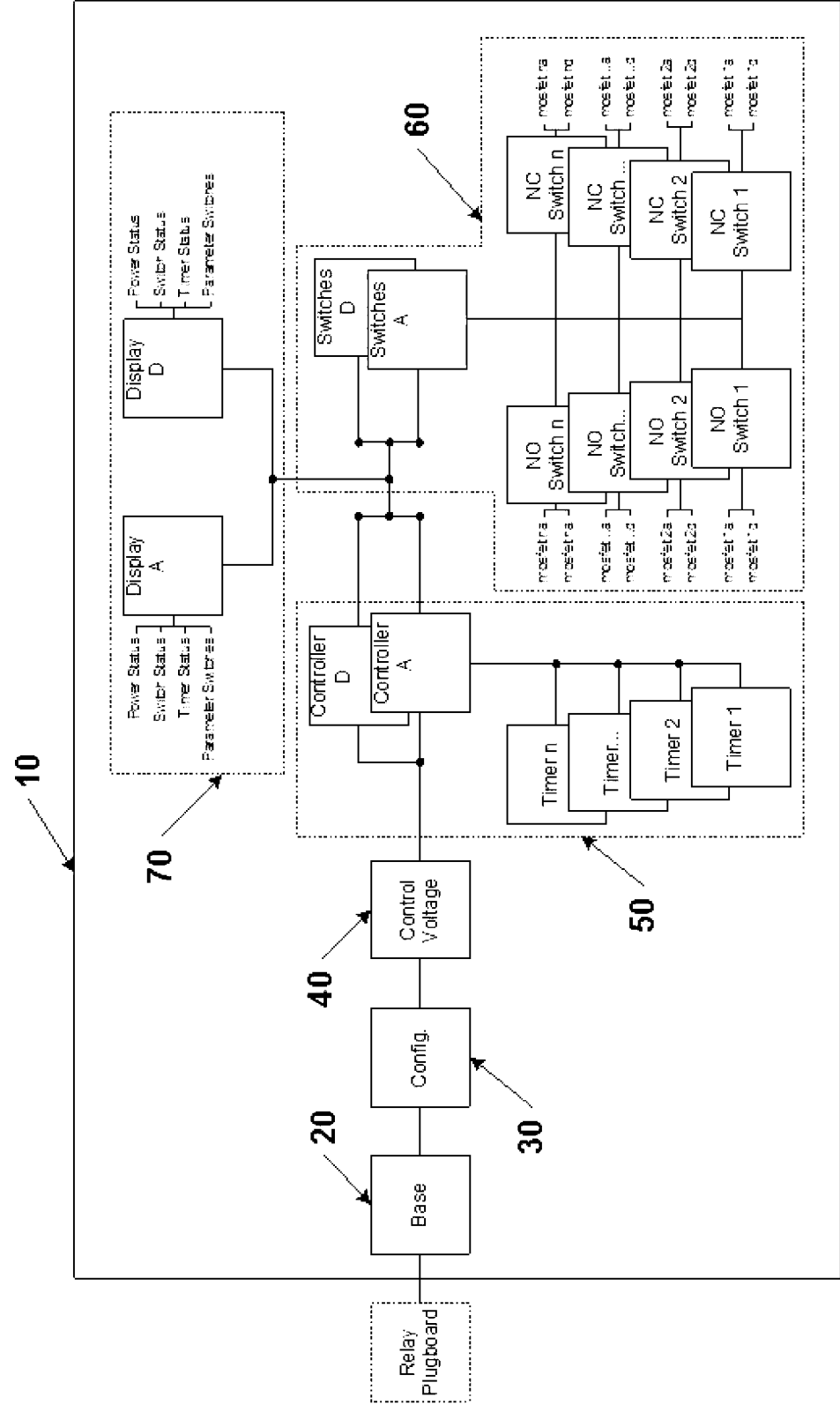


Figure 1

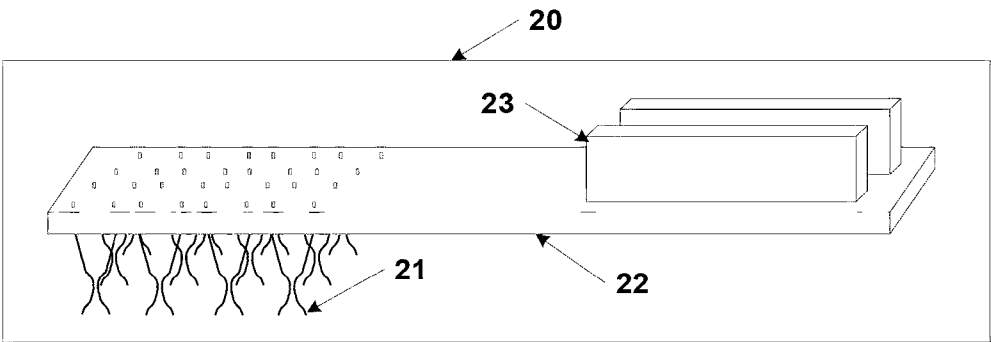


Figure 2

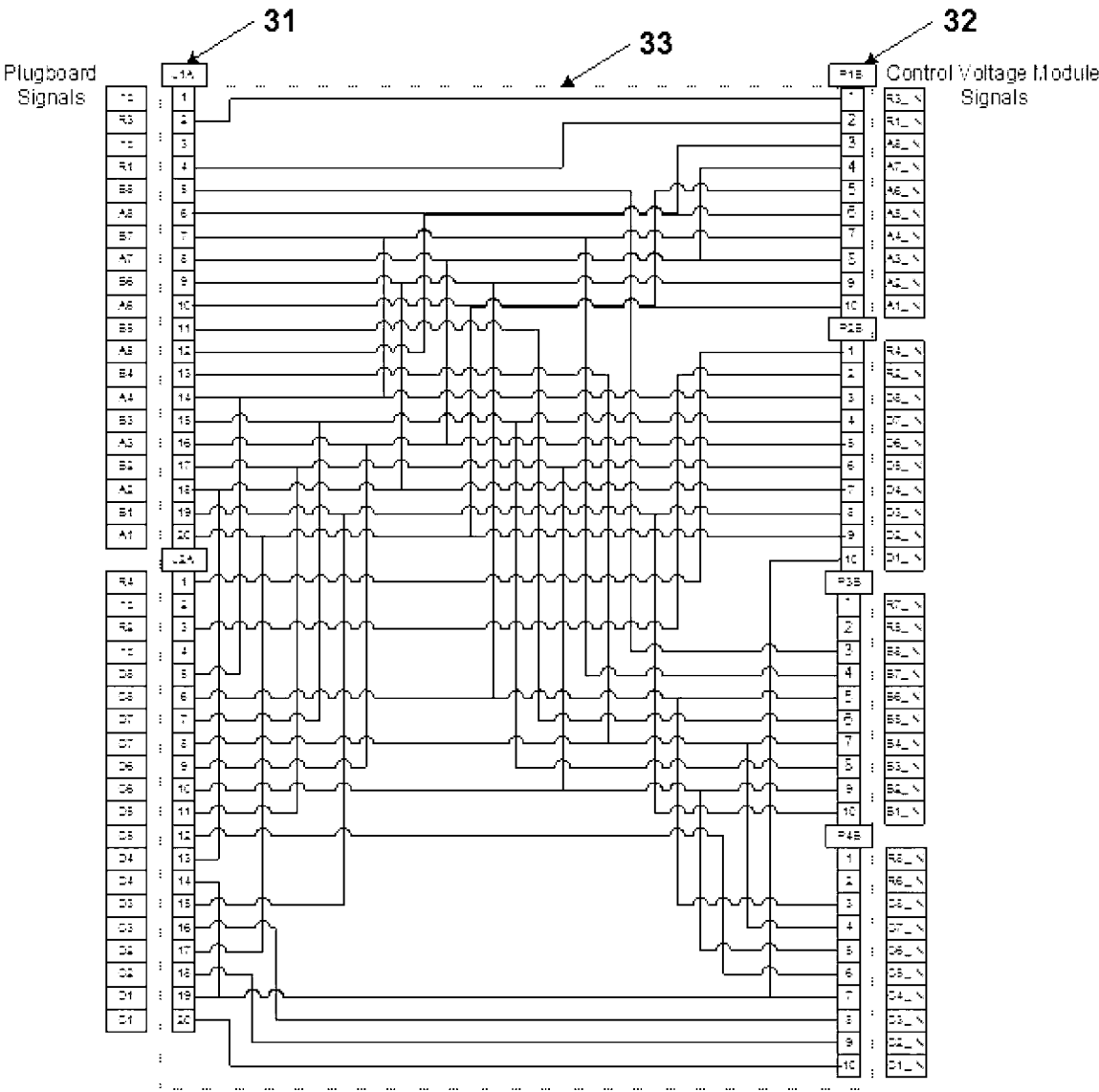


Figure 3

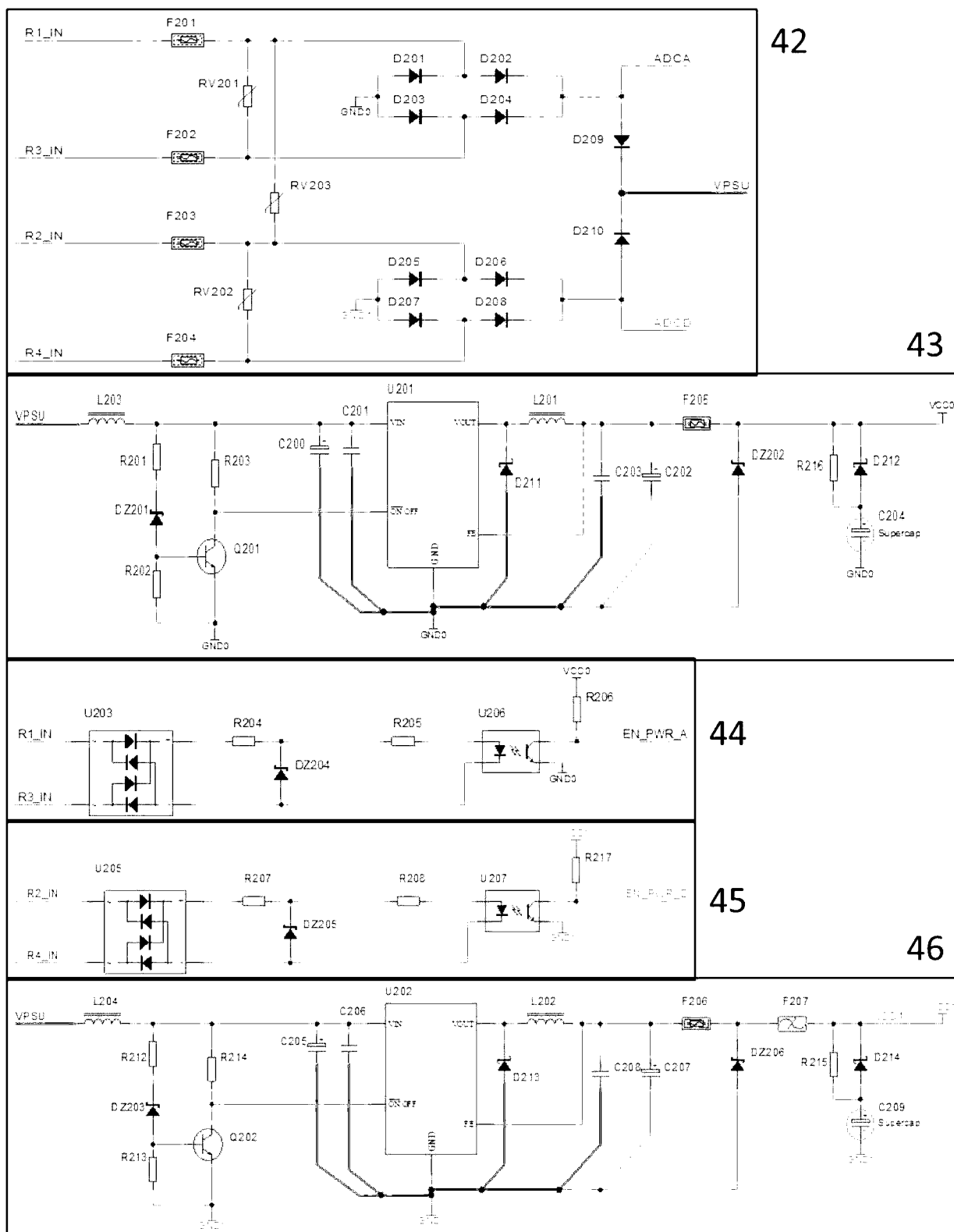


Figure 4

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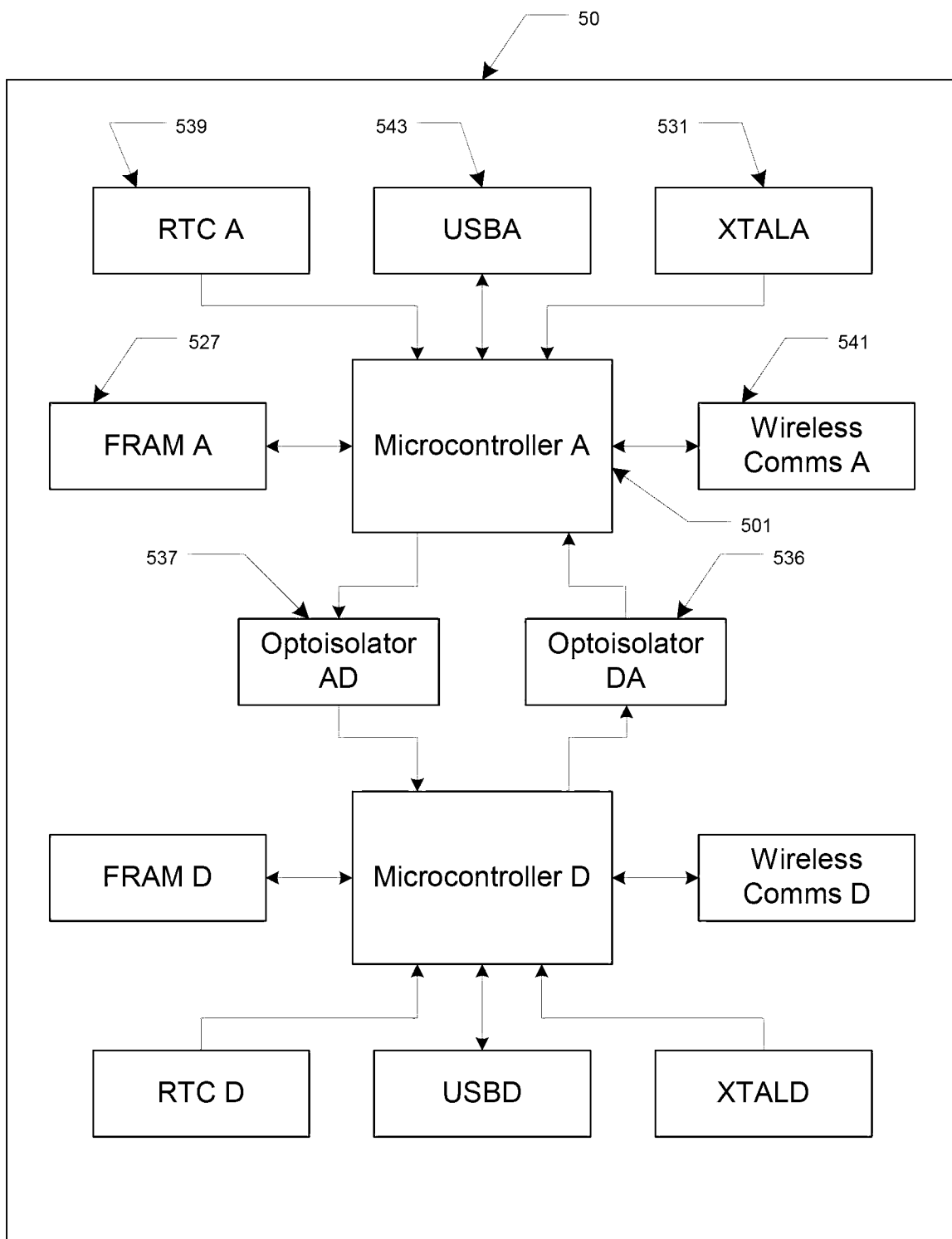


Figure 5

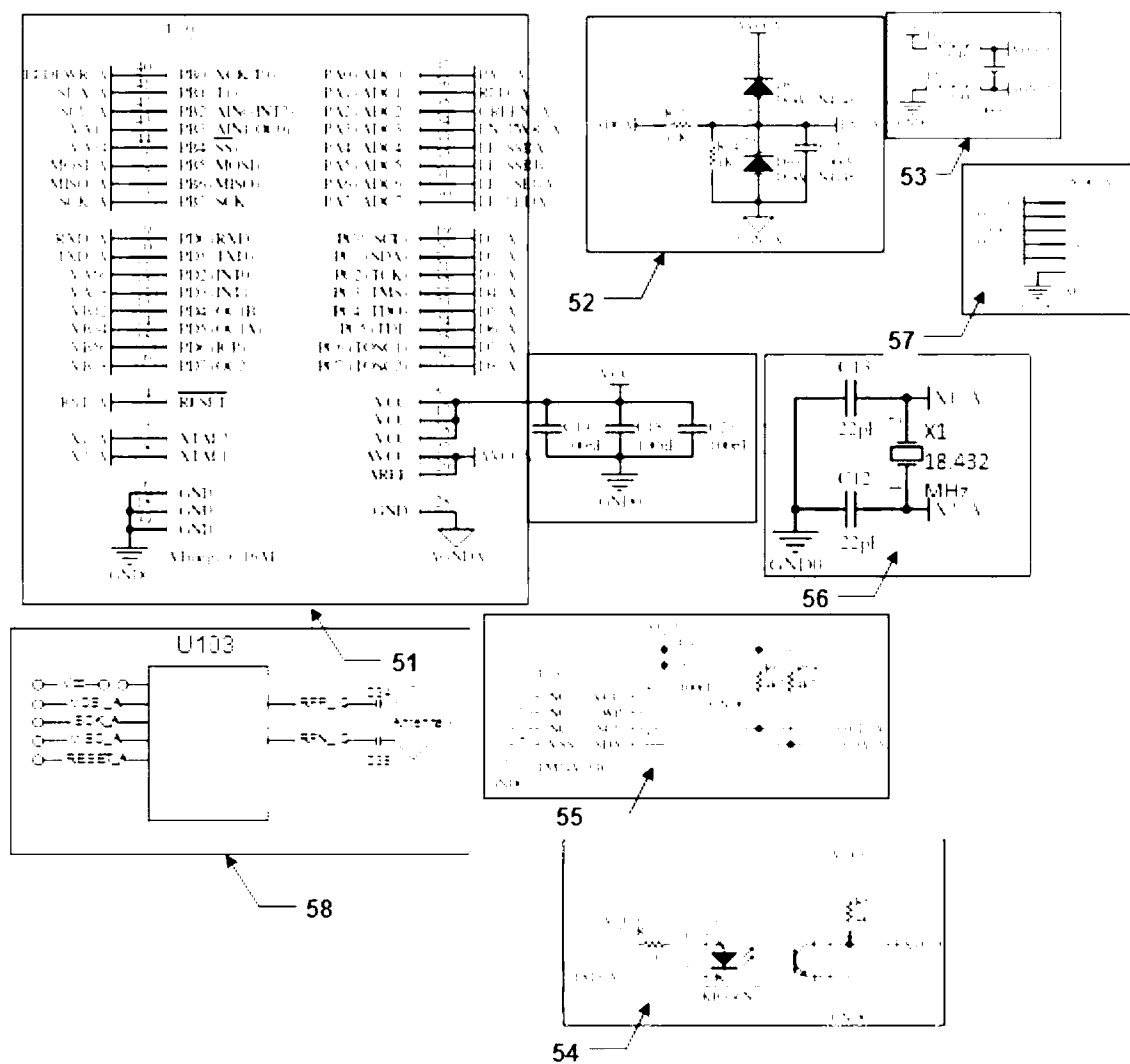


Figure 5A

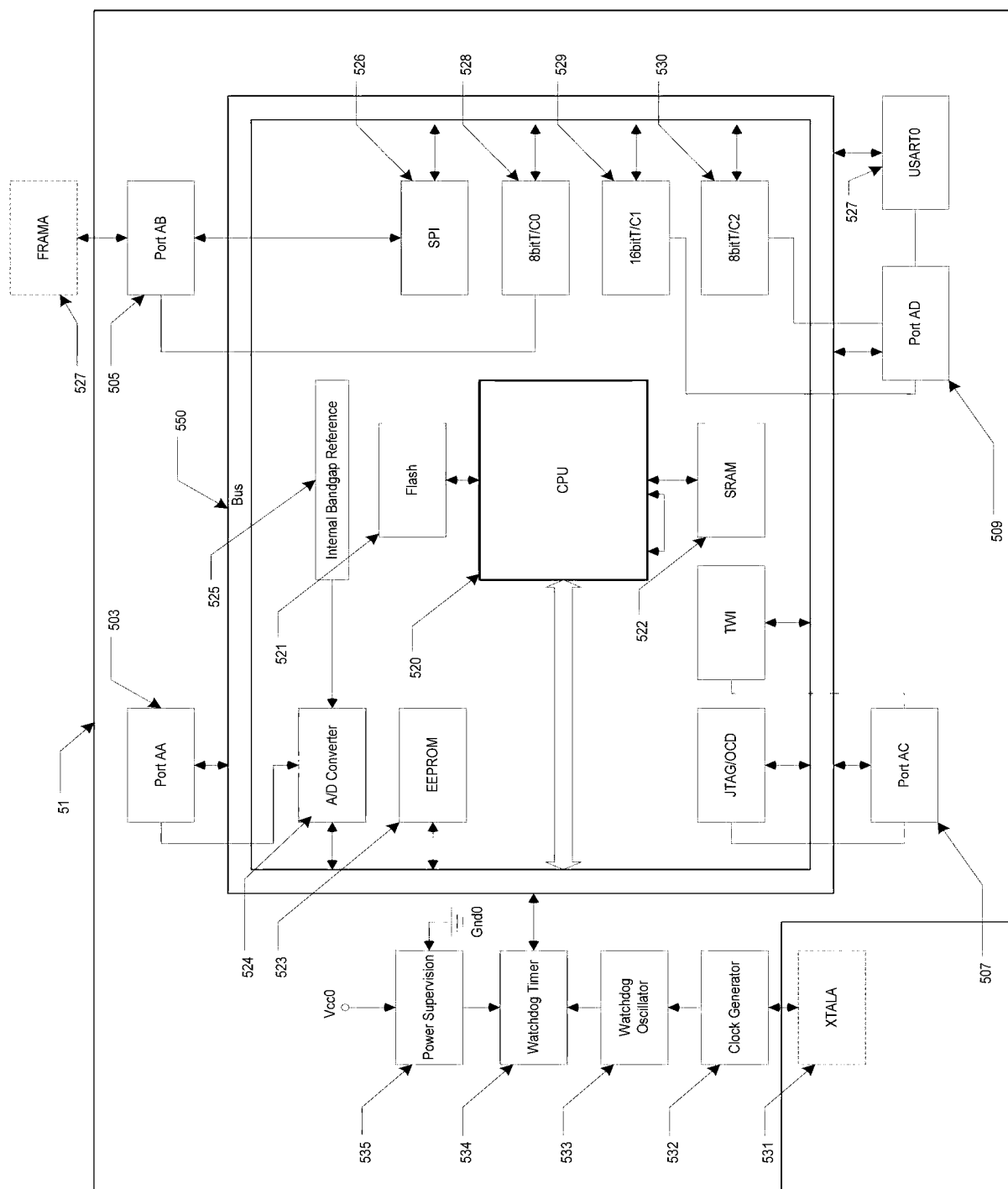
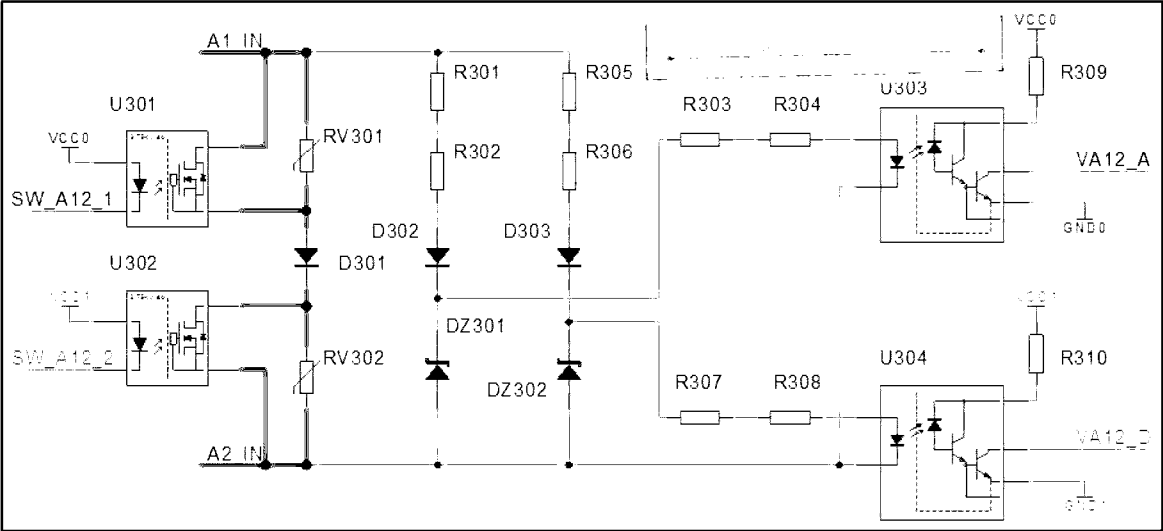


Figure 5B

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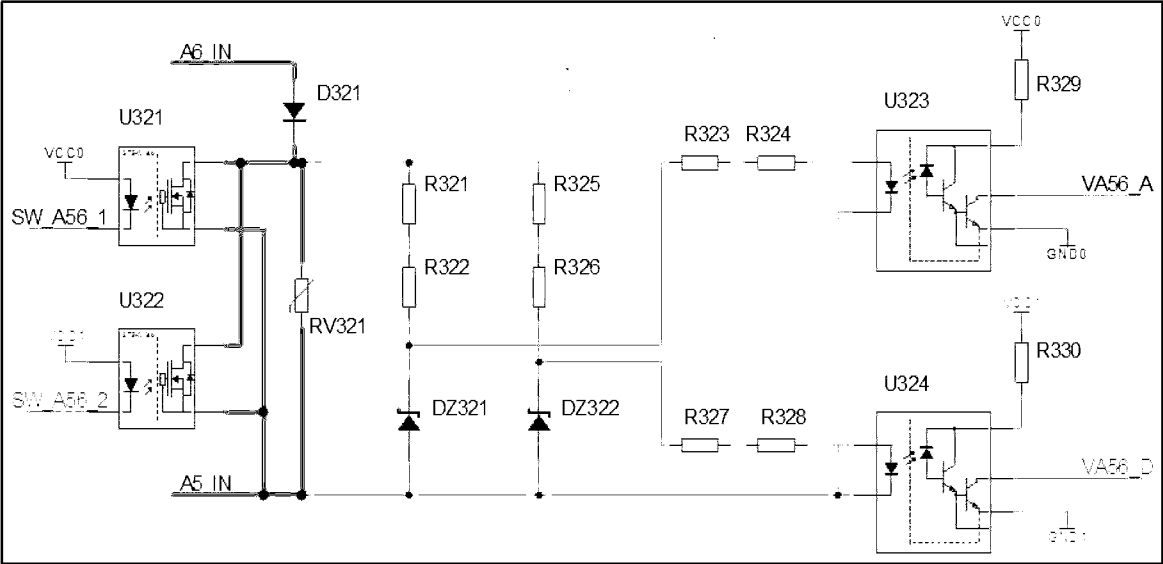


Figure 6

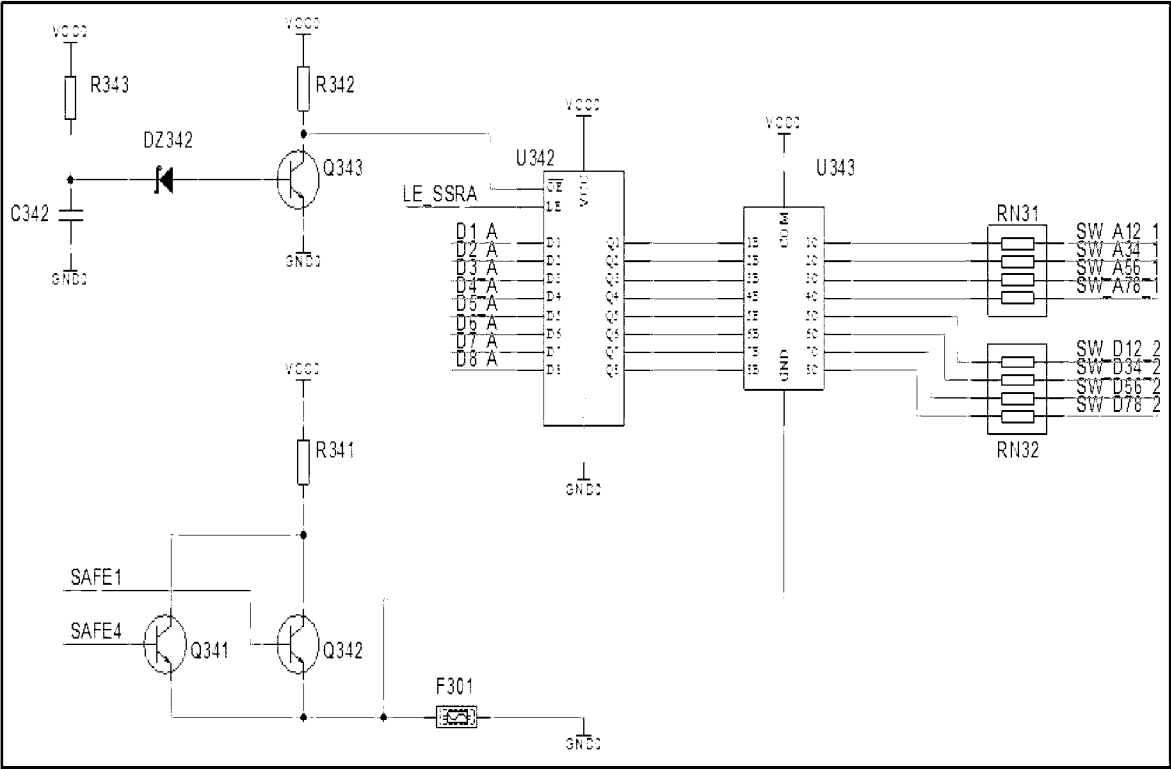


Figure 6A

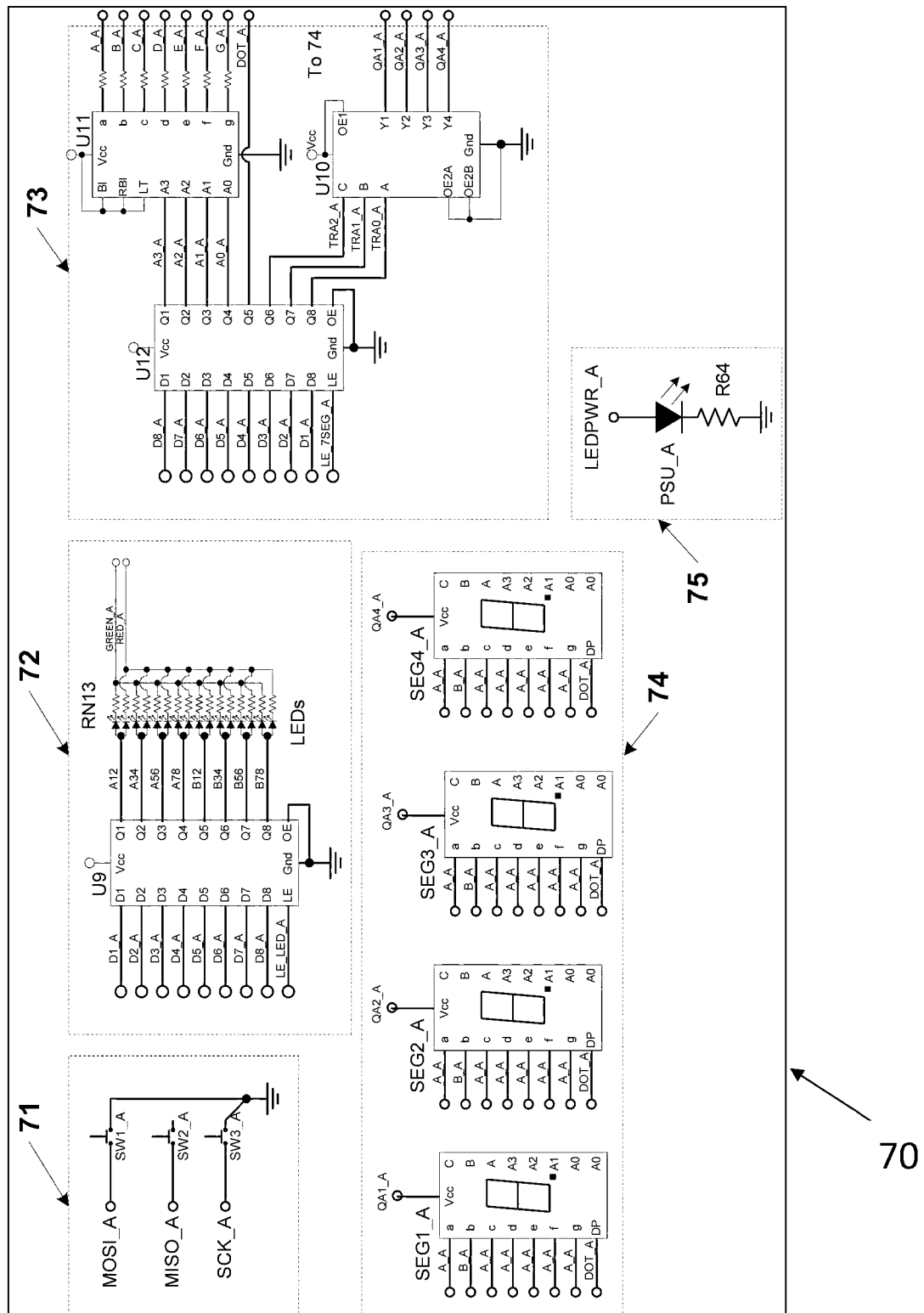


Figure 7

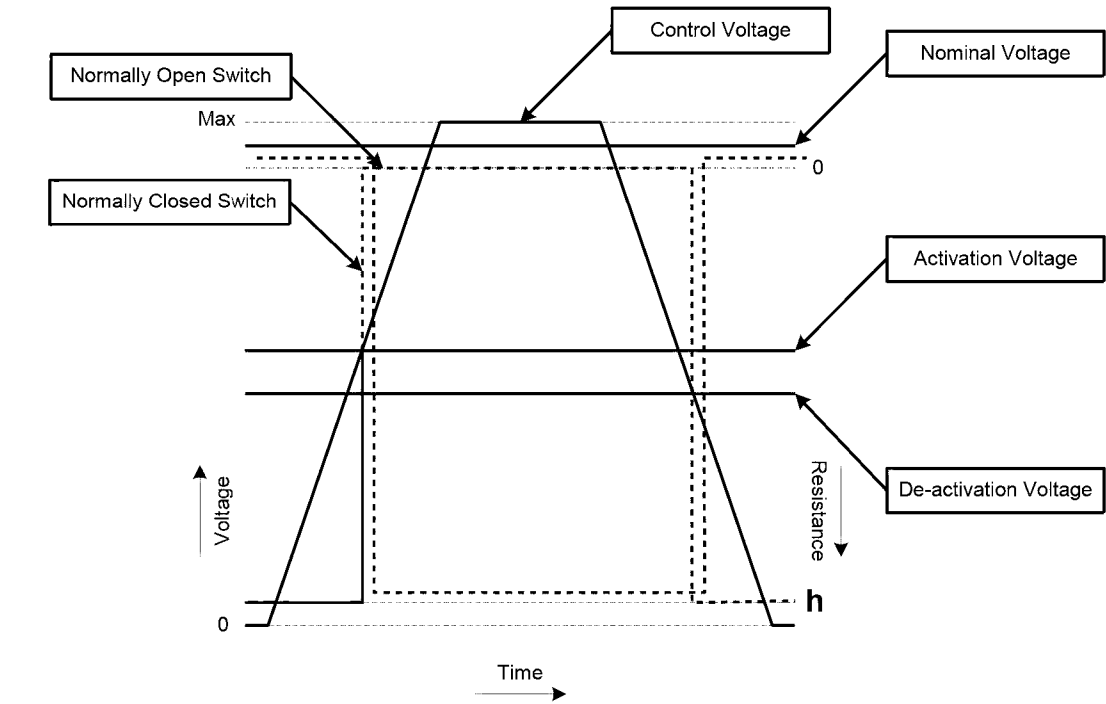


Figure 8

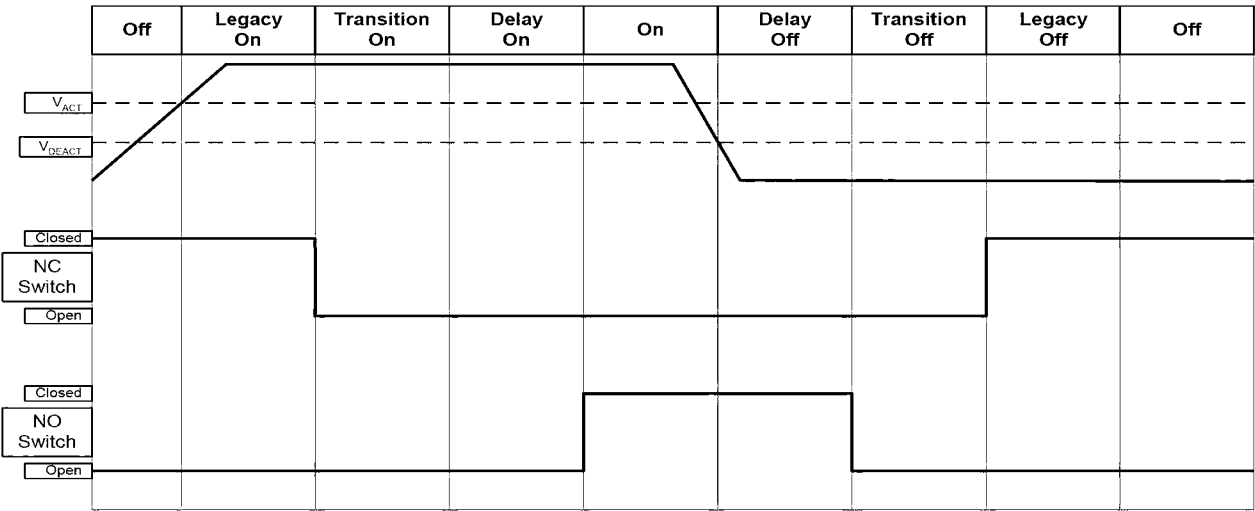
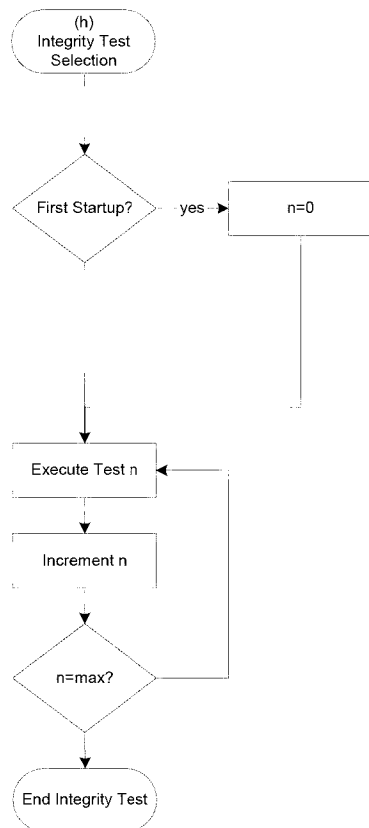
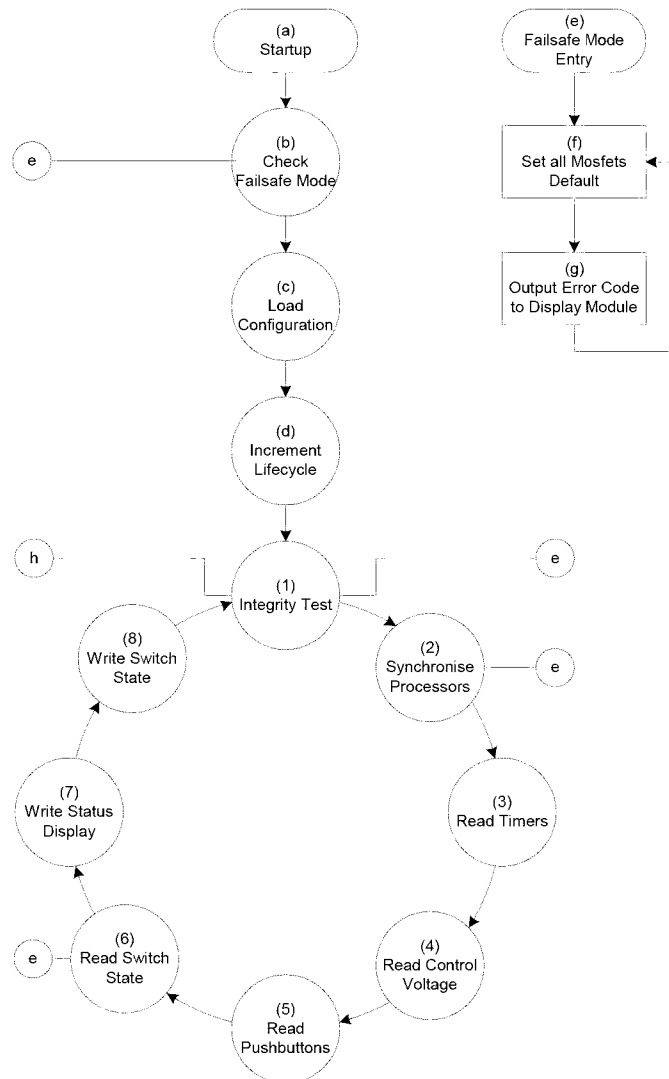


Figure 9

Integrity Test Selection



Main Loop



Failsafe Mode

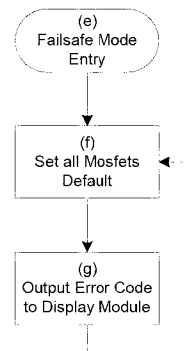


Figure 10

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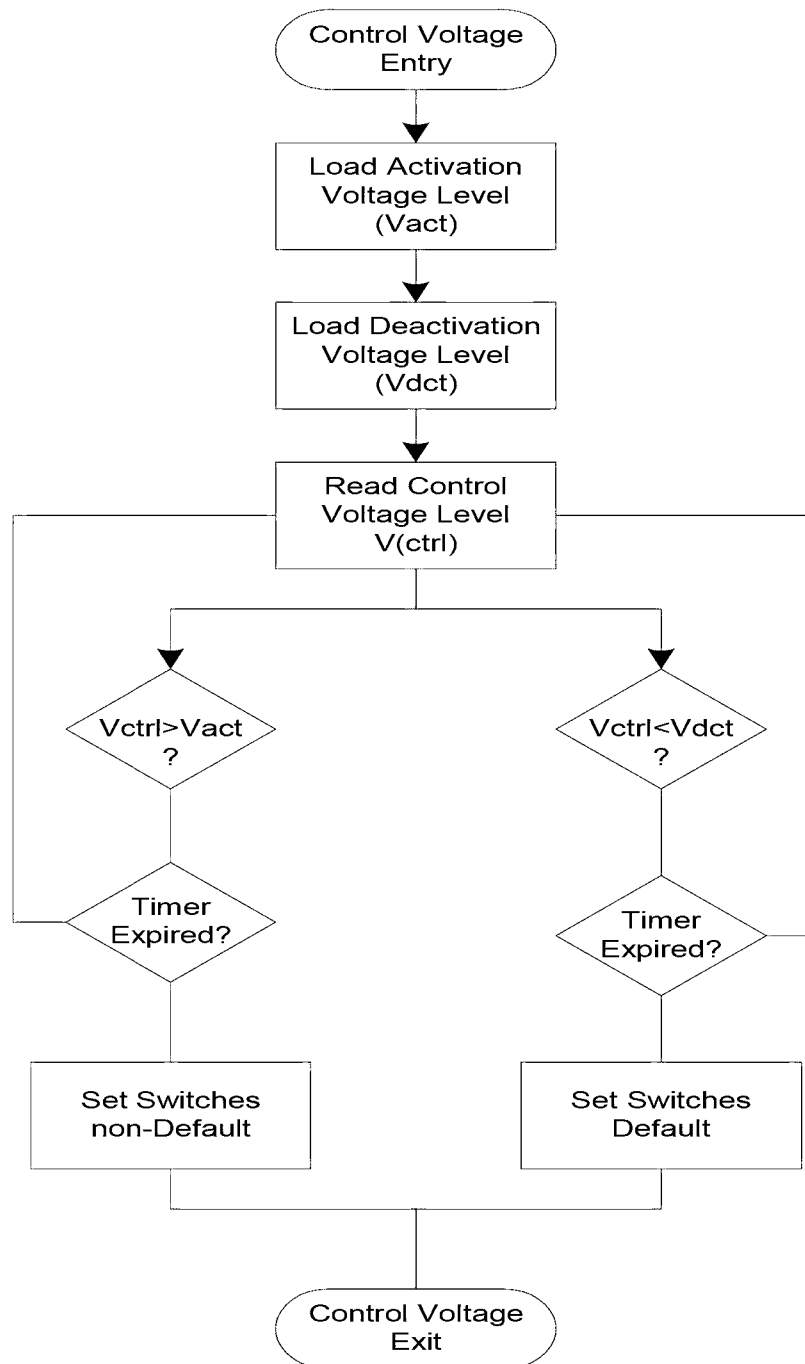


Figure 11